PC-100/CL2 SDRAM Unbuffered DIMM

32Mx64bits SDRAM DIMM based on 16Mx8, 4Bank, 4K Refresh, 3.3V SDRAM

General Description

The VDAAA1816 is 32Mx64 bits Synchronous DRAM Modules, The modules are composed of sixteen 16Mx8 bits CMOS Synchronous DRAMs in TSOP-II 400mil 54pin package and one 2Kbit EEPROM in 8pin TSSOP(TSOP) package on a 168pin glass–epoxy printed circuit board.

The V-Data is a Dual In-line Memory Module and is intended for mounting onto 168-pins edge connector sockets. Fully synchronous operation referenced to the positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock. The data paths are internally pipelined to achieve very high bandwidth.

Features

- PC-100/CL2 support
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Single 3.3±0.3V power supply
- All device pins are compatible with LVTTL interface
- Data mask function by DQM
- Serial Presence Detect with EEPROM
- Module bank : two physical bank
- PCB : B6986RAB,Height (28.00mm),double sided component, Four layers

Ordering Information.

Part No.	Frequency	Bank	Ref.	Package
VDAAA1816	100Mhz/CL2	4 Banks	4K	TSOP II

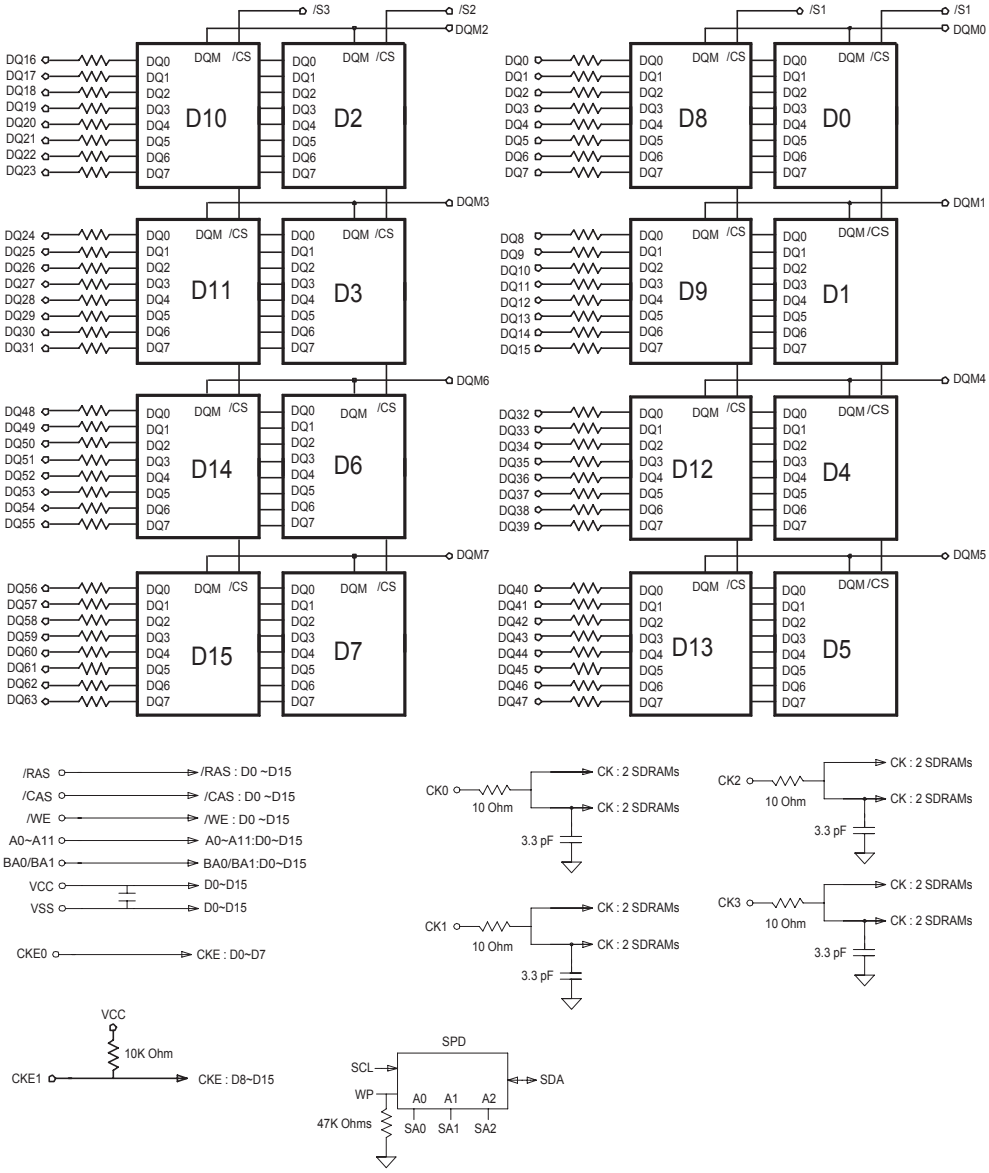
Pin Assignment

FRONT SIDE								BACK SIDE							
PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	VSS	22	NC	43	VSS	64	VSS	85	VSS	106	NC	127	VSS	148	VSS
2	DQ0	23	VSS	44	NC	65	DQ21	86	DQ32	107	VSS	128	CKE0	149	DQ53
3	DQ1	24	NC	45	/CS2	66	DQ22	87	DQ33	108	NC	129	NC	150	DQ54
4	DQ2	25	NC	46	DQM2	67	DQ23	88	DQ34	109	NC	130	DQM6	151	DQ55
5	DQ3	26	VCC	47	DQM3	68	VCC	89	DQ35	110	VCC	131	DQM7	152	VCC
6	VCC	27	/WE	48	NC	69	DQ24	90	VCC	111	/CAS	132	NC	153	DQ56
7	DQ4	28	DQM0	49	VCC	70	DQ25	91	DQ36	112	DQM4	133	VCC	154	DQ57
8	DQ5	29	DQM1	50	NC	71	DQ26	92	DQ37	113	DQM5	134	NC	155	DQ58
9	DQ6	30	/CS0	51	NC	72	DQ27	93	DQ38	114	NC	135	NC	156	DQ59
10	DQ7	31	NC	52	NC	73	VCC	94	DQ39	115	/RAS	136	NC	157	VCC
11	DQ8	32	VSS	53	NC	74	DQ28	95	DQ40	116	VSS	137	NC	158	DQ60
12	VSS	33	A0	54	VSS	75	DQ29	96	VSS	117	A1	138	VSS	159	DQ61
13	DQ9	34	A2	55	DQ16	76	DQ30	97	DQ41	118	A3	139	DQ48	160	DQ62
14	DQ10	35	A4	56	DQ17	77	DQ31	98	DQ42	119	A5	140	DQ49	161	DQ63
15	DQ11	36	A6	57	DQ18	78	VSS	99	DQ43	120	A7	141	DQ50	162	VSS
16	DQ12	37	A8	58	DQ19	79	CK2	100	DQ44	121	A9	142	DQ51	163	CK3
17	DQ13	38	A10/AP	59	VCC	80	NC	101	DQ45	122	BA0	143	VSS	164	NC
18	VCC	39	BA1	60	DQ20	81	WP	102	VCC	123	A11	144	DQ52	165	SA0
19	DQ14	40	VCC	61	NC	82	SDA	103	DQ46	124	VCC	145	NC	166	SA1
20	DQ15	41	VCC	62	NC	83	SCL	104	DQ47	125	CK1	146	NC	167	SA2
21	NC	42	CK0	63	NC	84	VCC	105	NC	126	NC	147	NC	168	VCC

Pin Description

PIN	NAME	FUNCTION
CK0~2	System Clock	Active on the positive edge to sample all inputs.
CKE0~1	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS0~3	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
A0~A12	Address	Row / Column address are multiplexed on the same pins.
BA0~BA1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63	Data	Data inputs / outputs are multiplexed on the same pins.
DQM0~7	Data Mask	Makes data output Hi-Z,
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CLK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CLK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VDD/VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
SDA	Serial data I/O	EEPROM serial data I/O
SCL	Serial clock	EEPROM clock input
SA0~2	Address in EEPROM	EEPROM address input
WP	Write Protect for EEPROM	Write Protect for Serial Presence Detect on DIMM
NC	No Connection	This pin is recommended to be left No Connection on the device.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{out}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 ℃

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH}=-2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL}=2mA
Input leakage current	I_{IL}	-5	-	5	uA	3
Output leakage current	I_{OL}	-5	-	5	uA	4

Note : 1. V_{IH} (max)=4.6V AC for pulse width ≦ 10ns acceptable.

2.V_{IL}(min)=-1.5V AC for pulse width ≦ 10ns acceptable.

3.Any input 0V ≦ V_{IN} ≦ V_{DD} + 0.3V, all other pins are not under test = 0V.

4.Dout is disabled, 0V ≦ V_{OUT} ≦ V_{DD}.

AC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 ℃

Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	V_{IH} / V_{IL}	2.4 / 0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	TR / tF	1	Ns	
Output timing measurement reference level	Voutfef	1.4	V	
Output load capacitance for access time measurement	CL	50	pF	2

Note: 1. 3.15V ≦ V_{DD} ≦ 3.6V

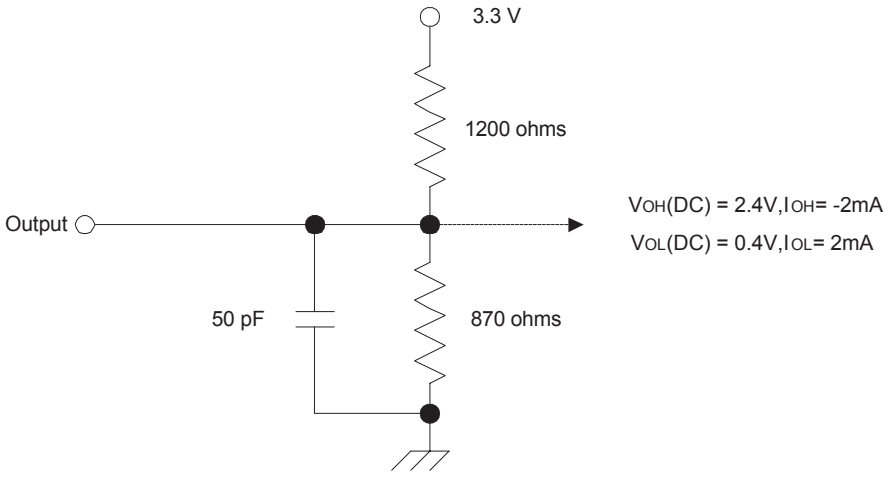
2. Output load to measure access times is equivalent to two TTL gates and one capacitor (30pF). For details, refer to AC/DC output load circuit.

Capacitance

TA=25℃, f-=1Mhz, VDD=3.3V

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	CI1	25	40	pF
	A0~A11,BA0,BA1,CKE,/CS,/RAS, /CAS,/WE,DQM	CI2	40	55	pF
Data input / output capacitance	DQM	CI/O	5	15	pF

Output load circuit



DC Characteristics I

Parameter	Symbol	Min	Max	Unit	Note
Input leakage current	I_{LI}	-1	1	uA	1
Output leakage current	I_{LO}	-1	1	uA	2
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output low voltage	V_{OL}	-	0.4	V	I_{OL} = 4mA

Note : 1.V_{IN} = 0 TO 3.6V, All other pins are not tested under V_{IN} = 0V.

2.D_{OUT} is disabled, V_{OUT} = 0 to 3.6.

DC Characteristics II

Parameter	Symbol	Test condition	Speed	Unit	Note
Operating Current	IDD1	Burst length=1, One bank active tRC≧tRC(min),I_{OL}=0mA	1,400	mA	1
Precharge standby current in power down mode	IDD2P	CKE≦V_{IL}(max), tCK=min	32	mA	
	IDD2PS	CKE≦V_{IL}(max), tCK=∞	32		
Precharge standby current in Non power down mode	IDD2N	CKE≧V_{IH}(min), /CS≧V_{IH}(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V	320	mA	
	IDD2NS	CKE≧V_{IH}(min), tCK=∞ Input signals are stable.	160		
Active standby current in power down mode	IDD3P	CKE≦V_{IL}(max), tCK=min	120	mA	
	IDD3PS	CKE≦V_{IL}(max), tCK=∞	120		
Active standby current in Non power down mode	IDD3N	CKE≧V_{IH}(min), /CS≧V_{IH}(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V	640	mA	
	IDD3NS	CKE≧V_{IH}(min), tCK=∞ Input signals are stable.	640		
Burst mode operating current	IDD4	t_{CK}≧t_{CK}(min),I_{OL}=0 mA All banks active	1,600	mA	1
Auto refresh current	IDD5	tRRC≧tRRC(min), All banks active	3,840	mA	2
Self refresh current	IDD6	CKE≦0.2V	32	mA	

Note: 1. IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open.

2. Min. of tRRC is shown at AC characteristics.

AC Characteristics

Parameter		Symbol	VDAAA1816		Unit	Note
			Min	Max		
System clock Cycle time	/CAS Latency = 3	tCK3	7.5	1000	ns	
	/CAS Latency = 2	tCK2	10			
Clock high pulse width		tCHW	2.5		ns	1
Clock low pulse width		tCLW	2.5		ns	1
Access time form clock	/CAS Latency = 3	tAC3		5.4	ns	2
	/CAS Latency = 2	tAC2		6		
/RAS cycle time	Operation	tRC	65		ns	
	Auto Refresh	tRRC	65			
/RAS to /CAS delay		tRCD	20		ns	
/RAS active time		tRAS	45	100K	ns	
/RAS precharge time		tRP	20		ns	
/RAS to /RAS bank active delay		tRRD	15		ns	
/CAS to /CAS delay		tCCD	1		CLK	
Write command to data – in delay		tWTL	0		CLK	
Data – in to precharge command		tDPL	2		CLK	
Data – in active command		tDAL	5		CLK	
DQM to data – out Hi-Z		tDQZ	2		CLK	
DQM to data – in mask		tDQM	0		CLK	
Data – out hold time		tOH	2.7		ns	
Data – input setup time		tDS	1.5		ns	1
Data – input hold time		tDH	0.8		ns	1
Address setup time		tAS	1.5		ns	1
Address hold time		tAH	0.8		ns	1
CKE setup time		tCKS	1.5		ns	1
CKE hold time		tCKH	0.8		ns	1
Command setup time		tCS	1.5		ns	1
Command hold time		tCH	0.8		ns	1
CLK to data output in low Z-time		tOLZ	1		ns	
MRS to new command		tMRD	2		CLK	
Power down exit time		tPDE	1		CLK	
Self refresh exit time		tSRE	1		CLK	3
Refresh time		tREF		64	ms	

Note : 1. Assume tR / tF (input rise and fall time) is 1 ns.

2. Access times to be measured with input signals of 1v / ns edge rate.

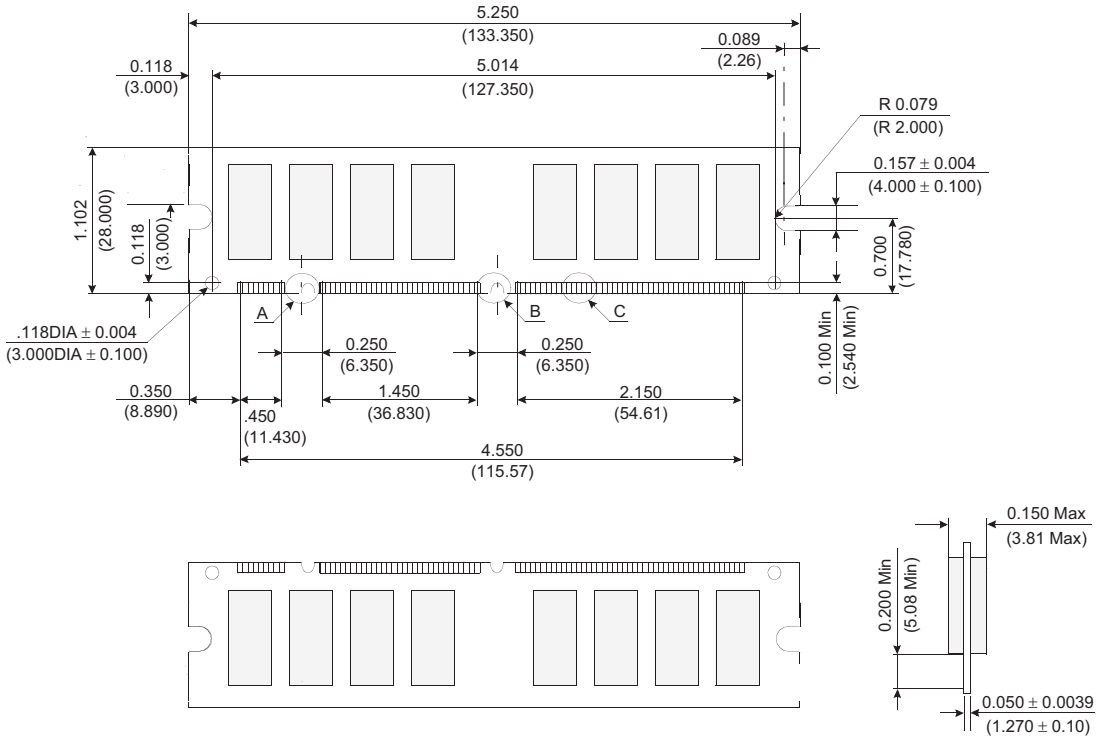
3.A new command can be given tRRC after self refresh exit.

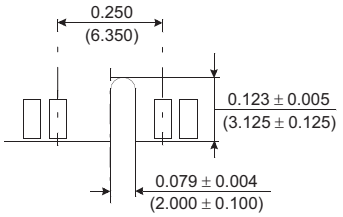
Command Truth-Table

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	X	OP code		
No Operation		H	X	H	X	X	X	X	X		
				L	H	H	H				
Bank Active		H	X	L	L	H	H	X	RA		V
Read		H	X	L	H	L	H	X	CA	L	V
Read with Auto Precharge										H	
Write		H	X	L	H	L	L	X	CA	L	V
Write with Auto Precharge										H	
Precharge All Bank		H	X	L	L	H	L	X	X	H	X
Precharge select Bank										L	V
Burst Stop		H	X	L	H	H	L	X	X		
DQM		H	X					V	X		
Auto Refresh		H	H	L	L	L	H	X	X		
Self Refresh	Entry	H	L	L	L	L	H	X	X		
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Precharge Power down	Entry	H	L	H	X	X	X	X	X		
				L	H	H	H				
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Clock Suspend	Entry	H	L	H	X	X	X	X	X		
				L	V	V	V				
	Exit	L	H	X				X	X		

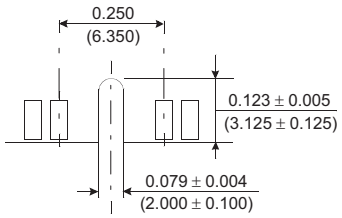
Package Information

Units : Inches (Millimeters)

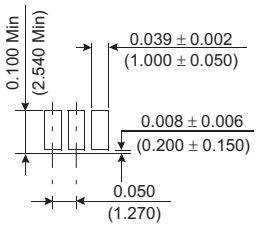




Detail A



Detail B



Detail C