SigmaDSP™ Multichannel 28-Bit Audio Processor

AD1940

FEATURES

- 16-channel digital audio processor
- Accepts sample rates up to 192 kHz
- 28-bit × 28-bit multiplier with full 56-bit accumulator
- Fully-programmable program RAM for custom program download
- Parameter RAM allows complete control of 1,024 parameters
- Control port features safeload for transparent parameter updates and complete mode and memory transfer control
- Target/slew RAM for click-free volume control and dynamic parameter updates
- Double precision mode for full 56-bit processing
- PLL for generating MCLK from 64 × f_S, 256 × f_S, 384 × f_S, or 512 × f_S clocks
- Hardware-accelerated DSP core
- 21 kB (6,144 words) data memory for up to 128 ms of audio delay at f_S = 48 kHz
- Flexible serial data port with I²S compatible, left-justified, and right-justified serial port modes
- 8- and 16-channel TDM input/output modes
- On-chip voltage regulator for compatibility with 3.3 V and 5 V systems
- Programmable low power mode
- Fast start-up and boot time from power on or reset
- 48-lead LQFP plastic package

APPLICATIONS

- Automotive sound systems
- Digital televisions
- Home theater systems (Dolby Digital/DTS postprocessor)
- Multichannel audio systems
- Mini-component stereos
- Multimedia audio
- Digital speaker crossover
- Musical instruments
- In-seat sound systems (aircrafts/motor coaches)

FUNCTIONAL BLOCK DIAGRAM

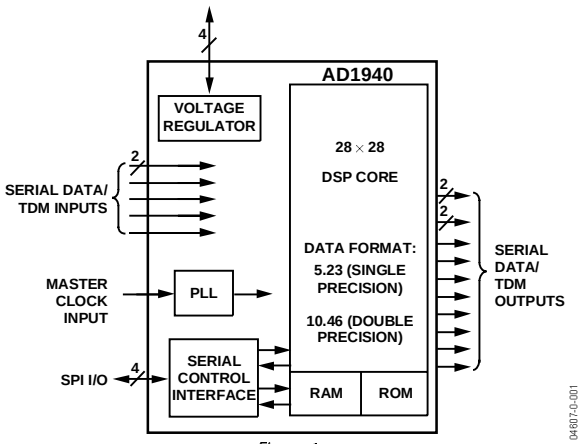

Figure 1.

GENERAL DESCRIPTION

The AD1940 is a complete 28-bit, single-chip, multichannel audio DSP for equalization, multiband dynamics processing, delay compensation, speaker compensation, and image enhancement. These algorithms can be used to compensate for the real-world limitations of speakers, amplifiers, and listening environments, resulting in a dramatic improvement of perceived audio quality.

The signal processing used in the AD1940 is comparable to that found in high end studio equipment. Most of the processing is done in full, 56-bit double-precision mode, resulting in very good low level signal performance and the absence of limit cycles or idle tones. The dynamics processor uses a sophisticated, multiple-breakpoint algorithm often found in high end broadcast compressors.

The AD1940 is a fully-programmable DSP. Easy to use software allows the user to graphically configure a custom signal processing flow using blocks such as biquad filters, dynamics processors, and surround sound processors. An extensive control port allows click-free parameter updates, along with readback capability from any point in the algorithm flow.

The AD1940's digital input and output ports allow a glueless connection to ADCs and DACs by multiple, 2-channel serial data streams or TDM data streams. When in TDM mode, the AD1940 can input 8 or 16 channels of serial data, and can output either 8 or 16 channels of serial data. The input and output port configurations can be individually set. The AD1940 is controlled via a 4-wire SPI port.

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

SPECIFICATIONS

Test conditions, unless otherwise noted.

Table 1.

Parameter	Conditions
Supply Voltage (VDD)	2.5 V
PLL Voltage (PLL_VDD)	2.5 V
Output Voltage (ODVDD)	5.0 V
INVDD Voltage	5.0 V
Ambient Temperature	25°C
Master Clock Input	3.072 MHz, 64 × f_S mode
Load Capacitance	50 pF
Load Current	±1 mA
Input Voltage, HI	2.4 V
Input Voltage, LO	0.8 V

DIGITAL I/O

Table 2. Digital I/O[1]

Parameter	Min	Max	Unit
Input Voltage, HI (V_{IH})	2.1		V
Input Voltage, LO (V_{IL})		0.8	V
Input Leakage (I_{IH})		10	µA
Input Leakage (I_{IL})		10	µA
High Level Output Voltage (V_{OH}) ODVDD = 4.5 V, I_{OH} = 1 mA	3.9		V
High Level Output Voltage (V_{OH}) ODVDD = 3.0 V, I_{OH} = 1 mA	2.6		V
Low Level Output Voltage (V_{OL}) ODVDD = 4.5 V, I_{OL} = 1 mA		0.4	V
Low Level Output Voltage (V_{OL}) ODVDD = 3.0 V, I_{OL} = 1 mA		0.3	V
Input Capacitance		5	pF

[1] All measurements across −40°C to 125°C (case) and across VDD = 2.25 V to 2.75 V.

POWER

Table 3.

Parameter	Min	Typ	Max[1]	Unit
Supplies				
Voltage	2.25	2.5	2.75	V
Digital Current		92	155[2]	mA
PLL Current		3.5	8	mA
Digital Current, Reset		4.5[3]	13[3]	mA
PLL Current, Reset		3	8.5	mA
Dissipation				
Operation, all supplies		238.8		mW
Reset, all supplies		10.8		mW

[1] Maximum specifications are measured across −40°C to 125°C (case) and across VDD = 2.25 V to 2.75 V.
[2] Measurement running a typical large program that writes to all 16 outputs with 0 dB digital sine waves applied to all eight inputs. Your program may differ.
[3] The digital reset current is specified for the given test conditions. This current scales with the input MCLK rate, so higher input clocks draw more current while in reset.

TEMPERATURE RANGE

Table 4.

Parameter	Min	Typ	Max	Unit
Functionality Guaranteed	−40		+105	°C Ambient
	−40		+125	°C Case

DIGITAL TIMING

Table 5 Digital Timing[1]

Parameter		Comments	Min	Max	Unit
t_{MP}	MCLK Period	512 f_S mode	36	244	ns
t_{MP}	MCLK Period	384 f_S mode	48	366	ns
t_{MP}	MCLK Period	256 f_S mode	73	488	ns
t_{MP}	MCLK Period	64 f_S mode	291	1953	ns
t_{MP}	MCLK Period	Bypass mode	12		ns
t_{MDC}	MCLK Duty Cycle	Bypass mode	40	60	%
t_{BIL}	BCLK_IN LO Pulse Width		4		ns
t_{BIH}	BCLK_IN HI Pulse Width		2		ns
t_{LIS}	LRCLK_IN Setup	To BCLK_IN rising	12		ns
t_{LIH}	LRCLK_IN Hold	From BCLK_IN rising	0		ns
t_{SIS}	SDATA_INx Setup	To BCLK_IN rising	3		ns
t_{SIH}	SDATA_INx Hold	From BCLK_IN rising	2		ns
t_{LOS}	LRCLK_OUTx Setup	Slave mode	2		ns
t_{LOH}	LRCLK_OUTx Hold	Slave mode	2		ns
t_{IS}	BCLK_OUTx Falling to LRCLK_OUTx Timing Skew			2	ns
t_{SODS}	SDATA_OUTx Delay	Slave mode, from BCLK_OUTx falling		17	ns
t_{SODM}	SDATA_OUTx Delay	Master mode, from BCLK_OUTx falling		17	ns
t_{CCPL}	CCLK Pulse Width LO		1 × INTMCLK (14)[2]		ns
t_{CCPH}	CCLK Pulse Width HI		1 × INTMCLK (14)[2]		ns
t_{CLS}	CLATCH Setup	To CCLK rising	0		ns
t_{CLH}	CLATCH Hold	From CCLK rising	2 × INTMCLK + 4 (32)[2]		ns
t_{CLPH}	CLATCH Pulse Width HI		2 × INTMCLK (28)[2]		ns
t_{CDS}	CDATA Setup	To CCLK rising	0		ns
t_{CDH}	CDATA Hold	From CCLK rising	2 × INTMCLK + 2 (30)[2]		ns
t_{COD}	COUT Delay	From CCLK rising		4 × INTMCLK +18 (74)[2]	ns
t_{RLPW}	RESETB LO Pulse Width		10		ns

[1] All timing specifications are given for the default (I²S) states of the serial input control port and the serial output control ports. See Table 32.
[2] These specifications are based on the internal master clock period in a specific application. In normal operation, the master clock runs at 1,536 × f_S, so the internal master clock at f_S = 48 kHz has a 14 ns period. The values in parentheses are the timing values for f_S = 48 kHz.

PLL

Table 6.

Parameter	Min	Typ	Max	Unit
Lock Time		3	20	ms

REGULATOR

Table 7.

Parameter	Min	Typ	Max	Unit
VSENSE Output Voltage	2.25	2.5	2.68	V

ABSOLUTE MAXIMUM RATINGS

Table 8.

Parameter	Min	Max	Unit
VDD to DGND	−0.3	+3.0	V
PLL_ VDD to PGND	−0.3	+3.0	V
OD VDD to DGND	−0.3	+6.0	V
INVDD to DGND	ODVDD	+6.0	V
Digital Inputs	DGND − 0.3	INVDD + 0.3	V
Maximum Junction Temperature		135	°C
Storage Temperature Range	−65	+150	°C
Soldering (10 sec)		300	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9. Package Characteristics

Parameter	Min	Typ	Max	Unit
θ_{JA} Thermal Resistance (Junction-to-Ambient)		72		°C/W
θ_{JC} Thermal Resistance (Junction-to-Case)		19.5		°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

DIGITAL TIMING DIAGRAMS

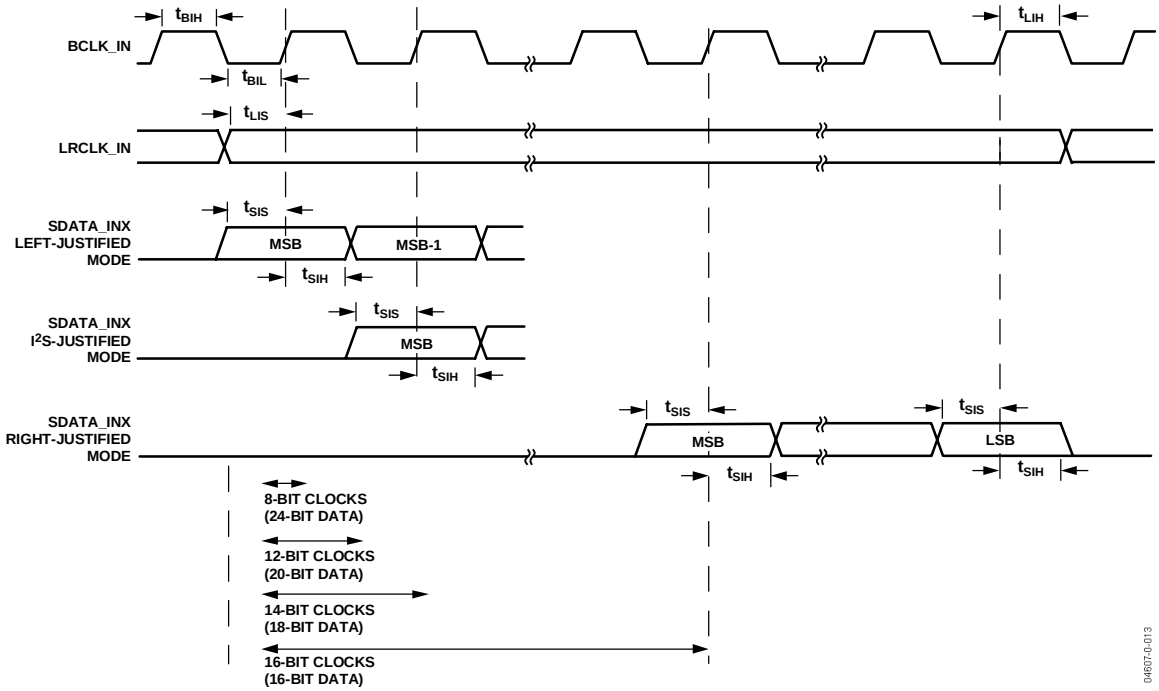


Figure 2. Serial Input Port Timing

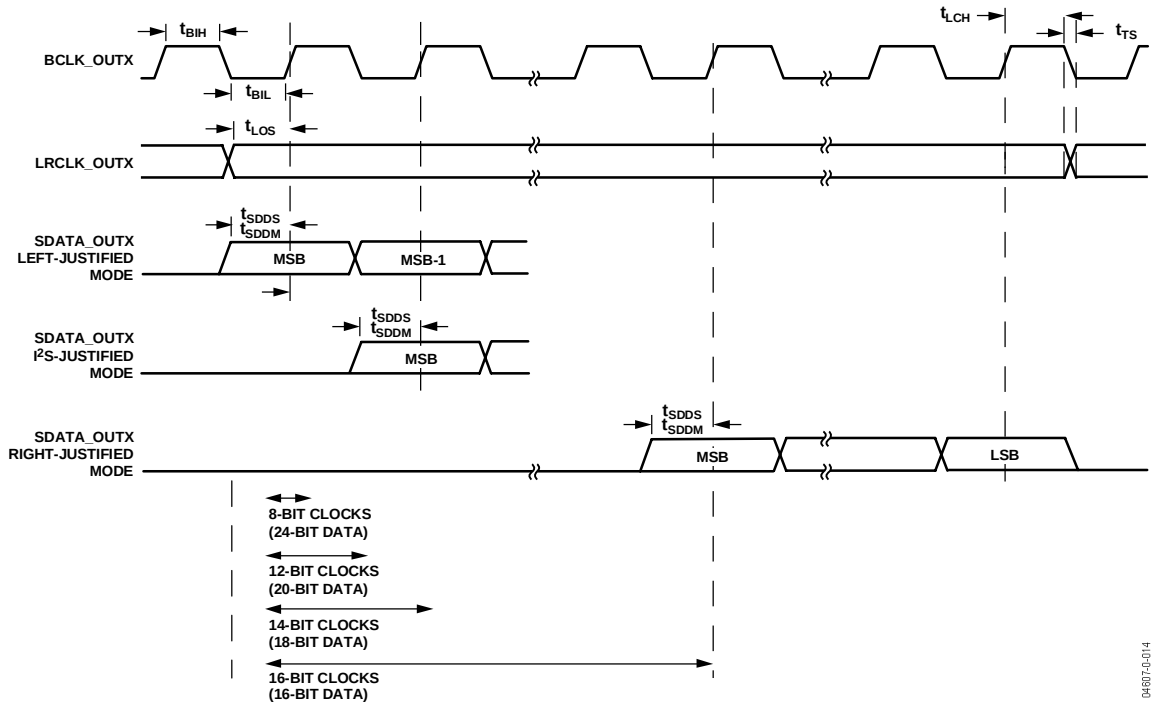


Figure 3. Serial Output Port Timing

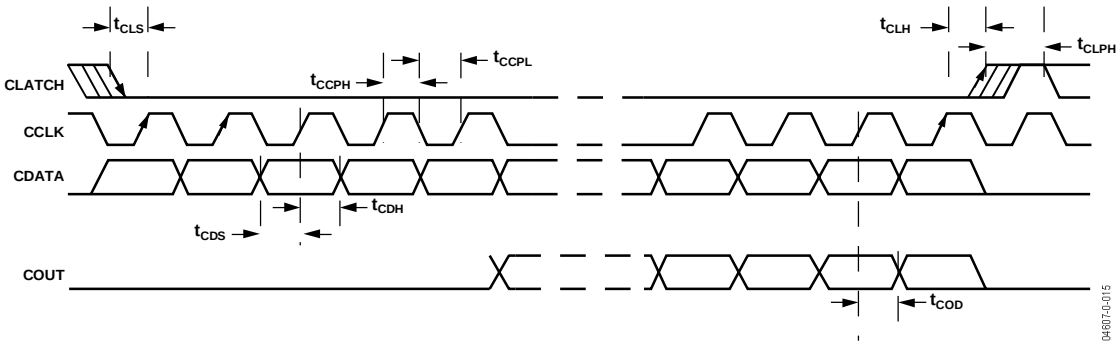


Figure 4. SPI Port Timing

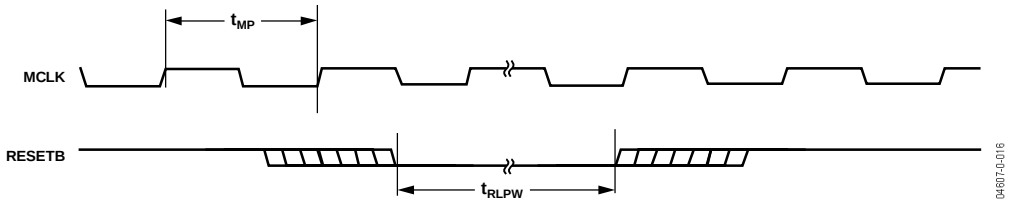


Figure 5. Master Clock and Reset Timing

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

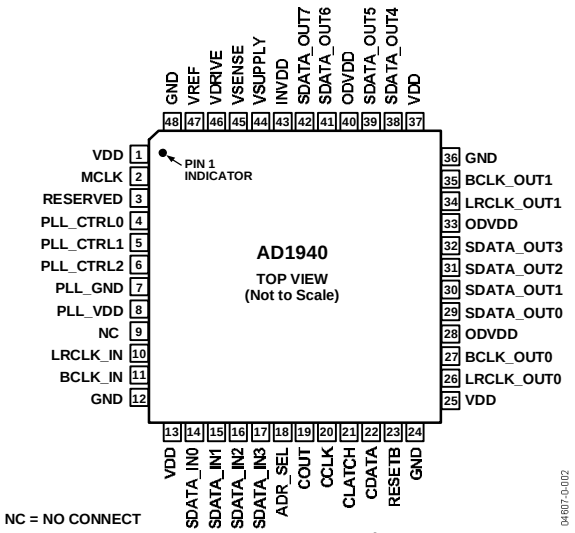


Figure6. 48-Lead LQFP Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	I/O	Mnemonic	Description
1, 25, 37		VDD	Core Power.
2	IN	MCLK	Master Clock Input.
3		RESERVED	This pin should be connected to ground.
4	IN	PLL_CTRL0	PLL Control 0.
5	IN	PLL_CTRL1	PLL Control 1.
6	IN	PLL_CTRL2	PLL Control 2.
7		PLL_GND	PLL Ground.
8		PLL_VDD	PLL Power.
9		NC	No Connect.
10	IN	LRCLK_IN	Left/Right Clock for Serial or TDM Data Inputs.
11	IN	BCLK_IN	Bit Clock for Serial or TDM Data Inputs.
12, 24, 36, 48		GND	Digital Ground.
13		VDD	Core Power.
14	IN	SDATA_IN0	Serial Data Input 0.
15	IN	SDATA_IN1	Serial Data Input 1.
16	IN	SDATA_IN2/TDM_IN1	Serial Data Input 2/TDM Input 1.
17	IN	SDATA_IN3/TDM_IN0	Serial Data Input 3/TDM Input 0.
18	IN	ADR_SEL	Control Port Address Select.
19	OUT	COUT	SPI Data Output.
20	IN	CCLK	SPI Clock.
21	IN	CLATCH	SPI Data Latch.
22	IN	CDATA	SPI Data Input.
23	IN	RESETB	Reset the AD1940
26	IN/OUT	LRCLK_OUT0	Left/Right Clock Output 0.
27	IN/OUT	BCLK_OUT0	Bit Clock Output 0.
28, 33, 40		ODVDD	Power Connection for Output Pins.
29	OUT	SDATA_OUT0/TDM_O0	Serial Data Output 0/TDM (16- or 8-Channel) Output 0.
30	OUT	SDATA_OUT1	Serial Data Output 1.

Pin No.	I/O	Mnemonic	Description
31	OUT	SDATA_OUT2	Serial Data Output 2.
32	OUT	SDATA_OUT3	Serial Data Output 3.
34	IN/OUT	LRCLK_OUT1	Left/Right Clock Output 1.
35	IN/OUT	BCLK_OUT1	Bit Clock Output 1.
38	OUT	SDATA_OUT4/TDM_O1	Serial Data Output 4/TDM (8-Channel) Output 1.
39	OUT	SDATA_OUT5	Serial Data Output 5.
41	OUT	SDATA_OUT6	Serial Data Output 6.
42	OUT	SDATA_OUT7/DCSOUT	Serial Data Output 7/Data Capture Output.
43		INVDD	Input Voltage Reference.
44	IN	VSUPPLY	Voltage Level Input to Regulator. Usually 3.3 V or 5 V.
45	IN	VSENSE	Digital Power Level. Should be tied to VDD.
46	OUT	VDRIVE	Drive for External PNP Transistor.
47	OUT	VREF	Reference Level for Voltage Regulator.

FEATURES

The core of the AD1940 is a 28-bit DSP (56-bit with double precision) optimized for audio processing.

The AD1940 contains a program RAM that is initialized from an internal program ROM on power-up. The program RAM can be loaded with a custom program after power-up. Signal processing parameters are stored in a 1024-location parameter RAM, which is initialized on power-up by an internal boot-ROM. New values are written to the parameter RAM using the control port. The values stored in the parameter RAM control individual signal processing blocks, such as IIR equalization filters, dynamics processors, audio delays, and mixer levels. A safeload feature allows parameters to be transparently updated without causing clicks on the output signals.

The target/slew RAM contains 64 locations and can be used as channel volume controls or for other parameter updates. These RAM locations take a target value for a given parameter and ramp the current parameter value to the new value using a specified time constant and one of a selection of linear or logarithmic curves.

The AD1940 has a sophisticated control port that supports complete read/write capability of all memory locations. Five control registers (core, RAM configuration, Serial Output 0 to 7, Serial Output 8 to 15, and serial input) are provided to offer complete control of the chip's configuration and serial modes. Handshaking is included for ease of memory uploads/downloads.

The AD1940 contains eight independent data capture circuits that can be programmed to tap the signal flow of the processor at any point in the DSP algorithm flow. Six of these captured signals can be accessed by reading from the data capture registers through the control port. The remaining two data capture registers can be used to send any internal captured signal to a stereo digital output signal on Pin SDATA_OUT7 for driving external DACs or digital analyzers.

The AD1940 has very flexible serial data input/output ports that allows for glueless interconnection to a variety of ADCs, DACs, general-purpose DSPs, S/PDIF receivers, and sample rate converters. The AD1940 can be configured in I²S, left-justified, right-justified, or TDM serial port compatible modes. It can support 16, 20, and 24 bits in all modes. The AD1940 accepts serial audio data in MSB first and twos complement format.

The AD1940 operates from a single 2.5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 48-lead LQFP package for operation over the −40°C to +105°C temperature range.

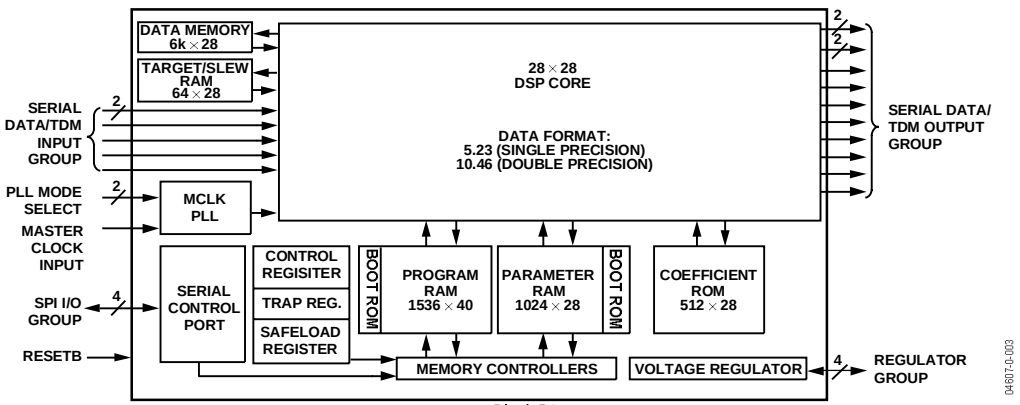


Figure 7. Block Diagram

PIN FUNCTIONS

Table 10 shows the AD1940's pin numbers, names, and functions. Input pins have a logic threshold compatible with TTL input levels and may be used in systems with 3.3 V or 5 V logic.

SDATA_IN0
SDATA_IN1
SDATA_IN2/TDM_IN1
SDATA_IN3/TDM_IN0

Serial Data/TDM Inputs. The serial format is selected by writing to Bits 2:0 of the serial input port control register. SDATA_IN2 and SDATA_IN3 are dual-function pins that can be set to a variety of standard 2-channel formats or to TDM mode. Two of these four pins (SDATA_IN2 and SDATA_IN3) can be used as TDM inputs in either dual-wire 8-channel mode or single-wire 16-channel mode (TDM_O0 only). In dual-wire 8-channel mode, Channels 0-7 will be input on SDATA_IN3 and Channels 8-15 on SDATA_IN2. In single-wire 16-channel mode, Channels 0-15 will be input on SDATA_IN2. See the Serial Data Input/Output Ports section for further explanation.

LRCLK_IN
BCLK_IN

Left/Right and Bit Clocks for Timing the Input Data. These input clocks are associated with the SDATA_IN0-3 signals. The input port is always in a slave configuration. These pins also function as frame sync and bit clock for the input TDM stream.

SDATA_OUT0/TDM_O0
SDATA_OUT1
SDATA_OUT2,
SDATA_OUT3
SDATA_OUT4/TDM_O1
SDATA_OUT5
SDATA_OUT6
SDATA_OUT7/DCSOUT

Serial Data/TDM/Data Capture Outputs. These pins are used for serial digital outputs. For non-TDM systems, these eight pins can output 16 channels of digital audio, using a variety of standard two-channel formats. They are grouped into two groups of four pins (0-3 and 4-7); each group can be independently set to any of the available serial modes, allowing the AD1940 to simultaneously communicate with two external devices with different serial formats. Two of these eight pins (SDATA_OUT0 and SDATA_OUT4) can be used as TDM outputs in either dual-wire 8-channel mode or single-wire 16-channel mode (TDM_OUT0 only). In dual-wire 8-channel mode, Channels 0-7 will be output on SDATA_OUT0 and Channels 8-15 on SDATA_OUT4. See the Serial Data Input/Output Ports section for further explanation. SDATA_OUT7 can also be used as a data capture output, as described in the Data Capture Registers section.

LRCLK_OUT0
BCLK_OUT0

Output Clocks. This clock pair is used for outputs SDATA_OUT0–3. In slave mode, these clocks are inputs to the AD1940. On power-up, these pins are set to slave mode to avoid conflicts with external master-mode devices.

LRCLK_OUT1
BCLK_OUT1

Output Clocks. This clock pair is used for outputs SDATA_OUT4–7. In slave mode, these clocks are inputs to the AD1940. On power-up, these pins are set to slave mode to avoid conflicts with external master-mode devices.

MCLK

Master Clock Input. The AD1940 uses a PLL to generate the appropriate internal clock for the DSP core. An in-depth description of using the PLL is found in the Setting Master Clock/PLL Mode section.

PLL_CTRL0
PLL_CTRL1
PLL_CTRL2

PLL Mode Control Pins. The functionality of these pins is described in the Setting Master Clock/PLL Mode section.

CDATA

Serial Data Input for the SPI Control Port.

COUT

Serial Data Output for the SPI Port. This is used for reading back registers and memory locations. It is three-stated when an SPI read is not active.

CCLK

SPI Bit Clock. This clock may either run continuously or be gated off in between SPI transactions.

CLATCH

SPI Latch Signal. This must go low at the beginning of an SPI transaction and high at the end of a transaction. Each SPI transaction may take a different number of CCLKs to complete, depending on the address and read/write bit that are sent at the beginning of the SPI transaction.

ADR_SEL

Address Select. This pin selects the address for the AD1940's communication with the control port. This allows two AD1940s to be used with a single CLATCH signal.

RESETB

Active-Low Reset Signal. After RESETB goes high, the AD1940 goes through an initialization sequence where the program and parameter RAMs are initialized with the contents of the on-board boot ROMs. All registers are set to 0, and the data RAMs are also set to 0. The initialization is complete after 8,192 internal MCLK cycles (referenced to the rising edge of RESETB), which corresponds to 1,366 external MCLK cycles if the part is in 256 × f_S mode. New values should not be written to the control port until the initialization is complete.

VREF

Voltage Reference for Regulator. This pin is driven by an internal 1.15 V reference voltage.

VDRIVE

Drive for External Transistor. The base of the voltage regulator's external PNP transistor is driven from this pin.

VSENSE

Digital power level. The voltage level on the VDD pins is sensed on VSENSE. VSENSE should be tied to VDD.

VSUPPLY

Main Supply Voltage Level. This pin is tied to the board's main voltage supply. This is usually 3.3 V or 5 V.

VDD (4)

Digital VDD for Core. 2.5 V nominal.

GND (4)

Digital Ground.

PLL_VDD

Supply for AD1940 PLL. 2.5 V nominal.

PLL_GND

PLL Ground.

ODVDD (3)

VDD for All Digital Outputs. The high levels of the digital output signals are set on this pin. The voltage can range from 2.5 V to 5.0 V.

INVDD

Peak Input Voltage Level. The highest voltage level that the input pins will see should be connected to INVDD. This is to protect the chip inputs from voltage overstress. The voltage on this pin must always be at or above the level of ODVDD.

SIGNAL PROCESSING

OVERVIEW

The AD1940 is designed to provide all signal processing functions commonly used in stereo or multichannel playback systems. The signal processing flow is set by using the ADI-supplied software, which allows graphical entry and real-time control of all signal processing functions.

Many of the signal processing functions are coded using full, 56-bit double-precision arithmetic. The input and output word lengths are 24 bits. Four extra headroom bits are used in the processor to allow internal gains up to 24 dB without clipping. Additional gains can be achieved by initially scaling down the input signal in the signal flow.

The signal processing blocks can be arranged in a custom program that can be loaded to the AD1940's RAM. The available signal processing blocks are explained in the following sections.

NUMERIC FORMATS

It is common in DSP systems to use a standardized method of specifying numeric formats. Fractional number systems are specified by an A.B format, where A is the number of bits to the left of the decimal point and B is the number of bits to the right of the decimal point.

The AD1940 uses the same numeric format for both the coefficient values (stored in the parameter RAM) and the signal data values. The format is as follows:

Numerical Format: 5.23

Range: –16.0 to (+16.0 – 1 LSB)

Examples:
10000000000000000000000000000 = –16.0
11100000000000000000000000000 = –4.0
11111000000000000000000000000 = –1.0
11111110000000000000000000000 = –0.25
11111111111111111111111111111 = (1 LSB below 0.0)
00000000000000000000000000000 = 0.0
00000010000000000000000000000 = 0.25
00001000000000000000000000000 = 1.0
00100000000000000000000000000 = 4.0
01111111111111111111111111111 = (16.0 – 1 LSB).

The serial port accepts up to 24 bits on the input and is sign-extended to the full 28 bits of the core. This allows internal gains of up to 24 dB without encountering internal clipping.

A digital clipper circuit is used between the output of the DSP core and the serial output ports (see Figure 8). This clips the top four bits of the signal to produce a 24-bit output with a range of 1.0 (minus 1 LSB) to –1.0.

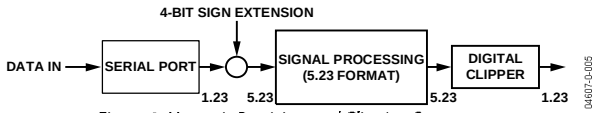


Figure 8. Numeric Precision and Clipping Structure

PROGRAMMING

On power-up, the AD1940's default program passes the unprocessed input signals to the outputs but the outputs come up muted by default (see Power-Up Sequence section). There are 1,536 instruction cycles per audio sample, resulting in an internal clock rate of 73.728 MHz (for f_S = 48 kHz). This DSP runs in a stream-oriented manner, meaning all 1,536 instructions are executed each sample period. The AD1940 may also be set up to accept double or quad-speed inputs by reducing the number of instructions/sample, which can be set in the core control register.

The part can be programmed easily using graphical tools provided by Analog Devices. No knowledge of writing DSP code is needed to program this part. The user can simply connect graphical blocks such as biquad filters, dynamics processors, mixers, and delays in a signal flow schematic, compile the design, and load the program and parameter files into the AD1940's Program RAM through the control port. Signal processing blocks available in the provided libraries include

- Single- and double-precision biquad filters
- Mono and multichannel dynamics processors
- Mixers and splitters
- Tone and noise generators
- First-order filters
- Fixed and variable gain
- RMS look-up tables
- Loudness
- Delay
- Stereo enhancement (Phat Stereo™)
- Interpolators and Decimators

More blocks are always in development. Analog Devices also provides proprietary and third-party algorithms for applications such as matrix decoding, bass enhancement, and surround virtualizers. Please contact ADI for information about licensing these algorithms.

CONTROL PORT

OVERVIEW

The AD1940 has many different control options that can be set through an SPI interface. Most signal processing parameters are controlled by writing new values to the parameter RAM using the control port. Other functions, such as mute and input/output mode control, are programmed by writing to the control registers.

The control port is capable of full read/write operation for all of the memories and registers. All addresses may be accessed in both a single-address mode or a burst mode. A control word consists of the chip address, the register/RAM subaddress, and the data to be written. The data can be variable in its byte width.

The first byte of a control word (Byte 0) contains the 7-bit chip address plus the R/W bit. The next two bytes (Bytes 1 and 2) together form the subaddress of the memory or register location within the AD1940. This subaddress needs to be two bytes because the memories within the AD1940 are directly addressable, and their sizes exceed the range of single-byte addressing. All subsequent bytes (Bytes 3, 4, etc.) contain the data, such as control port data or program or parameter data.

The AD1940 has several mechanisms for updating signal processing parameters in real time without causing pops or clicks. In cases where large blocks of data need to be downloaded, the output of the DSP core can be halted (using Bit 9 of the core control register), new data loaded, and then restarted. This is typically done during the booting sequence at start-up or when loading a new program into RAM. In cases where only a few parameters need to be changed, they can be loaded without halting the program. To avoid unwanted side effects while loading parameters on the fly, the SigmaDSP provides the safeload registers. The safeload registers can be used to buffer a full set of parameters (e.g. the five coefficients of a biquad) and then transfer these parameters into the active program within one audio frame. The safeload mode uses internal logic to prevent contention between the DSP core and the control port.

The SPI port uses a 4-wire interface, consisting of CLATCH, CCLK, CDATA, and COUT signals. The CLATCH signal goes low at the beginning of a transaction and high at the end of a transaction. The CCLK signal latches CDATA on a low-to-high transition. COUT data is shifted out of the AD1940 on the falling edge of CCLK and should be clocked into the receiving device, such as a microcontroller, on CCLK's rising edge. The CDATA signal carries the serial input data, and the COUT signal is the serial output data. The COUT signal remains three-stated until a read operation is requested. This allows other SPI-compatible peripherals to share the same readback line. All SPI transactions follow the same basic format, shown in Table 11. A timing diagram is shown in Figure 4. All data written should be MSB-first.

Table 11. Generic SPI Word Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4, etc.
chip_adr [6:0], R/$\overline{W}$	0000, adr[11:8]	adr[7:0]	data	data

Chip Address R/$\overline{W}$

The first byte of an SPI transaction includes the 7-bit chip address and a R/$\overline{W}$ bit. The chip address is set by the ADR_SEL pin. This allows two AD1940s to share a CLATCH signal, yet still operate independently. When ADR_SEL is low, the chip address is 0000000; when it is high, the address is 0000001. The LSB of this first byte determines whether the SPI transaction is a read (Logic Level 1) or a write (Logic Level 0).

RAM/Register Address

The 12-bit RAM/register address word is decoded into a location in one of the memories or registers.

Data Bytes

The number of data bytes varies according to the register or memory being accessed. In burst write mode, an initial address is given followed by a continuous sequence of data for consecutive memory/register locations. The detailed data format diagram for continuous-mode operation is given in the Control Port Read/Write Data Formats section.

A sample timing diagram for a single SPI write operation to the parameter RAM is shown in Figure 9. A sample timing diagram of a single SPI read operation is shown in Figure 10. The COUT pin goes from three-state to driven at the beginning of Byte 3. In this example, Bytes 0 to 2 contain the addresses and R/W bit, and subsequent bytes carry the data. The exact formats for specific types of writes are shown in Table 21 to Table 30.

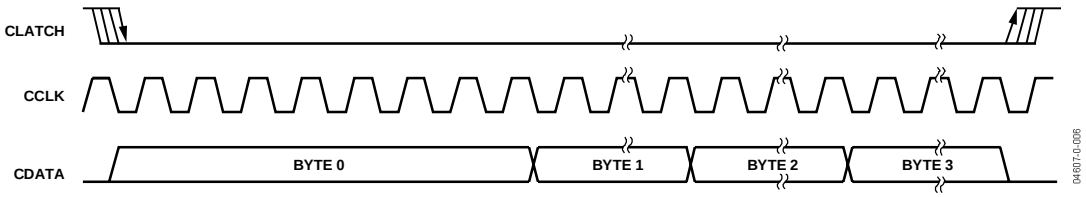


Figure 9. Sample of SPI WRITE format (Single-Write Mode)

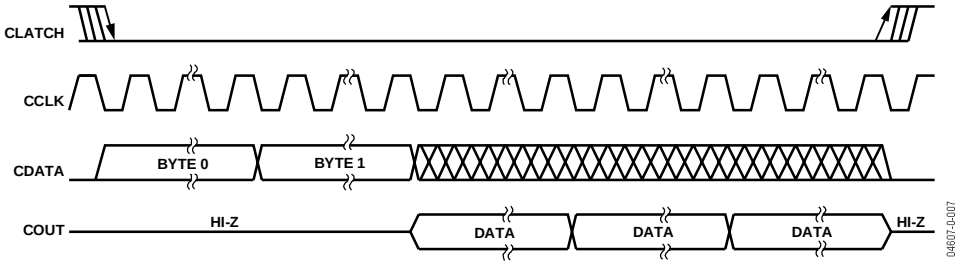


Figure 10. Sample of SPI READ Format (Single-Read Mode)

RAMS AND REGISTERS

Table 12. Control Port Addresses

SPI Address	Register Name	Read/Write Word Length
0–1023 (0x0000–0x03FF)	Parameter RAM	Write: 4 Bytes, Read: 4 Bytes
1024–2559 (0x0400–0x09FF)	Program RAM	Write: 5 Bytes, Read: 5 Bytes
2560–2623 (0x0A00–0x0A3F)	Target/Slew RAM	Write: 5 Bytes, Read: N/A
2624–2628 (0x0A40–0x0A44)	Parameter RAM Data Safeload Registers 0–4	Write: 5 Bytes, Read: N/A
2629–2633 (0x0A45–0x0A49)	Parameter RAM Indirect Address Safeload Registers 0-4	Write: 2 Bytes, Read: N/A
2634–2639 (0x0A4A–0x0A4F)	Data Capture Registers 0–5 (Control Port Readback)	Write: 2 Bytes, Read: 3 Bytes
2640–2641 (0x0A50–0x0A51)	Data Capture Registers (Digital Output)	Write: 2 Bytes, Read: N/A
2642 (0x0A52)	DSP Core Control Register	Write: 2 Bytes, Read: 2 Bytes
2643 (0x0A53)	RAM Configuration Register	Write: 1 Byte, Read: 1 Byte
2644 (0x0A54)	Serial Output Control Register 1 (Channels 0–7)	Write: 2 Bytes, Read: 2 Bytes
2645 (0x0A55)	Serial Output Control Register 2 (Channels 8–15)	Write: 2 Bytes, Read: 2 Bytes
2646 (0x0A56)	Serial Input Control Register	Write: 1 Byte, Read: 1 Byte

Table 13. RAM Read/Write Modes

Memory	Size	SPI Address Range	Read	Write	Burst Mode Available?	Write Modes
Parameter RAM	1024 × 28	0–1023 (0x0000–0x03FF)	Yes	Yes	Yes	Direct Write[1] Safeload Write
Program RAM	1536 × 40	1024–2559 (0x0400–0x09FF)	Yes	Yes	Yes	Direct Write[1]
Target/Slew RAM	64 × 34	2560–2623 (0x0A00–0x0A3F)	No	Yes (via Safeload)	Yes[2]	Safeload Write

[1] DSP core should be shut down first to avoid clicks/pops.
[2] The target/slew RAMs need to be written through the safeload registers. Safeload writes may be done in either single-write or burst-mode.

CONTROL PORT ADDRESSING

Table 12 shows the addressing of the AD1940's RAM and register spaces. The address space encompasses a set of registers and three RAMs: one each for holding signal processing parameters, holding the program instructions, and ramping parameter values. The program and parameter RAMs are initialized on power-up from on-board boot ROMs.

Table 13 shows the sizes and available writing modes of the parameter, program, and target/slew RAMs.

PARAMETER RAM CONTENTS

The parameter RAM is 28 bits wide and occupies Addresses 0 to 1023. The parameter RAM is initialized to all 0s on power-up. The data format of the parameter RAM is twos complement 5.23. This means that the coefficients may range from +16.0 (minus 1 LSB) to –16.0, with 1.0 represented by the binary word 0000100000000000000000000000.

Options for Parameter Updates

The parameter RAM can be written and read using one of the two following methods.

1. **Direct Read/Write.** This method allows direct access to the program and parameter RAMs. This mode of operation is normally used during a complete new load of the RAMs, using burst-mode addressing. The clear registers bit in the core control register should be set to 0 using this mode to avoid any clicks or pops in the outputs. Note that it is also possible to use this mode during live program execution, but since there is no handshaking between the core and the control port, the parameter RAM will be unavailable to the DSP core during control writes, resulting in clicks and pops in the audio stream.

2. **Safeload Writes.** Up to five safeload registers can be loaded with address/data intended for the parameter RAM. The data is then transferred to the requested address when the RAM is not busy. This method can be used for dynamic updates while live program material is playing through the AD1940/AD1941. For example, a complete update of one biquad section can occur in one audio frame, while the RAM is not busy. This method is not available for writing to the program RAM or control registers.

The following section discusses these two options in more detail.

RECOMMENDED PROGRAM/PARAMETER LOADING PROCEDURES

When writing large amounts of data to the program or parameter RAM in direct write mode, the processor core should be disabled to prevent unpleasant noises from appearing at the audio output. The AD1940 contains several mechanisms for disabling the core.

If the loaded program does NOT use the target/slew RAM as the main system volume control (for example, the default power-up program)

1. Assert Bit 9 (LOW to assert—default setting) and Bit 6 (HIGH to assert) of the core control register. This zeroes the accumulators, the serial output registers, and the serial input registers.
2. Fill the program RAM using burst mode writes.
3. Fill the parameter RAM using burst mode writes.
4. Assert Bit 7 of the core control register to initiate a data-memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
5. Deassert Bit 9 and Bit 6 of the core control register to allow the core to begin normal operation

If the loaded program does use the target/slew RAM as the main system volume control:

1. Assert Bit 12 of the core control register. This begins a volume ramp-down, with a time constant determined by the upper bits of the target RAM. Wait for this ramp-down to complete (the user may poll Bit 13 of the core control register, or simply wait for a given amount of time).
2. Assert Bit 9 (LOW to assert) and Bit 6 (HIGH to assert) of the core control register. This zeroes the accumulators, the serial output registers, and the serial input registers.
3. Fill the program RAM using burst-mode writes.
4. Fill the parameter RAM using burst-mode writes.
5. Assert Bit 7 of the core control register to initiate a data-memory clear sequence. Wait at least 100 µs for this sequence to complete. This bit is automatically cleared after the operation is complete.
6. Deassert Bit 9 and Bit 6 of the core control register.
7. If the newly loaded program also uses the target/slew RAM, deassert Bit 12 of the core control register to begin a volume ramp-up procedure.

TARGET/SLEW RAM

The target/slew RAM is a bank of 64 RAM locations, each of which can each be set to autoramp from one value to a desired final value in one of four modes.

Summary

The target/slew RAM is used by the DSP when a program is loaded into the program RAM that uses one or more locations in the slew RAM to access internal coefficient data. Typically, these coefficients are used for volume controls or smooth cross-fading effects, but may be used to update any value in the parameter RAM. Each of the 64 locations in the slew RAM are linked to corresponding locations in the target RAM. When a new value is written to the target RAM using the control port, the corresponding slew RAM location begins to ramp toward the target. The value is updated once per audio frame (LRCLK period).

The target RAM is 34 bits wide. The lower 28 bits contain the target data in 5.23 format for the linear and exponential (constant dB and RC-type) ramp types. For constant time ramping, the lower 28 bits contain 16 bits in 2.14 format and 12 bits to set the current step. The upper six bits are used to determine the type and speed of the ramp envelope in all modes. The format of the data write for linear and exponential formats is shown in Table 14. Table 15 shows the data write format for the constant time ramping.

Data can only be written to the target/slew RAM using the safeload registers as described in the Safeload Registers section. A mute slew RAM bit is included in the core control register to simultaneously set all the slew RAM target values to 0. This is useful for implementing a global multichannel mute. When this bit is deasserted, all slew RAM values will return to their original pre-muted states.

Table 14. Linear, Constant dB, and RC-type Ramp Data Write

Byte 0	Byte 1	Bytes 2–4
000000, curve_type[1:0]	time_const[3:0], data[27:24]	data[23:0]

Table 15. Constant Time Ramp Data Write

Byte 0	Byte 1	Bytes 2–4
000000, curve_type[1:0]	update_step[0], #_of_steps[2:0], data[15:12]	data[11:0], reserved[11:0]

The four ramping curve types are

1. Linear—Value slews to target using a fixed step size.
2. Constant dB—Value slews to target using the current value to calculate the step size. The resulting curve has a constant rise and decay when measured in dB.
3. RC-type—Value slews to target using the difference between target and current values to calculate the step size, producing a simple RC type curve for rising and falling.
4. Constant Time—Value slews to the target in a fixed number of steps in a linear fashion. The control port mute has no affect on this type.

Table 16 Target/Slew RAM Ramp Type Settings

Setting	Ramp Type
00	Linear
01	Constant dB
10	RC-Type
11	Constant Time

The following sections detail how the control port writes to the target/slew RAM to control the time constant and ramp type parameters.

Ramp Types 1–3: Linear, Constant dB, RC-type (34-Bit Write)

The target word for the first three ramp types is broken up into three parts. The 34-bit command is written with six leading 0s to extend the data write to five bytes. The parts of the target RAM write are described below.

- Ramp Type (2 bits)
- Time Constant (4 bits)
  0000 = Fastest
  1111 = Slowest
- Data (28 Bits): 5.23 Format

Ramp Type 4—Constant Time (34-Bit Write)

The target word for the constant time ramp type is written in five parts, with the 34-bit command again written with six leading zeros to extend the data write to five bytes. The parts of the constant time target RAM write are described below.

- Ramp Type (2 bits).
- Update Step (1 bit). Set to 1 when new target is loaded to trigger step value update. Value is automatically reset after the step value is updated.
- Number of Steps (3 bits). The number of steps that it takes to slew to the target value is set by these three bits, with the number of steps equal to $2^{3\text{-bit setting}+6}$.
  000 = 64
  001 = 128
  010 = 256
  011 = 512
  100 = 1024
  101 = 2048
  110 = 4096
  111 = 8196
- Data (16 bits). 2.14 format.
- Reserved (12 bits). When writing to the RAM, these bits should all be set to 0.

Target and Slew RAM Initialization

On reset, the target/slew RAM initializes to preset values. The target RAM initializes to a linear ramp type with a time constant of 5 and the data set to 1.0. The slew RAM initializes to a value of 1.0. These defaults give a full-scale (1.0 to 0.0) ramp time of 21.3 ms.

Linear Update Math

Linear math is the addition or subtraction of a constant value (step). The equation to describe this step size is

$$step = \frac{2^{13}}{\frac{10^{2\times(tconst-5)}}{20}}$$

The result of the equation is normalized to 5.23 data format. This gives a time constant range from 6.75 ms to 213.4 ms. (–60 dB relative to 0 dB full scale). An example of this kind of update is shown in Figure 11. All slew RAM figure examples, except the second constant time plot, show a ramp from –80 dB to 0 dB (full scale). All figures except the constant time plots (Figure 14 and Figure 15) use a time constant of 0x7 (0x0 being the fastest and 0xF being the slowest).

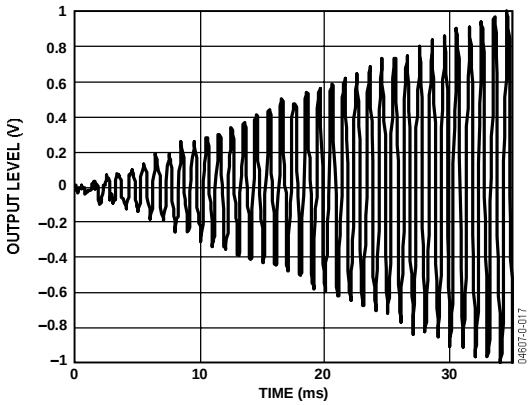


Figure 11. Slew RAM—Linear Update Plot

Constant dB and RC-type (Exponential) Update Math

Exponential math is accomplished by shifts and adds with a range from 6.1 ms to 1.27 s (–60 dB relative to 0 dB full scale). When the ramp type is set to 01 (constant dB), each step size is set to the current value in the slew data. When the ramp type bits are set to 10 (RC type), the step sizes are equal to the difference between the values in the target RAM and slew RAM. Figure 12 and Figure 13 show examples of this type of target/slew RAM ramping. A decaying plot of both the constant dB and RC-type ramps would be a mirror image of what is shown in Figure 12.

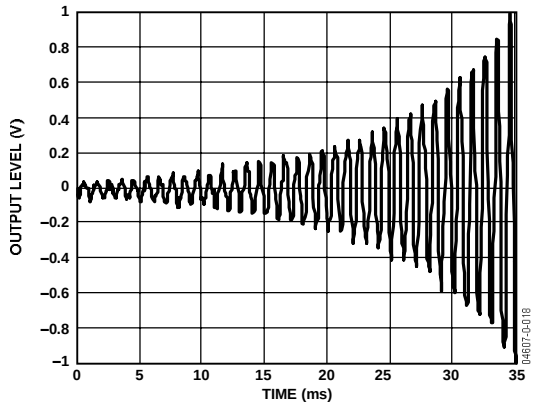


Figure 12. Slew RAM—Constant dB Update Plot

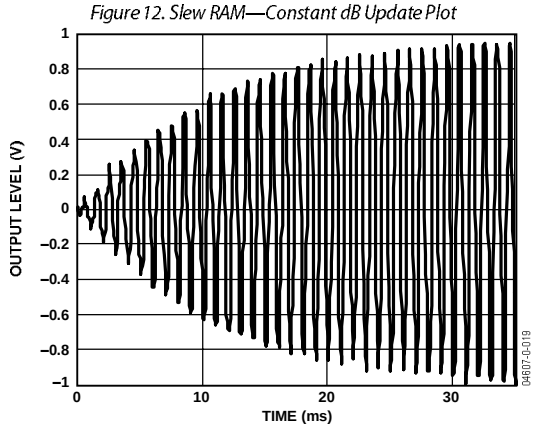


Figure 13. Slew RAM—RC-Type Update Plot

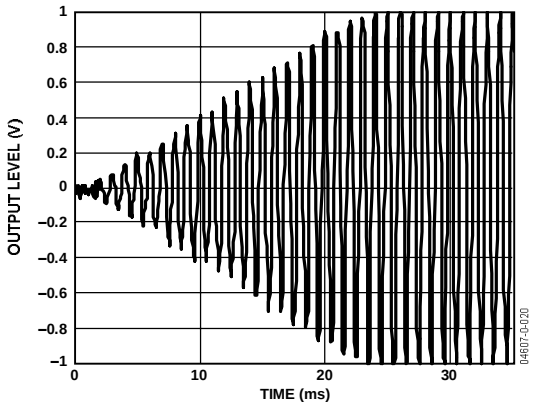


Figure 14 Slew RAM—Constant Time Update Plot, Full Scale

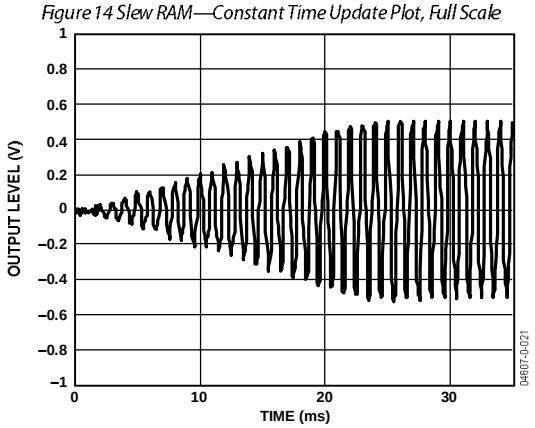


Figure 15 Slew RAM—Constant Time Update Plot, Half Scale

Constant Time Update Math

Constant time math is accomplished by adding a step value that is calculated after each new target is loaded. The equation for this step size is

$$Step = (Target\ Data - Slew\ Data)/(Number\ of\ Steps)$$

Figure 14 shows a plot of the target/slew RAM operating in constant time mode. For this example, 128 steps are used to reach the target value. This type of ramping will take a fixed amount of time for a given number of steps, regardless of the difference in the initial state and the target value. Figure 15 shows a plot of a constant time ramp from −80 dB to −6 dB (half scale) using 128 steps. You can see that the ramp takes the same amount of time as the previous ramp from −80 dB to 0 dB.

SAFELOAD REGISTERS

Many applications require real-time control of signal processing parameters, such as filter coefficients, mixer gains, multichannel virtualizing parameters, or dynamics processing curves. To prevent instability from occurring, all of the parameters of a biquad filter must be updated at the same time. Otherwise, the filter could execute for one or two audio frames with a mix of old and new coefficients. This mix could cause temporary instability, leading to transients that could take a long time to decay. To eliminate this problem, the AD1940 loads a set of 10 registers in the control port (five for 28-bit parameters, and another five for indirectly addressing the target/slew RAMs) with the desired parameter or target/slew RAM address and data. Five registers are used because a biquad filter uses five coefficients, and it is desirable to be able to do a complete biquad update in one transaction. The safeload registers can be used to update either the parameter RAM or target/slew RAM values. Once these registers are loaded, the appropriate initiate safe transfer bit (there are separate bits for parameter and target/slew loads) in the core control register should be set to initiate the loading into RAM. Program lengths should be limited to 1,531 cycles (1,536 − 5) to ensure that the SigmaDSP is able to perform the safeloads. It can be guaranteed that the safeload will have occurred within one LRCLK period (21 µs at f_S = 48 kHz) of the initiate safe transfer bit being set.

The safeload logic automatically sends only those safeload registers that have been written to since the last safeload operation. For example, if only two parameters are to be sent, only two of the five safeload registers must be written to. When the initiate safe transfer bit (in the core control register) is asserted, only those two registers are sent; the other three registers are not sent to the RAM and can still hold old or invalid data.

Table 17. Data Capture Control Registers (2634–2641)

Register Bits	Function
12:2	11-Bit Program Counter Address
1:0	Register Select 00 = Mult_X_input 01 = Mult_Y_input 10 = MAC_output 11 = Accum_fback

DATA CAPTURE REGISTERS

The AD1940's data capture feature allows the data at any node in the signal processing flow to be sent to one of six control port-readable registers or to a serial output pin. This can be used to monitor and display information about internal signal levels or compressor/limiter activity.

The AD1940 contains six independent control port-readable data capture registers, and two digital output capture registers. The digital output registers are output on SDATA_OUT7 when the data capture serial out enable bit (Bit 14) is set in Serial Output Control Register 2. These registers are useful when debugging the signal processing flow.

For each of the data capture registers, a capture count and a register select must be set. The capture count is a number between 0 and 1,535 that corresponds to the program step number where the capture will occur. The register select field programs one of four registers in the DSP core that will be transferred to the data capture register when the program counter equals the capture count. The register select field selections are shown in Table 18.

Table 18. Data Capture Output Register Select

Setting	Register
00	Multiplier X Input (Mult_X_input)
01	Multiplier Y Input (Mult_Y_input)
10	Multiplier-Accumulator Output (MAC_out)
11	Accumulator Feedback (Accum_fback)

The capture count and register select bits are set by writing to one of the eight data capture registers at register addresses

2634: Control Port Data Capture Setup Register 0
2635: Control Port Data Capture Setup Register 1
2636: Control Port Data Capture Setup Register 2
2637: Control Port Data Capture Setup Register 3
2638: Control Port Data Capture Setup Register 4
2639: Control Port Data Capture Setup Register 5
2640: Digital Out Data Capture Setup Register 0
2641: Digital Out Data Capture Setup Register 1

The captured data is in 5.19 twos complement data format for all eight register select fields. The four LSBs are truncated from the internal 5.23 data-word.

The data that must be written to set up the data capture is a concatenation of the 11-bit program count index with the 2-bit register select field. The capture count and register select values that correspond to the desired point to be monitored in the signal processing flow can be found in a file output from the program compiler. The capture registers can be accessed by reading from locations 2634 to 2639 (for control port capture registers). The format for reading and writing to the data capture registers can be seen in Table 27 and Table 28.

Table 19. DSP Core Control Register (2642)

Register Bits	Function
15:14	Reserved
13	Slew RAM Muted (Read Only)
12	Mute Slew RAM, All Locations
11	Reserved, Set to 0
10	Use Serial Out LRCLK for Output Latch
9	Clear Internal Registers to All 0s, Active Low
8	Force Multiplier to 0
7	Inititalize Data Memory with 0s
6	Mute Serial Input Port
5	Initiate Safe Transfer to Target RAM
4	Initiate Safe Transfer to Parameter RAM
3:2	Input Serial Port to Sequencer Sync 00 = LRCLK 01 = LRCLK/2 10 = LRCLK/4 11 = LRCLK/8
1:0	Program Length 00 = 1536 01 = 768 10 = 384 11 = 192

DSP CORE CONTROL REGISTER

The controls in this register set the operation of the AD1940's DSP core. Bits 6 to 9 can be set to initiate a shutdown of the core. The output is muted when this is performed, so it is best to first assert the mute slew RAM bit (if slew RAM locations are used as volume controls in the program) to avoid a click or pop when shutdown is asserted.

Slew RAM Muted (Bit 13)

This bit is set to 1 when the slew RAM mute operation has been completed. This bit is read-only and is automatically cleared by reading.

Mute Slew RAM, All Locations (Bit 12)

Setting this bit to 1 initiates a mute of all 64 slew RAM locations. When reset to 0, all RAM locations return to their previous state. This bit is only functional if slew RAM locations are used in the custom program design. Keep in mind that the AD1940's default program does not use any slew RAM volume controls, so this bit has no effect in that case. The mute operation is identical to writing all 0s to the data portion of the target RAM, and therefore the time constant and linear/exponential curve selection is determined by the bits that have

been previously written to the high bits of the target RAM.

Use Serial Out LRCLK for Output Latch (Bit 10)

Normally, data is transferred from the DSP core to the serial output registers at the end of each program cycle. In some cases (e.g., when output sample rate is set to some multiple of input sampling rate), it is desirable to transfer the internal core data multiple times during a single input audio sample period. Setting this bit to 1 allows the output LRCLK signal to control this data transfer rather than the internal end-of-sequence signal. Operation in this mode may require custom assembly-language coding in the ADI graphical tools.

Clear Registers to All Zeros (Bit 9)

Setting this bit to 0 sets the contents of the accumulators and serial output registers to 0. Like the other register bits, this one powers up to 0. This means the AD1940 powers up in clear mode and will not pass a signal until a 1 is written to this bit. This is intended to prevent noises from inadvertently occurring during the power-up sequence.

Force Multiplier to Zero (Bit 8)

When this bit is set to 1, the input to the DSP multiplier is set to 0, which results in the multiplier output being 0. This control bit is included for maximum flexibility, and is normally not used.

Initialize Data Memory with Zeros (Bit 7)

Setting this bit to 1 initializes all data memory locations to 0. This bit is cleared to 0 after the operation is complete. This bit should be asserted after a complete program/parameter download has occurred to ensure click-free operation.

Zero Serial Input Port (Bit 6)

When this bit is set to 1, the 16 serial input channels are forced to all 0s.

Initiate Safe Transfer to Target RAM (Bit 5)

Setting this bit to 1 initiates a safeload transfer to the target/slew RAM. This bit is cleared when the operation is completed. There are five safeload register pairs (address/data); only those registers that have been written since the last safeload event are transferred. Address 0 corresponds to the first target RAM location.

Initiate Safe Transfer to Parameter RAM (Bit 4)

Setting this bit to 1 initiates a safeload transfer to the parameter RAM. This bit is cleared when the operation is completed. There are five safeload registers pairs (address/data); only those registers that have been written since the last safeload event are transferred. Address 0 corresponds to the first parameter RAM location.

Input Serial Port to Sequencer Sync (Bits 3:2)

Normally, the internal sequencer is synchronized to the incoming audio frame rate by comparing the internal program counter with the edge of the LRCLK input signal. In some cases the AD1940 may be used to decimate an incoming signal by some integer factor. In this case, it is desirable to synchronize the sequencer to a submultiple of the incoming LRCLK rate so more than one audio input sample is available to the program during a single audio output frame. For example, if these bits are set to 01 (LRCLK/2), a 96 kHz input can be used with a 48 kHz output, allowing two consecutive input samples to be processed during a single audio output frame. Operation in this mode may require custom assembly-language coding in the ADI graphical tools.

Program Length (Bits 1:0)

96 kHz and 192 kHz modes

These bits set the length of the internal program. The default program length is 1,536 instructions for f_s = 48 kHz, but the program length can be shortened by factors of 2 to accommodate sample rates higher than 48 kHz. For f_s = 96 kHz the program length should be set to 768 (01), and the length should be set at 384 steps (10) for f_s = 192 kHz. A program length of 192 steps is available, but will not be commonly used.

Low Power Mode

This setting can also be used to reduce the power consumption of the AD1940. If the program length is set to 768 steps and f_s = 48 kHz, instead of 96 kHz, then the power consumption of the part will be cut in approximately half. Correspondingly, when the program length is set to 384 steps with f_s = 48 kHz the power consumption will be about ¼ of what it is in normal operation with 1,536 program steps and f_s = 48 kHz.

Table 20. RAM Configuration Register (2643)

Register Bits	Function
7:4	Reserved
3:0	RAM Modulo, 1 LSB corresponds to 512 locations, max = 0b1100 (6 k)

RAM CONFIGURATION REGISTER

The AD1940 uses a modulo RAM addressing scheme to allow filters and other blocks to be coded easily without requiring filter data to be explicitly moved during the filtering operation. This is accomplished by adding the contents of an address offset counter to the actual base address supplied in the AD1940's core. This address offset counter is incremented automatically at the audio frame rate.

This method works well for most audio applications that involve filtering. In some cases, however, it is desirable to have direct access to the RAM, bypassing the autoincrementing address offset counter. For this reason, the data memory in the AD1940 can be divided into modulo and nonmodulo portions by programming the RAM configuration register (Table 20). The address range from 0 to 512 × (RAM configuration register contents) is treated as modulo memory with autoincrementing address offset registers. The maximum setting of this register is the full size of the RAM, or 6,144 (6 k) data words. Note that

addresses in this range automatically wrap around the modulo boundary as set by the register. This feature is not normally used with ADI-supplied blocks. For normal operation, this register may be left in its default state, which sets up the entire RAM to use the autoincrement feature. This feature is included for maximum programming flexibility and may be used in the case of specialized software development.

CONTROL PORT READ/WRITE DATA FORMATS

The read/write formats of the control port are designed to be byte-oriented. This allows for easy programming of common microcontroller chips. In order to fit into a byte-oriented format, 0s are appended to the data fields before the MSB in order to extend the data word to the next multiple of eight bits. For example, 28-bit words written to the parameter RAM are appended with four leading 0s in order to reach 32 bits (4 bytes); 40-bit words written to the program RAM are not appended with any 0s because it is already a full 5 bytes. These zero-extended data fields are appended to a 3-byte field consisting of a 7-bit chip address, a read/write bit, and an 11-bit RAM/register address. The control port knows how many data bytes to expect based on the address that is received in the first three bytes.

The total number of bytes for a single-location write command can vary from four bytes (for a control register write), to eight bytes (for a program RAM write). Burst mode may be used to fill contiguous register or RAM locations. A burst mode write is done by writing the address and data of the first RAM/register location to be written. Rather than ending the control port transaction (by bringing the CLATCH signal high in the AD1940, after the data word, as would be done in a single-address write, the next data word can be written immediately without first writing its specific address. The AD1940 control port autoincrements the address of each write, even across the boundaries of the different RAMs and registers.

Table 21. Parameter RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes 4–6
chip_adr [6:0], $\overline{W}$/R	0000, param_adr[11:8]	param_adr[7:0]	0000, param[27:24]	param [23:0]

Table 22. Parameter RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3	Bytes 4–6	Byte 7	Byte 11
chip_adr [6:0], $\overline{W}$/R	0000, param_adr[11:8]	param_adr[7:0]	0000, param[27:24]	param[23:0]	Byte 8	Byte 12
					Byte 9	Byte 13
					Byte 10	Byte 14
			<—param_adr—>		param_adr + 1	param_adr + 2

Table 23. Program RAM Read/Write Format (Single Address)

Byte 0	Byte 1	Byte 2	Bytes 3–7
chip_adr [6:0], $\overline{W}$/R	0000, prog_adr[11:8]	prog_adr[7:0]	prog[39:0]

Table 24. Program RAM Block Read/Write Format (Burst Mode)

Byte 0	Byte 1	Byte 2	Byte 3-7	Byte 8	Byte 13
chip_adr [6:0], $\overline{W}$/R	0000, prog_adr[11:8]	prog_adr[7:0]	prog[39:0]	Byte 9	Byte 14
				Byte 10	Byte 15
				Byte 11	Byte 16
				Byte 12	Byte 17
			<—prog_adr—>	prog_adr +1	prog_adr +2

Table 25. Control Register Read/Write Format (Core, Serial Out 0, Serial Out 1)

Byte 0	Byte1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], $\overline{W}$/R	0000, reg_adr[11:8]	reg_adr[7:0]	data[15:8]	data[7:0]

Table 26. Control Register Read/Write Format (RAM Configuration, Serial Input)

Byte 0	Byte1	Byte 2	Byte 3
chip_adr [6:0], $\overline{W}$/R	0000, reg_adr[11:8]	reg_adr[7:0]	data[7:0]

Table 27. Data Capture Register Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], $\overline{W}$/R	0000, data_capture_adr[11:8]	data_capture_adr[7:0]	000, progCount[10:6][1]	progCount[5:0][1], regSel[1:0][2]

[1] ProgCount[10:0] = value of program counter where trap occurs (the table of values is generated by the program compiler).
[2] RegSel[1:0] selects one of four registers (see Data Capture Registers section).

Table 28. Data Capture (Control Port Readback) Register Read Format

Byte 0	Byte 1	Byte 2	Bytes 3–5
chip_adr [6:0], $\overline{W}$/R	0000, data_capture_adr[11:8]	data_capture_adr[7:0]	data[23:0]

Table 29. Safeload Register Data Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Bytes 4–7
chip_adr [6:0], $\overline{W}$/R	0000, safeload_adr[11:8]	safeload_adr[7:0]	000000, data[33:32]	data[31:0]

Table 30. Safeload Register Address Write Format

Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
chip_adr [6:0], $\overline{W}$/R	0000, safeload_adr[11:8]	safeload_adr[7:0]	000000, param_adr[9:8]	param_adr[7:0]

SERIAL DATA INPUT/OUTPUT PORTS

The AD1940's flexible serial data input and output ports can be set to accept or transmit data in 2-channel formats or in an 8- or 16-channel TDM stream. Data is processed in twos complement, MSB-first format. The left channel data field always precedes the right channel data field in the 2-channel streams. In the TDM modes, Slots 0 to 3 (8-channel TDM) or Slots 0 to 7 (16-channel TDM) fall in the first half of the audio frame, and Slots 4 to 7 (or Slots 8 to 15 in 16-channel TDM) are in the second half of the frame. The serial modes are set in the serial output and serial input control registers.

The input control register allows control of clock polarity and data input modes. The valid data formats are I²S , left-justified, right-justified (24-, 20-, 18-, or 16-bit), 8-channel, and 16-channel TDM. In all modes except for the right-justified modes, the serial port will accept an arbitrary number of bits up to a limit of 24. Extra bits will not cause an error, but they will be truncated internally. Proper operation of the right-justified modes requires that there be exactly 64 BCLKs per audio frame. The TDM data is input on SDATA_IN2 and SDATA_IN3 when in 2 × 8-channel TDM mode, and on SDATA_IN2 in 16-channel TDM mode. The LRCLK in TDM mode can be input to the AD1940 as either a 50/50 duty cycle clock or as a bit-wide pulse.

The two clock domains on the serial output ports can generate two separate 8-channel TDM streams or one 16-channel TDM stream. When in 16-channel TDM mode, the data is clocked by LRCLK_OUT0 and BCLK_OUT0. The AD1940 must be in slave mode for 16-channel TDM unless the data is sampled at 48 kHz; the part cannot generate a TDM bit clock that is fast enough to support 96 kHz or 192 kHz. In 8-channel TDM mode, the AD1940 can be a master for 48 kHz and 96 kHz data, but not for 192 kHz data. Table 31 displays the modes in which the serial output port will function.

The output control registers give the user control of clock polarities, clock frequencies, clock types, and data format. In all modes except for the right-justified modes (MSB delayed by 8, 12, or 16), the serial port accepts an arbitrary number of bits up to a limit of 24. Extra bits will not cause an error, but will be truncated internally. Proper operation of the right-justified modes requires the LSB to align with the edge of the LRCLK. The default settings of all serial port control registers correspond to 2-channel I²S mode. LRCLK_OUT0 and BCLK_OUT0 are clocks for Serial Output Ports 0 to 7, and LRCLK_OUT1 and BCLK_OUT1 Clock Ports 8 to 15.

All registers default to being set as all 0s. All register settings apply to both master and slave modes unless otherwise noted.

Table 32 shows the proper configurations for standard audio data formats.

Table 31 Serial Output Port Master/Slave Mode Capabilities

f_S	2-Channel Modes (I²S, Left-Justified, Right-Justified)	8-Channel TDM	16-Channel TDM
48 kHz	Master and slave	Master and slave	Master and slave
96 kHz	Master and slave	Master and slave	Slave only
192 kHz	Master and slave	Slave only	Slave only

Table 32. Data Format Configurations

Format	LRCLK Polarity	LRCLK Type	BCLK Polarity	MSB Position
I²S (Figure 16)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by one BCLK
Left-Justified (Figure 17)	Frame begins on rising edge	Clock	Data changes on falling edge	Aligned with LRCLK edge
Right-Justified (Figure 18)	Frame begins on rising edge	Clock	Data changes on falling edge	Delayed from LRCLK edge by 8, 12, or 16 BCLKs
TDM with Clock (Figure 19)	Frame begins on falling edge	Clock	Data changes on falling edge	Delayed from start of word clock by one BCLK
TDM with Pulse (Figure 20)	Frame begins on rising edge	Pulse	Data changes on falling edge	Delayed from start of word clock by one BCLK

Table 33. Serial Output Control Register 1 (Channels 0–7) (2644)

Register Bits	Function
15	Dither Enable 0 = Diabled 1 = Enabled
14	Internally Link TDM Streams into Single, 16-Channel Stream 0 = Indepenent 1 = Linked
13	LRCLK Polarity 0 = Frame Begins on Falling Edge 1 = Frame Begins on Rising Edge
12	BCLK Polarity 0 = Data Changes on Falling Edge 1 = Data Changes on Rising Edge
11	Master/Slave 0 = Slave 1 = Master
10:9	BCLK Frequency (Master Mode only) 00 = core_clock/24 01 = core_clock/12 10 = core_clock/6 11 = core_clock/3
8:7	Frame Sync Frequency (Master Mode only) 00 = core_clock/1536 01 = core_clock/768 10 = core_clock/384
6	Frame Sync Type 0 = LRCLK 1 = Pulse
5	Serial Output/TDM Mode Control 0 = 8 Serial Data Outputs 1 = Enable TDM (8- or 16-Channel) on SDATA_OUT0
4:2	MSB Position 000 = Delay by 1 001 = Delay by 0 010 = Delay by 8 011 = Delay by 12 100 = Delay by 16 101 Reserved 111 Reserved
1:0	Output Word Length, Channels 0–7 00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = 16 Bits

Table 34. Serial Output Control Register 2 (Channels 8–15) (2645)

Register Bits	Function
15	Dither Enable 0 = Disabled 1 = Enabled
14	Data Capture Serial Out Enable (Uses SDATA_OUT7) 0 = Disable 1 = Enable
13	LRCLK Polarity 0 = Frame Begins on Falling Edge 1 = Frame Begins on Rising Edge
12	BCLK Polarity 0 = Data Changes on Falling Edge 1 = Data Changes on Rising Edge
11	Master/Slave 0 = Slave 1 = Master
10:9	BCLK Frequency (Master Mode only) 00 = core_clock/24 01 = core_clock/12 10 = core_clock/6 11 = core_clock/3
8:7	Frame Sync Frequency (Master Mode only) 00 = core_clock/1536 01 = core_clock/768 10 = core_clock/384
6	Frame Sync Type 0 = LRCLK 1 = Pulse
5	Serial Output/TDM Mode Control 0 = 8 Serial Data Outputs 1 = Enable TDM on SDATA_OUT4 (8-Channel) or SDATA_OUT0 (16-Channel)
4:2	MSB Position 000 = Delay by 1 001 = Delay by 0 010 = Delay by 8 011 = Delay by 12 100 = Delay by 16 101 Reserved 111 Reserved
1:0	Output Word Length, Channels 8–15 00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = 16 Bits

SERIAL OUTPUT CONTROL REGISTERS

Dither Enable (Bit 15)

Setting this bit to 1 enables dither on the appropriate channels.

Internally Link TDM Streams into Single 16-Channel Stream (Bit 14, Serial Output Control Register 1)

When this bit is set to 1, the TDM output stream is output in a single 16-channel stream on SDATA_OUT0. When set to 0, TDM data is output on two independent 8-channel streams on Pins SDATA_OUT0 and SDATA_OUT4.

Data Capture Serial Out Enable (Bit 14, Serial Output Control Register 2)

When set to 1, SDATA_OUT7 is set as the output of the data capture digital output registers (2640–2641). See the Data Capture Registers section for a full explanation of using this mode.

LRCLK Polarity (Bit 13)

When set to 0, the left channel data is clocked when LRCLK is low, and the right data clocked when LRCLK is high. When set to 1, this is reversed.

BCLK Polarity (Bit 12)

This bit controls on which edge of the bit clock the output data is clocked. Data changes on the falling edge of BCLK_OUTx when this bit is set to 0, and on the rising edge when this bit is set at 1.

Master/Slave (Bit 11)

This bit sets whether the output port is a clock master or slave. The default setting is slave; on power-up, Pins BCLK_OUTx and LRCLK_OUTx are set as inputs until this bit is set to 1, at which time they become clock outputs.

BCLK Frequency (Bits 10:9)

When the output port is being used as a clock master, these bits set the frequency of the output bit clock, which is divided down from the internal 73.728 MHz core clock.

Frame Sync Frequency (Bits 8:7)

When the output port is used as a clock master, these bits set the frequency of the output word clock on the LRCLK_OUTx pins, which is divided down from the internal 73.728 MHz core clock.

Frame Sync Type (Bit 6)

This bit sets the type of signal on the LRCLK_OUTx pins. When set to 0, the signal is a word clock with a 50% duty cycle; when set to 1, the signal is a pulse with a duration of one bit clock at the beginning of the data frame.

Serial Output/TDM Mode Control (Bit 5)

Setting this bit to 1 changes the output port from multiple serial outputs to a single TDM output stream on the appropriate SDATA_OUTx pin. This bit must be set in both serial output control registers to enable 16-channel TDM on SDATA_OUT0.

MSB Position (Bits 4:2)

These three bits set the position of the MSB of data with respect to the LRCLK edge. The data output of the AD1940 is always MSB first.

Output Word Length (Bits 1:0)

These bits set the word length of the output data-word. All bits following the LSB are set to 0.

Table 35. Serial Input Control Register (2646)

Register Bits	Function
5	8-/16-channel TDM input 0 = Dual 8-channel TDM 1 = 16-channel TDM input
4	LRCLK polarity 0 = Frame begins on falling edge 1 = Frame begins on rising edge
3	BCLK polarity 0 = Data changes on falling edge 1 = Data changes on rising edge
2:0	Serial Input Mode 000 = I²S 001 = Left-justified 010 = TDM 011 = Right-justified, 24-bit 100 = Right-justified, 20-bit 101 = Right-justified, 18-bit 110 = Right-justified, 16-bit

SERIAL INPUT CONTROL REGISTER

8-/16-Channel TDM Input (Bit 5)

Setting this bit to 0 puts the AD1940 into dual 8-channel TDM input mode, with the two streams coming in on SDATA_IN2/TDM_IN1 and SDATA_IN3/TDM_IN0. Channels 0 to 7 will be input on TDM_IN0 and Channels 8 to 15 will come in on TDM_IN1. Setting this bit to 1 puts the part in 16-channel TDM input mode, input on TDM_IN1.

LRCLK Polarity (Bit 4)

When set to 0, the left channel data on the SDATA_INx pins is clocked when LRCLK_IN is low; and the right input data clocked when LRCLK_IN is high. When set to 1, this is reversed. In TDM mode, when this bit is set to 0, data is clocked in starting with the next appropriate BCLK edge (set in Bit 3 of this register) following a falling edge on the LRCLK_IN pin. When set to 1 and running in TDM mode, the input data is valid on the BCLK edge following a rising edge on the word clock (LRCLK_IN). The serial input port can also operate with a pulse input signal, rather than a clock. In this case, the first edge of the pulse is used by the AD1940 to start the data frame. When this polarity bit is set to 0, a low pulse should be used, and a high pulse should be used when the bit it set to 1.

BCLK Polarity (Bit 3)

This bit controls on which edge of the bit clock the input data changes, and on which edge it is clocked. Data changes on the falling edge of BCLK_IN when this bit is set to 0, and on the rising edge when this bit is set at 1.

Serial Input Mode (Bits 2:0)

These two bits control the data format that the input port expects to receive. Bits 3 and 4 of this control register will override the settings in Bits 2:0, so all four bits must be changed together for proper operation in some modes. The clock diagrams for these modes are shown in Figure 16, Figure 17, and Figure 18. Note that for left-justified and right-justified modes the LRCLK polarity is high, then low, which is opposite from the default setting of Bit 4.

When these bits are set to accept a TDM input, the AD1940's data starts after the edge defined by Bit 4. Figure 19 shows an 8-channel TDM stream with a high-to-low triggered LRCLK and data changing on the falling edge of the BCLK. The AD1940 expects the MSB of each data slot delayed by one BCLK from the beginning of the slot, just like in the stereo I²S format. In 8-channel TDM mode, Channels 0 to 3 will be in the first half of the frame, and Channels 4 to 7 will be in the second half. When in 16-channel TDM mode, the first half-frame will hold Channels 0 to 7, and the second half-frame will have Channels 8 to 15. Figure 20 shows an example of a TDM stream running with a pulse word clock, which would be used to interface to ADI codecs in their auxiliary mode. To work in this mode on either the input or output serial ports, the AD1940 should be set to frame beginning on the rising edge of LRCLK, data changing on the falling edge of BCLK, and MSB position delayed from the start of the word clock by one BCLK.

Table 32 explains the clock settings for each of these formats.

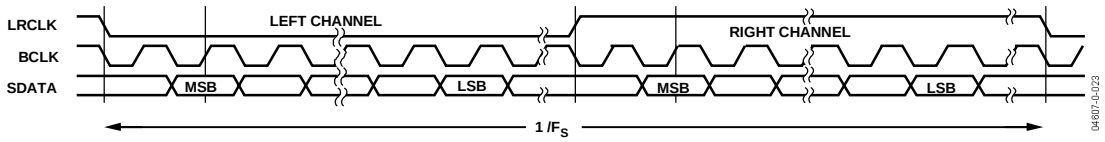


Figure 16. I²S Mode—16 to 24 Bits per Channel

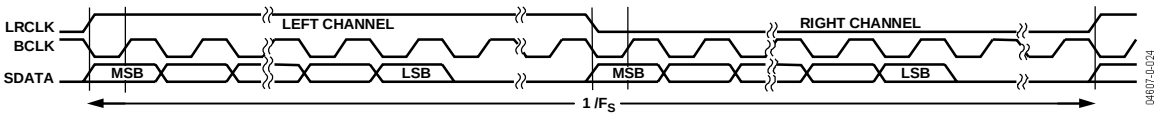


Figure 17. Left-Justified Mode—16 to 24 Bits per Channel

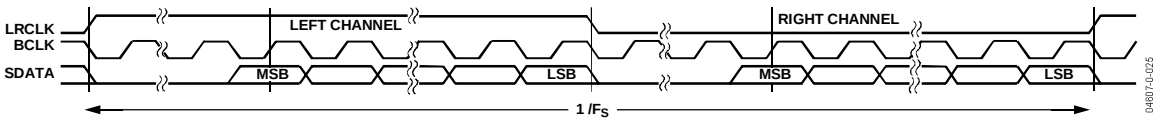


Figure 18. Right-Justified Mode—16 to 24 Bits per Channel

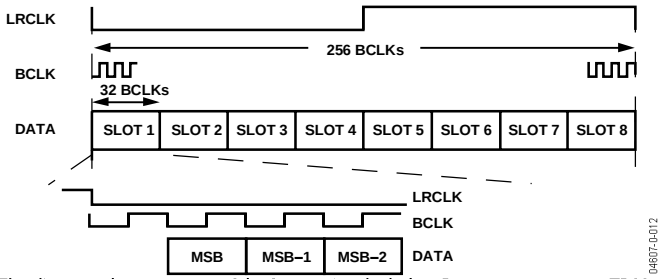


Figure 19. 8-Channel TDM Mode. This diagram shows just one of the formats in which the AD1940 can operate in TDM mode. Please refer to the Serial Data Input/Output Ports section for a more complete description of the modes of operation.

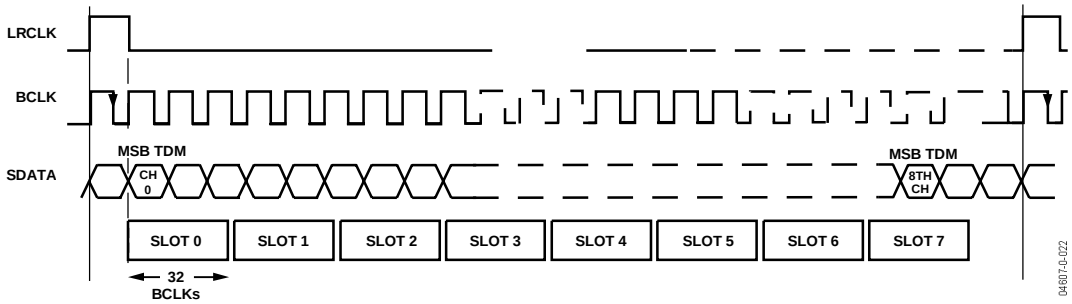


Figure 20. TDM Mode with Pulse Word Clock

INITIALIZATION

POWER-UP SEQUENCE

The AD1940 has a built-in power-up sequence that initializes the contents of all internal RAMs. During this time, the contents of the internal program boot ROM are copied to the internal program RAM memory, and the parameter RAM (all 0s) is filled with values from its associated boot ROM. The default boot ROM program simply copies the serial inputs to the serial outputs with no processing. The data memories are also cleared during this time.

The boot sequence, which starts on the rising edge of the RESETB pin, lasts for 8,192 cycles of the signal on the MCLK pin at start-up. Assuming even the slowest possible signal on this pin, a 64 × fs clock, the boot sequence will still complete before the PLL locks to the input clock. Since the boot sequence requires a stable master clock, the user should avoid writing to or reading from the registers until the MCLK input signal has settled and the PLL has locked. The PLL takes approximately 3 ms to lock. Coming out of reset, the clock mode is immediately set by the PLL_CTRL0, PLL_CTRL1, and PLL_CTRL2 pins. Reset is synched to the falling edge of the internal MCLK.

The power-up default signal processing flow in the AD1940 simply takes the eight inputs and copies these signals to the 16 digital outputs, as shown in Figure 21.

Figure 21. Default Program Signal Flow

SETTING MASTER CLOCK/PLL MODE

The AD1940's MCLK input feeds a PLL, which generates the 1536 × fs clock to run the DSP core. In normal operation, the input to MCLK must be one of the following; 64 × fs, 256 × fs, 384 × fs, or 512 × fs, where fs is the input sampling rate. The mode is set on PLL_CTRL0, PLL_CTRL1, and PLL_CTRL2, according to Table 36. If the AD1940 is set to receive double-rate signals (by reducing the number of program steps/sample by a factor of 2 using the core control register), then the master clock frequencies must be either 32 × fs, 128 × fs, 192 × fs, or 256 × fs. If the AD1940 is set to receive quad-rate signals (by reducing the number of program steps/sample by a factor of 4 using the core control register), then the master clock frequencies must be one of 16 × fs, 64 × fs, 96 × fs, or 128 × fs. On power-up, a clock signal must be present on MCLK so that the AD1940 can complete its initialization routine. The PLL can also run in bypass mode, where the clock present on MCLK is fed directly to the DSP core, although this setting is not recommended for normal operation.

Table 36. PLL Modes

MCLK Input	PLL_CTRL2	PLL_CTRL1	PLL_CTRL0
64 × fs	0	0	0
256 × fs	0	1	0
384 × fs	X[1]	X[1]	1
512 × fs	1	0	0
Bypass	1	1	0

[1] X = don't care

The clock mode should not be changed without also resetting the AD1940. If the mode is changed on the fly, a click or pop may result on the outputs. The state of the PLL_CTRLx pins should be changed while RESETB is held low.

VOLTAGE REGULATOR

The AD1940 includes an on-board voltage regulator that allows the chip to be used in systems where a 2.5 V supply is not available, but 3.3 V or 5 V is. The only external components needed for this are a PNP transistor such as an FZT953, a single capacitor, and a single resistor. The recommended design for the voltage regulator is shown in Figure 22. The 10 µF and 100 nF capacitors shown in this schematic are recommended for bypassing, but are not necessary for operation. Here, VDD is the main system voltage (3.3 V or 5 V) and should be connected to VSUPPLY. 2.5 V is generated at the transistor's collector, which is connected to the VDD pins, PLL_VDD and VSENSE. The reference voltage on VREF is 1.15 V and is generated by the regulator. A 1 nF capacitor should be connected between this pin and ground. VDRIVE is connected to the base of the PNP transistor. A 1 kΩ resistor should be connected between VDRIVE and VSUPPLY.

If the regulator is not used in the design, VSUPPLY, VREF, VDRIVE, and VSENSE can be tied to ground.

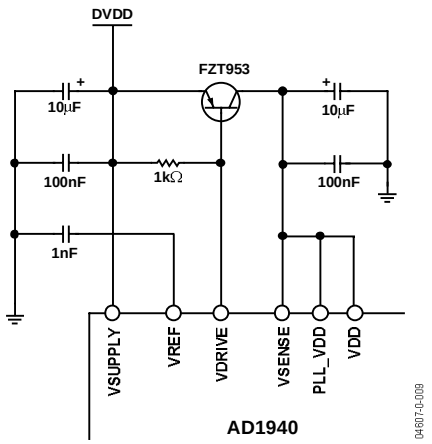
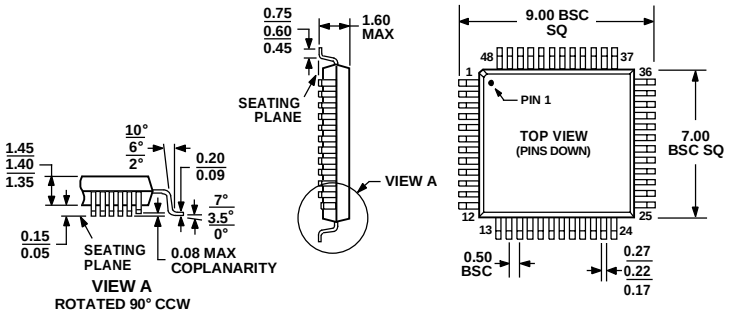


Figure 22. Voltage Regulator Design

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026BBC

Figure 23. 48-Lead Low-Profile Quad Flat Package [LQFP]
Dimensions Shown in Millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD1940YST	−40°C to +105°C	48-Lead LQFP	ST-48
AD1940YSTRL	−40°C to +105°C	48-Lead LQFP	ST-48 in 13″ Reel
AD1940YSTZ[1]	−40°C to +105°C	48-Lead LQFP	ST-48
AD1940YSTZRL[1]	−40°C to +105°C	48-Lead LQFP	ST-48 in 13″ Reel
Eval-AD1940EB		Evaluation Board	

[1] Z= Pb-free part.

NOTES

NOTES

Nonvolatile, I²C-Compatible 256-Position, Digital Potentiometer

AD5259

FEATURES

- Nonvolatile memory maintains wiper settings
- 256-position
- Thin LFCSP-10 (3 mm x 3 mm x 0.8 mm) package
- Compact MSOP-10 (3 mm × 4.9 mm x 1.1mm) package
- I²C®-compatible interface
- V_{LOGIC} pin provides increased interface flexibility
- End-to-end resistance 5 kΩ, 10 kΩ, 50 kΩ, 100 kΩ
- Resistance tolerance stored in EEPROM (0.1% accuracy)
- Power-on EEPROM refresh time < 1ms
- Software write protect command
- Address Decode Pin AD0 and Pin AD1 allow 4 packages per bus
- 100-year typical data retention at 55°C
- Wide operating temperature –40°C to +85°C
- 3 V to 5 V single supply

APPLICATIONS

- LCD panel V_{COM} adjustment
- LCD panel brightness and contrast control
- Mechanical potentiometer replacement in new designs
- Programmable power supplies
- RF amplifier biasing
- Automotive electronics adjustment
- Gain control and offset adjustment
- Fiber to the home systems
- Electronics level settings

GENERAL DESCRIPTION

The AD5259 provides a compact, nonvolatile LFCSP-10 (3 mm × 3 mm) or MSOP-10 (3 mm × 4.9 mm) packaged solution for 256-position adjustment applications. These devices perform the same electronic adjustment function as mechanical potentiometers[1] or variable resistors, but with enhanced resolution and solid-state reliability.

The wiper settings are controllable through an I²C-compatible digital interface that is also used to read back the wiper register and EEPROM content. Resistor tolerance is also stored within EEPROM, providing an end-to-end tolerance accuracy of 0.1%.

A separate V_{LOGIC} pin delivers increased interface flexibility. For users who need multiple parts on one bus, Address Bit AD0 and Address Bit AD1 allow up to four devices on the same bus.

FUNCTIONAL BLOCK DIAGRAMS

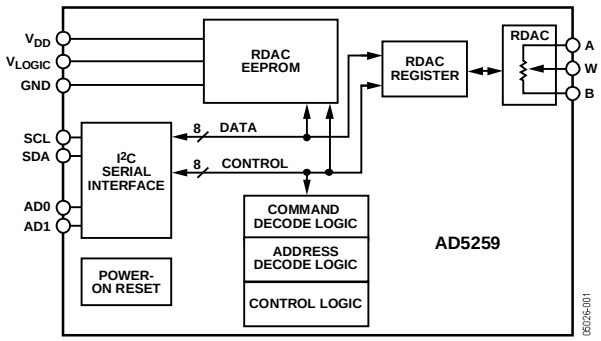


Figure 1. Block Diagram

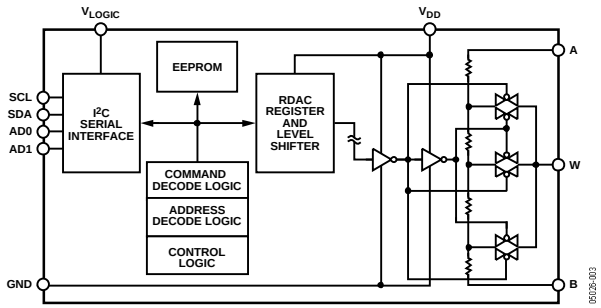


Figure 2. Block Diagram Showing Level Shifters

CONNECTION DIAGRAM

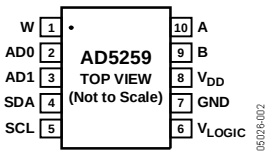


Figure 3. Pinout

[1] The terms digital potentiometer, VR (variable resistor), and RDAC are used interchangeably.

Rev. A

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REVISION HISTORY

7/05 — Rev. 0 to Rev. A

Added 10-Lead LFCSP ..... Universal
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2/05 — Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

V_{DD} = V_{LOGIC} = 5 V ± 10% or 3 V ± 10%; V_A = V_{DD}; V_B = 0 V; −40°C < T_A < +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS: RHEOSTAT MODE						
Resistor Differential Nonlinearity	R-DNL	R_{WB}, V_A = no connect				LSB
5 kΩ			−1	±0.2	+1	
10 kΩ			−1	±0.1	+1	
50 kΩ/100 kΩ			−0.5	±0.1	+0.5	
Resistor Integral Nonlinearity	R-INL	R_{WB}, V_A = no connect				LSB
5 kΩ			−4	±0.3	+4	
10 kΩ			−2	±0.2	+2	
50 kΩ/100 kΩ			−1	±0.4	+1	
Nominal Resistor Tolerance	ΔR_{AB}	T_A = 25°C, V_{DD} = 5.5 V	−30		+30	%
Resistance Temperature Coefficient	$(\Delta R_{AB} \times 10^6)/(R_{AB} \times \Delta T)$	Code = 0x00/0x80		500/15		ppm/°C
Total Wiper Resistance	R_{WB}	Code = 0x00		75	350	Ω
DC CHARACTERISTICS: POTENTIOMETER DIVIDER MODE						
Differential Nonlinearity	DNL					LSB
5 kΩ			−1	±0.2	+1	
10 kΩ			−0.5	±0.1	+0.5	
50 kΩ/100 kΩ			−0.5	±0.2	+0.5	
Integral Nonlinearity	INL					LSB
5 kΩ			−1	±0.2	+1	
10 kΩ			−0.5	±0.1	+0.5	
50 kΩ/100 kΩ			−0.5	±0.1	+0.5	
Full-Scale Error	V_{WFSE}	Code = 0xFF				LSB
5 kΩ			−7	−3	0	
10 kΩ			−4	−1.5	0	
50 kΩ/100 kΩ			−1	−0.4	0	
Zero-Scale Error	V_{WZSE}	Code = 0x00				LSB
5 kΩ			0	2.5	4	
10 kΩ			0	1	3	
50 kΩ/100 kΩ			0	0.2	0.5	
Voltage Divider Temperature Coefficient	$(\Delta V_W \times 10^6)/(V_W \times \Delta T)$	Code = 0x00/0x80		60/5		ppm/°C
RESISTOR TERMINALS						
Voltage Range	$V_{A, B, W}$		GND		V_{DD}	V
Capacitance A, B	$C_{A, B}$	f = 1 MHz, measured to GND, code = 0x80		45		pF
Capacitance W	C_W	f = 1 MHz, measured to GND, code = 0x80		60		pF
Common-Mode Leakage	I_{CM}	V_A = V_B = V_{DD}/2		10		nA

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DIGITAL INPUTS AND OUTPUTS						
Input Logic High	V_{IH}		0.7 × V_L		V_L + 0.5	V
Input Logic Low	V_{IL}		−0.5		0.3 × V_L	V
Leakage Current	I_{IL}					µA
SDA, AD0, AD1		V_{IN} = 0 V or 5 V		0.01	±1	
SCL – Logic High		V_{IN} = 0 V	−2.5	−1.3	+1	
SCL – Logic Low		V_{IN} = 5 V		0.01	±1	
Input Capacitance	C_{IL}			5		pF
POWER SUPPLIES						
Power Supply Range	V_{DD}		2.7		5.5	V
Positive Supply Current	I_{DD}			0.1	2	µA
Logic Supply	V_{LOGIC}		2.7		5.5	V
Logic Supply Current	I_{LOGIC}	V_{IH} = 5 V or V_{IL} = 0 V		3	6	µA
Programming Mode Current (EEPROM)	$I_{LOGIC(PROG)}$	V_{IH} = 5 V or V_{IL} = 0 V		35		mA
Power Dissipation	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = 5 V		15	40	µW
Power Supply Rejection Ratio	PSRR	V_{DD} = +5 V ± 10%, code = 0x80		±0.005	±0.06	%/%
DYNAMIC CHARACTERISTICS						
Bandwidth –3 dB	BW	Code = 0x80				
		R_{AB} = 5 kΩ		2000		kHz
		R_{AB} = 10 kΩ		800		kHz
		R_{AB} = 50 kΩ		160		kHz
		R_{AB} = 100 kΩ		80		kHz
Total Harmonic Distortion	THD_W	R_{AB} = 10 kΩ, V_A = 1 V rms, V_B = 0, f = 1 kHz		0.01		%
V_W Settling Time	t_S	R_{AB} = 10 kΩ, V_{AB} = 5 V, ±1 LSB error band		500		ns
Resistor Noise Voltage Density	e_{N_WB}	R_{WB} = 5 kΩ, f = 1 kHz		9		nV/√Hz

[1] Typical values represent average readings at 25°C and V_{DD} = 5 V.

TIMING CHARACTERISTICS

V_{DD} = V_{LOGIC} = 5 V ± 10% or 3 V ± 10%; V_A = V_{DD}; V_B = 0 V; −40°C < T_A < +85°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
I²C INTERFACE TIMING CHARACTERISTICS[1]						
SCL Clock Frequency	f_{SCL}		0		400	kHz
t_{BUF} Bus Free Time Between Stop and Start	t_1		1.3			µs
$t_{HD;STA}$ Hold Time (Repeated Start)	t_2	After this period, the first clock pulse is generated.	0.6			µs
t_{LOW} Low Period of SCL Clock	t_3		1.3			µs
t_{HIGH} High Period of SCL Clock	t_4		0.6			µs
$t_{SU;STA}$ Setup Time for Repeated Start Condition	t_5		0.6			µs
$t_{HD;DAT}$ Data Hold Time	t_6		0		0.9	µs
$t_{SU;DAT}$ Data Setup Time	t_7		100			ns
t_F Fall Time of Both SDA and SCL Signals	t_8				300	ns
t_R Rise Time of Both SDA and SCL Signals	t_9				300	ns
$t_{SU;STO}$ Setup Time for Stop Condition	t_{10}		0.6			µs
EEPROM Data Storing Time	t_{EEMEM_STORE}			26		ms
EEPROM Data Restoring Time at Power On[2]	$t_{EEMEM\_RESTORE1}$	V_{DD} rise time dependent. Measure without decoupling capacitors at V_{DD} and GND.		300		µs
EEPROM Data Restoring Time upon Restore Command[2]	$t_{EEMEM\_RESTORE2}$	V_{DD} = 5 V.		300		µs
EEPROM Data Rewritable Time[3]	$t_{EEMEM\_REWRITE}$			540		µs
FLASH/EE MEMORY RELIABILITY						
Endurance[4]			100	700		kCycles
Data Retention[5]				100		Years

[1] Standard I²C mode operation guaranteed by design.
[2] During power-up, the output is momentarily preset to midscale before restoring EEPROM content.
[3] Delay time after power-on PRESET prior to writing new EEPROM data.
[4] Endurance is qualified to 100,000 cycles per JEDEC Std. 22 method A117, and is measured at –40°C, +25°C, and +85°C; typical endurance at +25°C is 700,000 cycles.
[5] Retention lifetime equivalent at junction temperature (T_J) = 55°C per JEDEC Std. 22, Method A117. Retention lifetime based on an activation energy of 0.6 eV derates with junction temperature.

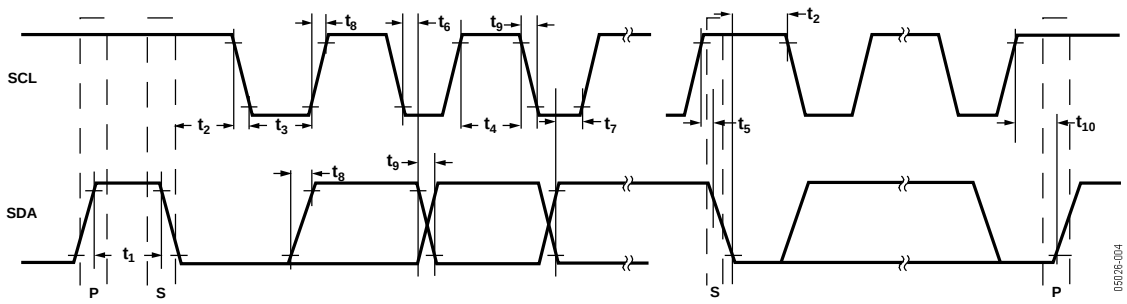

Figure 4. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Value
V_{DD}, V_{LOGIC} to GND	–0.3 V to +7 V
V_A, V_B, V_W to GND	GND – 0.3 V, V_{DD} + 0.3 V
I_{MAX}	
Pulsed[1]	±20 mA
Continuous	±5 mA
Digital Inputs and Output Voltage to GND	0 V to 7 V
Operating Temperature Range	–40°C to +85°C
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Thermal Resistance[2]	
θ_{JA}: MSOP–10	200°C/W

[1] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

[2] Package power dissipation = (T_{JMAX} – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

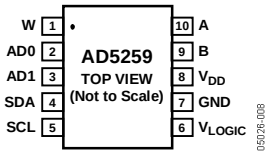

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin	Mnemonic	Description
1	W	W Terminal, GND ≤ V_W ≤ V_{DD}.
2	ADO	Programmable Pin 0 for Multiple Package Decoding. State is registered on power-up.
3	AD1	Programmable Pin 1 for Multiple Package Decoding. State is registered on power-up.
4	SDA	Serial Data Input/Output.
5	SCL	Serial Clock Input. Positive edge triggered.
6	V_{LOGIC}	Logic Power Supply.
7	GND	Digital Ground.
8	V_{DD}	Positive Power Supply.
9	B	B Terminal, GND ≤ V_B ≤ V_{DD}.
10	A	A Terminal, GND ≤ V_A ≤ V_{DD}.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = V_{LOGIC} = 5.5$ V, $R_{AB} = 10$ kΩ, $T_A = +25°C$; unless otherwise noted.

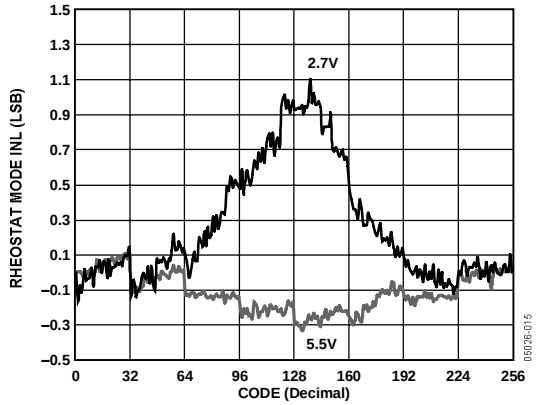

Figure 6. R-INL vs. Code vs. Supply Voltage

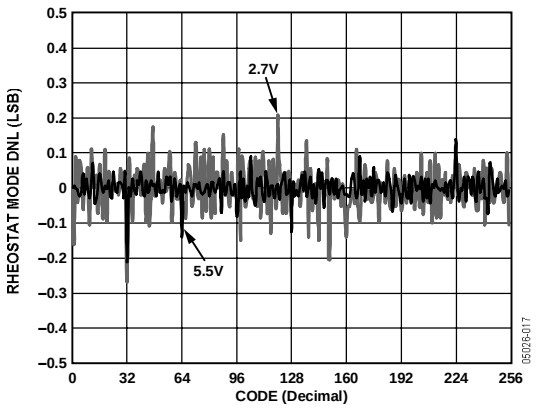

Figure 7. R-DNL vs. Code vs. Supply Voltage

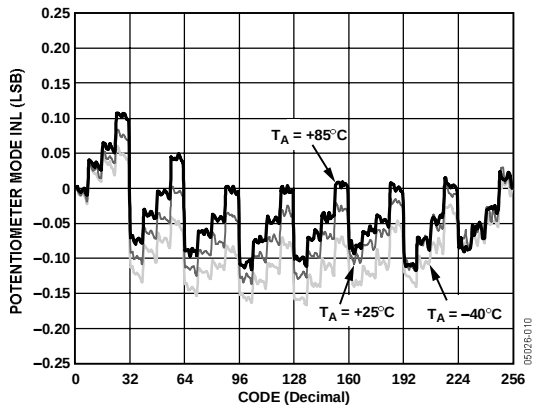

Figure 8. INL vs. Code vs. Temperature

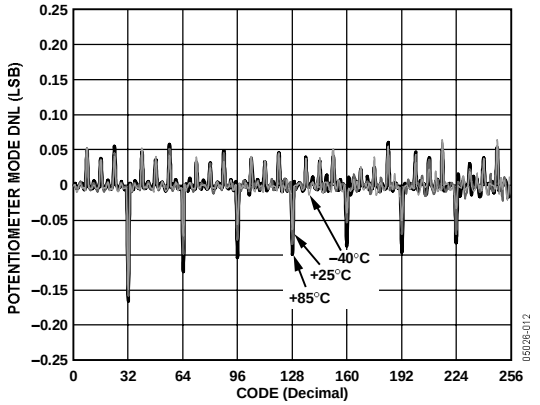

Figure 9. DNL vs. Code vs. Temperature

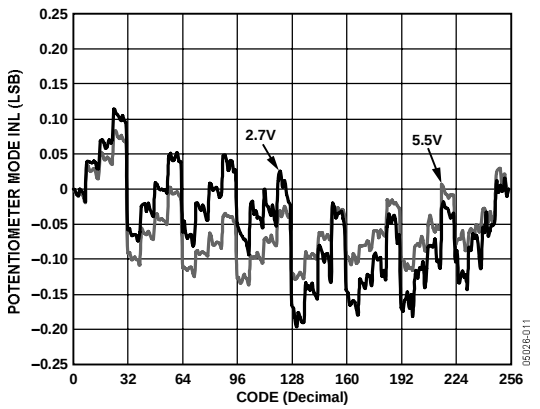

Figure 10. INL vs. Supply Voltages

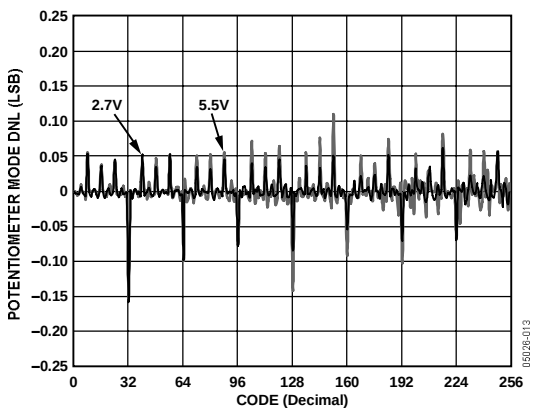

Figure 11. DNL vs. Code vs. Supply Voltage

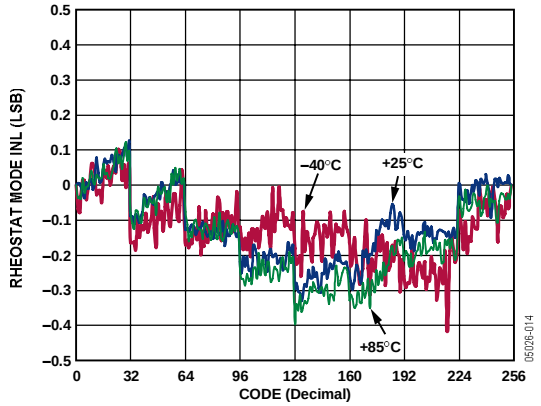

Figure 12. R-INL vs. Code vs. Temperature

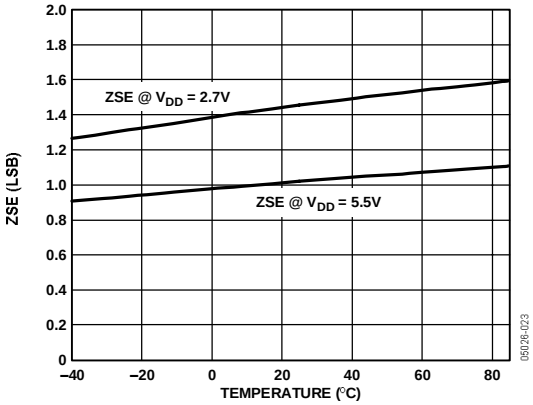

Figure 15. Zero-Scale Error vs. Temperature

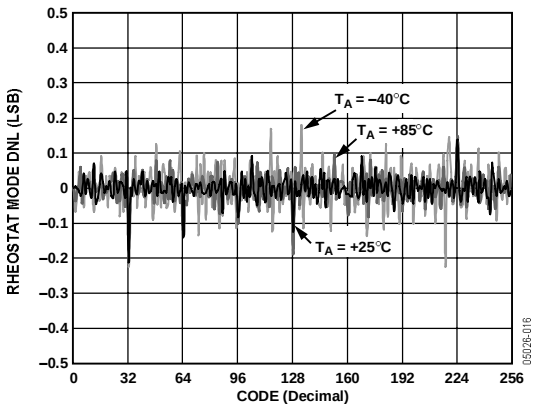

Figure 13. R-DNL vs. Code vs. Temperature

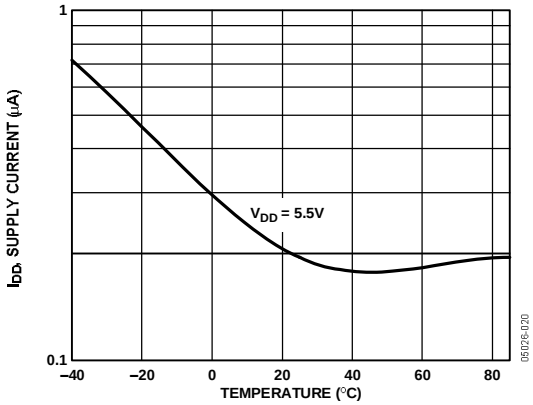

Figure 16. Supply Current vs. Temperature

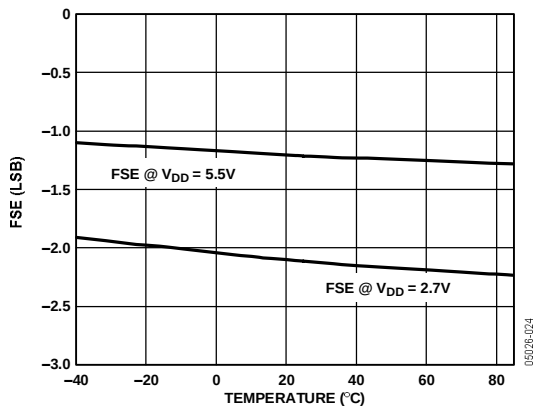

Figure 14. Full-Scale Error vs. Temperature

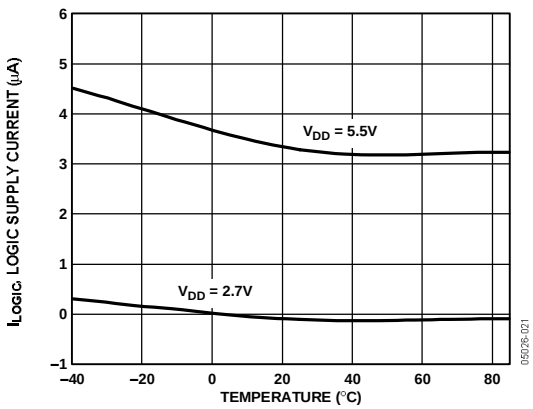

Figure 17. Logic Supply Current vs. Temperature vs. V_{DD}

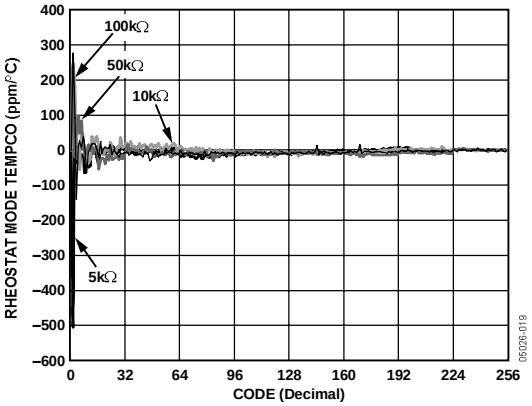

Figure 18. Rheostat Mode Tempco ($\Delta R_{AB} \times 10^6$)/($R_{AB} \times \Delta T$) vs. Code

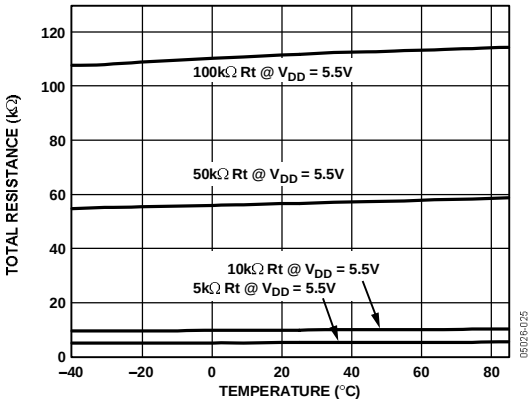

Figure 21. Total Resistance vs. Temperature

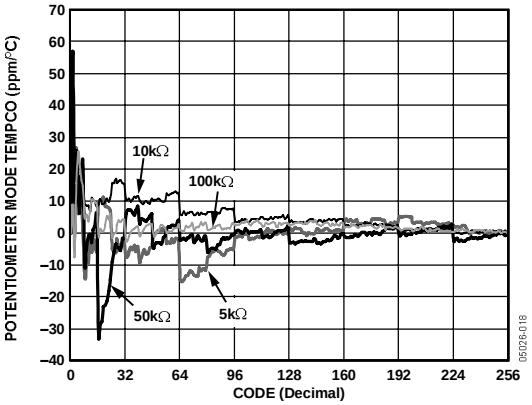

Figure 19. Potentiometer Mode Tempco ($\Delta V_W \times 10^6$)/($V_W \times \Delta T$) vs. Code

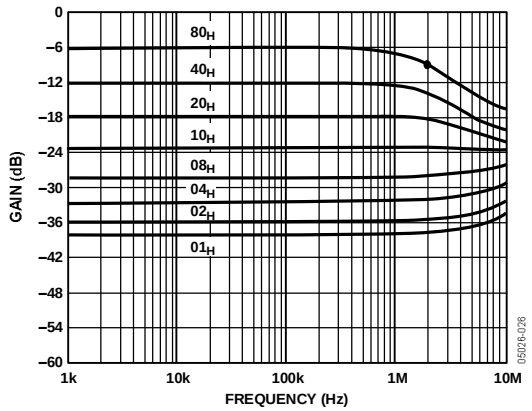

Figure 22. Gain vs. Frequency vs. Code, R_{AB} = 5 kΩ

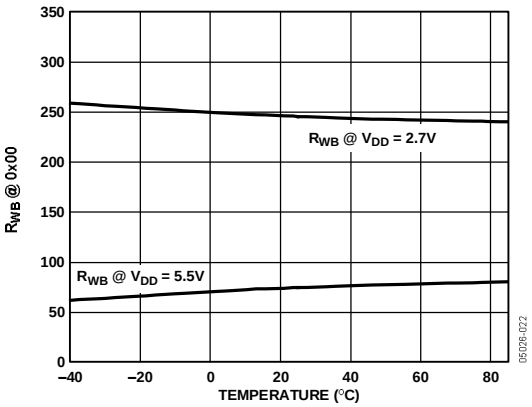

Figure 20. R_{WB} vs. Temperature

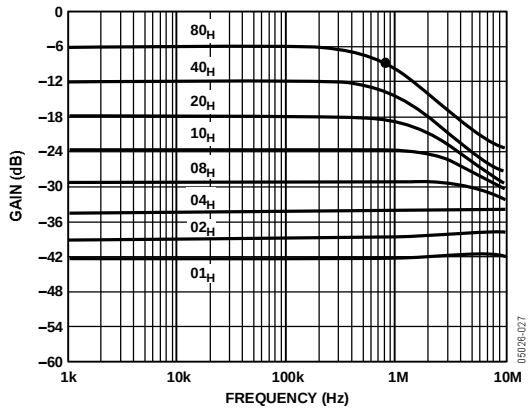

Figure 23. Gain vs. Frequency vs. Code, R_{AB} = 10 kΩ

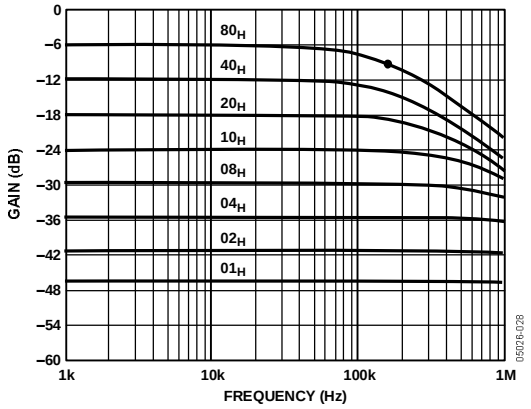

Figure 24. Gain vs. Frequency vs. Code, R_{AB} = 50 kΩ

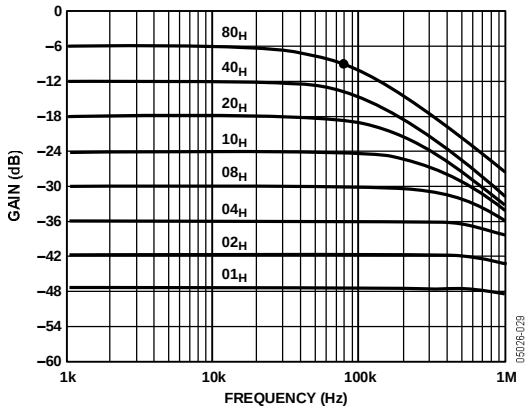

Figure 25. Gain vs. Frequency vs. Code, R_{AB} = 100 kΩ

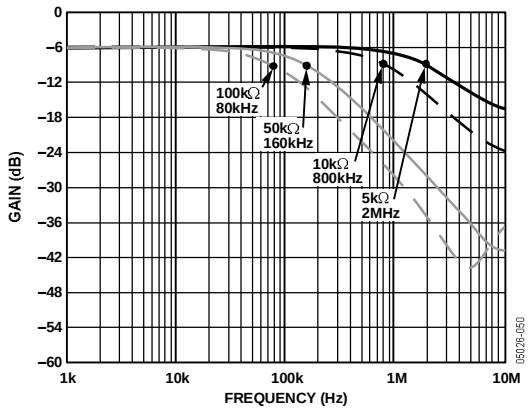

Figure 26. –3 dB Bandwidth @ Code = 0×80

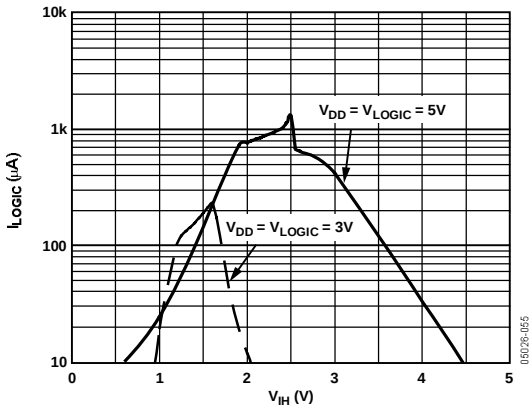

Figure 27. Logic Supply Current vs. Input Voltage

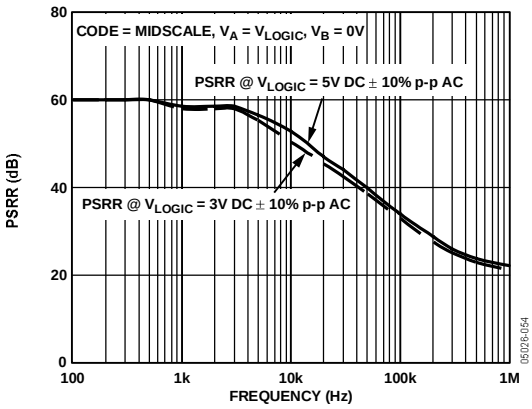

Figure 28. PSRR vs. Frequency

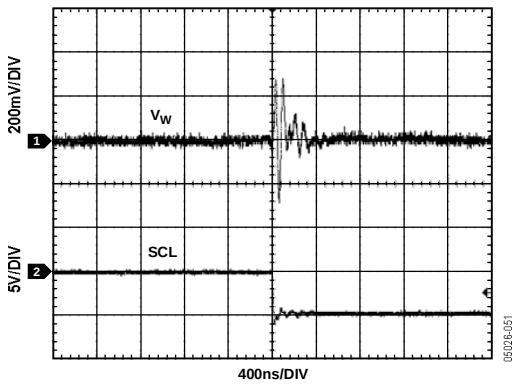

Figure 29. Digital Feedthrough

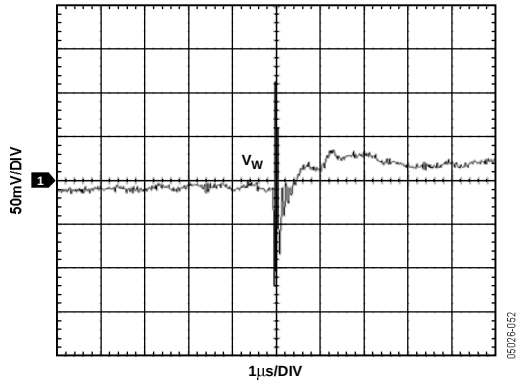

Figure 30. Midscale Glitch, Code 0×7F to 0×80

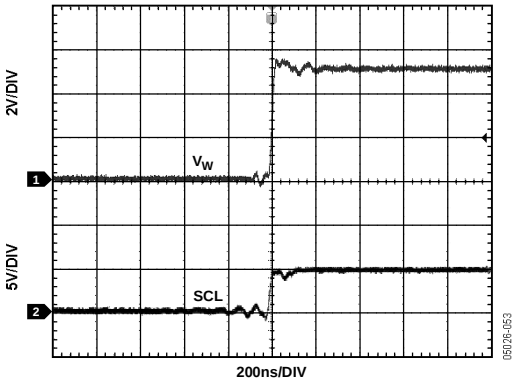

Figure 31. Large Signal Settling Time

TEST CIRCUITS

Figure 32 through Figure 37 illustrate the test circuits that define the test conditions used in the product Specifications tables.

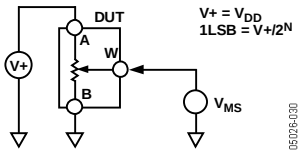

Figure 32. Test Circuit for Potentiometer Divider Nonlinearity Error (INL, DNL)

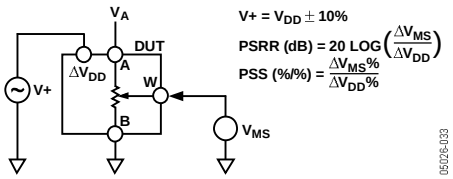

Figure 35. Test Circuit for Power Supply Sensitivity (PSS, PSSR)

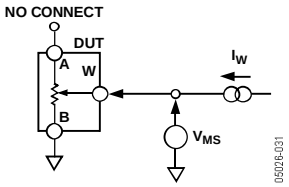

Figure 33. Test Circuit for Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

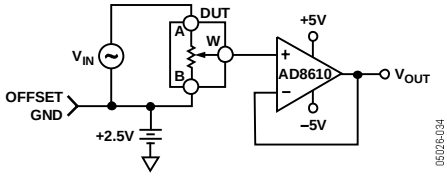

Figure 36. Test Circuit for Gain vs. Frequency

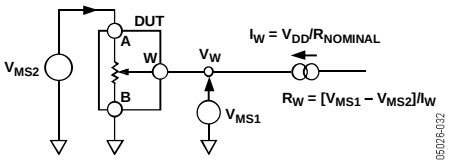

Figure 34. Test Circuit for Wiper Resistance

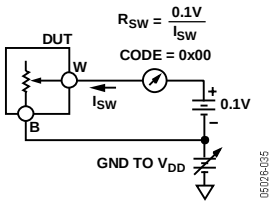

Figure 37. Test Circuit for Common-Mode Leakage Current

THEORY OF OPERATION

The AD5259 is a 256-position digitally-controlled variable resistor (VR) device. EEPROM is pre-loaded at midscale from the factory, and initial power-up is, accordingly, at midscale.

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistance (R_{AB}) of the RDAC between Terminal A and Terminal B is available in 5 kΩ, 10 kΩ, 50 kΩ, and 100 kΩ. The nominal resistance of the VR has 256 contact points accessed by the wiper terminal. The 8-bit data in the RDAC latch is decoded to select one of 256 possible settings.

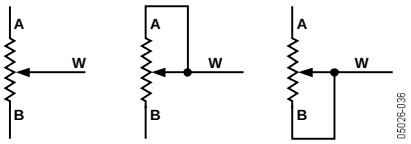

Figure 38. Rheostat Mode Configuration

The general equation determining the digitally programmed output resistance between Wiper W and Terminal B is

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + 2 \times R_W \quad (1)$$

where:
D is the decimal equivalent of the binary code loaded in the 8-bit RDAC register.
R_{AB} is the end-to-end resistance.
R_W is the wiper resistance contributed by the ON resistance of each internal switch.

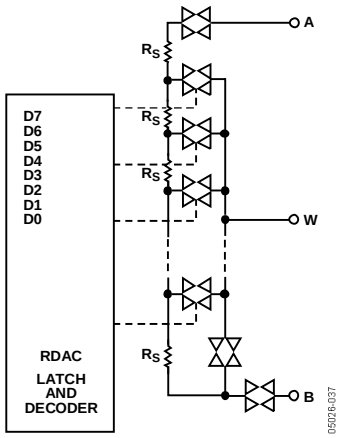

Figure 39. AD5259 Equivalent RDAC Circuit

In the zero-scale condition, there is a relatively low value finite wiper resistance. Care should be taken to limit the current flow between Wiper W and Terminal B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or destruction of the internal switch contact can occur.

Similar to the mechanical potentiometer, the resistance of the RDAC between Wiper W and Terminal A produces a digitally controlled complementary resistance, R_{WA}. The resistance value setting for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch increases in value. The general equation for this operation is

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + 2 \times R_W \quad (2)$$

Typical device-to-device matching is process lot dependent and may vary by up to ±30%. For this reason, resistance tolerance is stored in the EEPROM, enabling the user to know the actual R_{AB} within 0.1%.

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates a voltage divider at Wiper W to Terminal B and Wiper W to Terminal A proportional to the input voltage at Terminal A to Terminal B. Unlike the polarity of V_{DD} to GND, which must be positive, voltage across Terminal A to Terminal B, Wiper W to Terminal A, and Wiper W to Terminal B can be at either polarity.

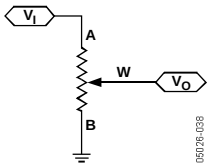

Figure 40. Potentiometer Mode Configuration

If ignoring the effect of the wiper resistance for approximation, connecting the A terminal to 5 V and the B terminal to ground produces an output voltage at Wiper W to Terminal B starting at 0 V up to 1 LSB less than 5 V. The general equation defining the output voltage at V_W with respect to ground for any valid input voltage applied to Terminal A and Terminal B is

$$V_W(D) = \frac{D}{256} V_A + \frac{256 - D}{256} V_B \quad (3)$$

A more accurate calculation, which includes the effect of wiper resistance, V_W, is

$$V_W(D) = \frac{R_{WB}(D)}{R_{AB}} V_A + \frac{R_{WA}(D)}{R_{AB}} V_B \quad (4)$$

Operation of the digital potentiometer in the divider mode results in a more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent mainly on the ratio of the Internal Resistors R_{WA} and R_{WB} and not the absolute values.

I²C-COMPATIBLE INTERFACE

The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high (see Figure 4). The next byte is the slave address byte, which consists of the slave address (first 7 bits) followed by an R/$\overline{W}$ bit (see Table 6). When the R/$\overline{W}$ bit is high, the master reads from the slave device. When the R/$\overline{W}$ bit is low, the master writes to the slave device.

The slave address of the part is determined by two configurable address pins, Pin AD0 and Pin AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I²C 7-bit address (see Table 5). The slave address corresponding to the transmitted address bits responds by pulling the SDA line low during the ninth clock pulse (this is termed the slave acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to, or read from, its serial register.

WRITING

In the write mode, the last bit (R/$\overline{W}$) of the slave address byte is logic low. The second byte is the instruction byte. The first three bits of the instruction byte are the command bits (see Table 6). The user must choose whether to write to the RDAC register, EEPROM register, or activate the software write protect (see Table 7 to Table 10). The final five bits are all zeros (see Table 13 to Table 14). The slave again responds by pulling the SDA line low during the ninth clock pulse.

The final byte is the data byte MSB first. With the write protect mode, data is not stored; rather, a logic high in the LSB enables write protect. Likewise, a logic low disables write protect. The slave again responds by pulling the SDA line low during the ninth clock pulse.

STORING/RESTORING

In this mode, only the address and instruction bytes are necessary. The last bit (R/$\overline{W}$) of the address byte is logic low. The first three bits of the instruction byte are the command bits (see Table 6). The two choices are transfer data from RDAC to EEPROM (store), or from EEPROM to RDAC (restore). The final five bits are all zeros (see Table 13 to Table 14).

READING

Assuming the register of interest was not just written to, it is necessary to write a dummy address and instruction byte. The instruction byte will vary depending on whether the data that is wanted is the RDAC register, EEPROM register, or tolerance register (see Table 11 and Table 16).

After the dummy address and instruction bytes are sent, a repeat start is necessary. After the repeat start, another address byte is needed, except this time the R/$\overline{W}$ bit is logic high. Following this address byte is the readback byte containing the information requested in the instruction byte. Read bits appear on the negative edges of the clock.

The tolerance register can be read back individually (see Table 15) or consecutively (see Table 16). Refer to the Read Modes section for detailed information on the interpretation of the tolerance bytes.

After all data bits have been read or written, a stop condition is established by the master. A stop condition is defined as a low-to-high transition on the SDA line while SCL is high. In write mode, the master pulls the SDA line high during the tenth clock pulse to establish a stop condition (see Figure 46). In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the tenth clock pulse, and then raises SDA high to establish a stop condition (see Figure 47).

A repeated write function gives the user flexibility to update the RDAC output a number of times after addressing and instructing the part only once. For example, after the RDAC has acknowledged its slave address and instruction bytes in the write mode, the RDAC output is updated on each successive byte until a stop condition is received. If different instructions are needed, the write/read mode has to start again with a new slave address, instruction, and data byte. Similarly, a repeated read function of the RDAC is also allowed.

I²C-COMPATIBLE FORMAT

The following generic, write, read, and store/restore control registers for the AD5259 all refer to the device addresses listed in Table 5; the mode/condition reference key (S, P, SA, MA, NA, $\overline{W}$, R, and X) is listed below.

S = Start Condition

P = Stop Condition

SA = Slave Acknowledge

MA = Master Acknowledge

NA = No Acknowledge

$\overline{\mathbf{W}}$ = Write

R = Read

X = Don't Care

AD1 and AD0 are two-state address pins.

Table 5. Device Address Lookup

AD1 Address Pin	AD0 Address Pin	I²C Device Address
0	0	0011000
1	0	0011010
0	1	1001100
1	1	1001110

GENERIC INTERFACE

Table 6. Generic Interface Format

S	**7-Bit Device Address** (See Table 5)	R/$\overline{W}$	SA	C2	C1	C0	A4	A3	A2	A1	A0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

Table 7. RDAC-to-EEPROM Interface Command Descriptions

C2	C1	C0	Command Description
0	0	0	Operation Between Interface and RDAC.
0	0	1	Operation Between Interface and EEPROM.
0	1	0	Operation Between Interface and Write Protection Register. See Table 10.
1	0	0	NOP.
1	0	1	Restore EEPROM to RDAC.
1	1	0	Store RDAC to EEPROM.

WRITE MODES

Table 8. Writing to RDAC Register

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	0	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

Table 9. Writing to EEPROM Register

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	1	0	0	0	0	0	SA	D7	D6	D5	D4	D3	D2	D1	D0	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

Table 10. Activating/Deactivating Software Write Protect

S	**7-Bit Device Address** (See Table 5)	0	SA	0	1	0	0	0	0	0	0	SA	0	0	0	0	0	0	0	WP	SA	P
	Slave Address Byte			Instruction Byte									Data Byte									

In order to activate the write protection mode, the WP bit in Table 10 must be logic high. To deactivate the write protection, the command must be sent again, except with the WP in logic zero state. WP is reset to the deactivated mode if power is cycled off and on.

READ MODES

Read modes are referred to as traditional because the first two bytes for all three cases are dummy bytes, which function to place the pointer towards the correct register; this is the reason for the repeat start. Theoretically, this step can be avoided if the user reads a register previously written to. For example, if the EEPROM was just written to, the user can then skip the two dummy bytes and proceed directly to the slave address byte, followed by the EEPROM readback data.

Table 11. Traditional Readback of RDAC Register Value

S	**7-Bit Device Address** (See Table 5)		0	SA	0	0	0	0	0	0	0	SA	S	**7-Bit Device Address** (See Table 5)		1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte				Instruction Byte									Slave Address Byte				Read Back Data									

↑
Repeat start

Table 12. Traditional Readback of Stored EEPROM Value

S	**7-Bit Device Address** (See Table 5)		0	SA	0	0	1	0	0	0	0	SA	S	**7-Bit Device Address** (See Table 5)		1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte				Instruction Byte									Slave Address Byte				Read Back Data									

↑
Repeat start

STORE/RESTORE MODES

Table 13. Storing RDAC Value to EEPROM

S	**7-Bit Device Address** (See Table 5)	0	SA	**1**	**1**	0	0	0	0	0	0	SA	P
	Slave Address Byte			Instruction Byte									

Table 14. Restoring EEPROM to RDAC

S	**7-Bit Device Address** (See Table 5)	0	SA	1	0	1	0	0	0	0	0	SA	P
	Slave Address Byte			Instruction Byte									

TOLERANCE READBACK MODES

Table 15. Traditional Readback of Tolerance (Individually)

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	**1**	**1**	**1**	**1**	**1**	0	SA	S	**7-Bit Device Address** (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte										Slave Address Byte			Sign + Integer Byte									

↑ Repeat start

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	1	1	1	1	1	1	SA	S	**7-Bit Device Address** (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte										Slave Address Byte			Decimal Byte									

↑ Repeat start

Table 16.Traditional Readback of Tolerance (Consecutively)

S	**7-Bit Device Address** (See Table 5)	0	SA	0	0	1	1	1	1	1	0	SA	S	**7-Bit Device Address** (See Table 5)	1	SA	D7	D6	D5	D4	D3	D2	D1	D0	MA	D7	D6	D5	D4	D3	D2	D1	D0	NA	P
	Slave Address Byte			Instruction Byte										Slave Address Byte			Sign + Integer Byte									Decimal Byte									

↑ Repeat start

Calculating R_{AB} Tolerance Stored in Read-Only Memory

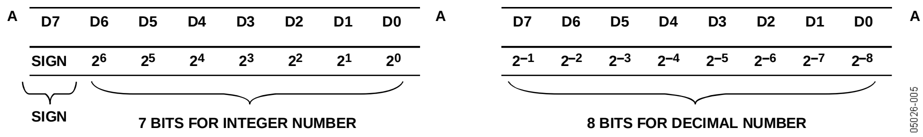

Figure 41. Format of Stored Tolerance in Sign Magnitude Format with Bit Position Descriptions. (Unit is Percent. Only Data Bytes are Shown.)

The AD5259 features a patented R_{AB} tolerance storage in the nonvolatile memory. The tolerance is stored in the memory during factory production and can be read by users at any time. The knowledge of stored tolerance allows users to accurately calculate R_{AB}. This feature is valuable for precision, rheostat mode, and open-loop applications where knowledge of absolute resistance is critical.

The stored tolerance resides in the read-only memory and is expressed as a percentage. The tolerance is stored in two memory location bytes in sign magnitude binary form (see Figure 41).

The two EEPROM address bytes are 11110 (sign + integer) and 11111 (decimal number). The two bytes can be individually accessed with two separate commands (see Table 15). Alternatively, readback of the first byte followed by the second byte can be done in one command (see Table 16). In the latter case, the memory pointer will automatically increment from the first to the second EEPROM location (increments from 11110 to 11111) if read consecutively.

In the first memory location, the MSB is designated for the sign (0 = + and 1= −) and the seven LSBs are designated for the integer portion of the tolerance. In the second memory location, all eight data bits are designated for the decimal portion of tolerance. Note the decimal portion has a limited accuracy of only 0.1%. For example, if the rated R_{AB} = 10 kΩ and the data readback from Address 11110 shows 0001 1100, and Address 11111 shows 0000 1111, then the tolerance can be calculated as

MSB: 0 = +
Next 7 MSB: 001 1100 = 28
8 LSB: 0000 1111 = $15 \times 2^{-8} = 0.06$
Tolerance = +28.06%
Rounded Tolerance = +28.1% and therefore,
R_{AB_ACTUAL} = 12.810 kΩ

ESD PROTECTION OF DIGITAL PINS AND RESISTOR TERMINALS

The AD5259 V_{DD}, V_{LOGIC}, and GND power supplies define the boundary conditions for proper 3-terminal and digital input operation. Supply signals present on Terminal A, Terminal B, and Terminal W that exceed V_{DD} or GND are clamped by the internal forward biased ESD protection diodes (see Figure 42). Digital Input SCL and Digital Input SDA are clamped by ESD protection diodes with respect to V_{LOGIC} and GND as shown in Figure 43.

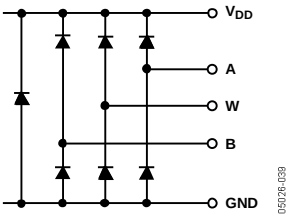

Figure 42. Maximum Terminal Voltages Set by V_{DD} and GND

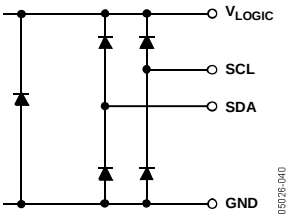

Figure 43. Maximum Terminal Voltages Set by V_{LOGIC} and GND

POWER-UP SEQUENCE

Because the ESD protection diodes limit the voltage compliance at Terminal A, Terminal B, and Terminal W (see Figure 42), it is important to power GND/V_{DD}/V_{LOGIC} before applying any voltage to Terminal A, Terminal B, and Terminal W; otherwise, the diode is forward biased, so the V_{DD} and V_{LOGIC} are powered unintentionally and may affect the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{LOGIC}, digital inputs, and then V_A, V_B, V_W. The relative order of powering V_A, V_B, V_W, and the digital inputs is not important as long as they are powered after GND/V_{DD}/V_{LOGIC}.

LAYOUT AND POWER SUPPLY BYPASSING

It is good practice to use compact, minimum lead length layout design. The leads to the inputs should be as direct as possible with minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with disc or chip ceramic capacitors of 0.01 µF to 0.1 µF. Low ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance and low frequency ripple (see Figure 44). The digital ground should also be joined remotely to the analog ground at one point to minimize the ground bounce.

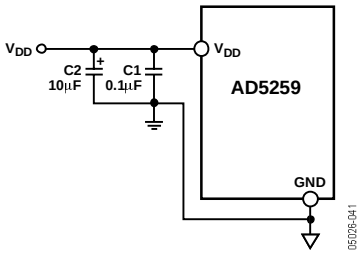

Figure 44. Power Supply Bypassing

MULTIPLE DEVICES ON ONE BUS

The AD5259 has two configurable address pins, Pin AD0 and Pin AD1. The state of these two pins is registered upon power-up and decoded into a corresponding I^2C-compatible 7-bit address (see Table 5). This allows up to four devices on the bus to be written to or read from independently.

EVALUATION BOARD

An evaluation board, with all necessary software, is available to program the AD5259 from any PC running Windows® 98/ 2000/ XP. The graphical user interface, as shown in Figure 45, is straightforward and easy to use. More detailed information is available in the board's user manual.

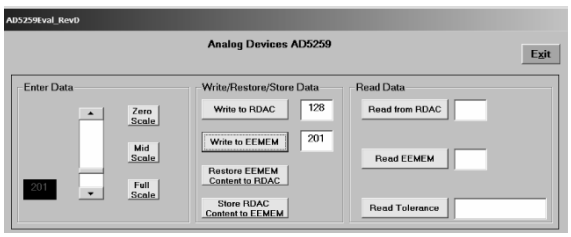

Figure 45. AD5259 Evaluation Board Software

DISPLAY APPLICATIONS

CIRCUITRY

A special feature of the AD5259 is its unique separation of the V_{LOGIC} and V_{DD} supply pins. The separation provides greater flexibility in applications that do not always provide needed supply voltages.

In particular, LCD panels often require a V_{COM} voltage in the range of 3 V to 5 V. The circuit in Figure 46 is the rare exception in which a 5 V supply is available to power the digital potentiometer.

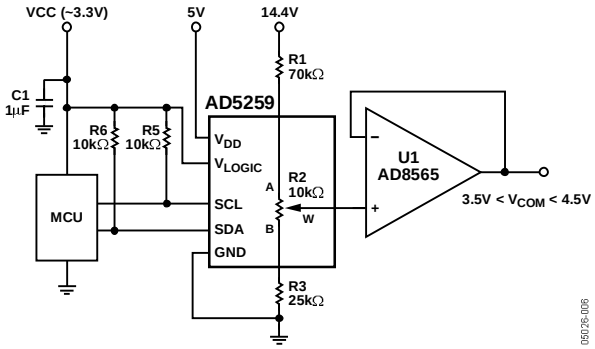

Figure 46. V_{COM} Adjustment Application

In the more common case shown in Figure 47, only analog 14.4 V and digital logic 3.3 V supplies are available. By placing discrete resistors above and below the digital potentiometer, V_{DD} can now be tapped off the resistor string itself. Based on the chosen resistor values, the voltage at V_{DD} in this case equals 4.8 V, allowing the wiper to be safely operated all the way up to 4.8 V. The current draw of V_{DD} will not affect that node's bias because it is only on the order of microamps. V_{LOGIC} is tied to the MCU's 3.3 V digital supply because V_{LOGIC} will draw the 35 mA which is needed when writing to the EEPROM. It would be impractical to try and source 35 mA through the 70 kΩ resistor, therefore, V_{LOGIC} is not connected to the same node as V_{DD}.

For this reason, V_{LOGIC} and V_{DD} are provided as two separate supply pins that can either be tied together or treated independently; V_{LOGIC} supplying the logic/EEPROM with power, and V_{DD} biasing up the A, B, and W terminals for added flexibility.

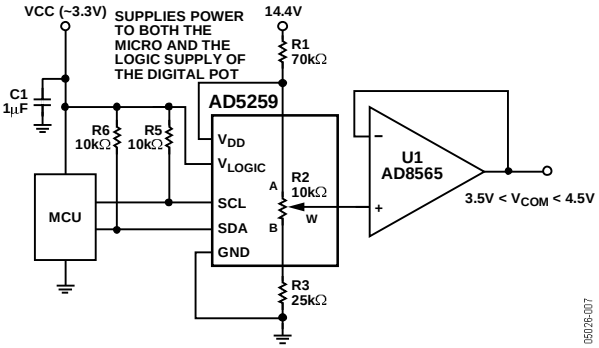

Figure 47. Circuitry When a Separate Supply is Not Available for V_{DD}

For a more detailed look at this application, refer to the article, "Simple VCOM Adjustment uses any Logic Supply Voltage" in the September 30, 2004 issue of *EDN* magazine.

OUTLINE DIMENSIONS

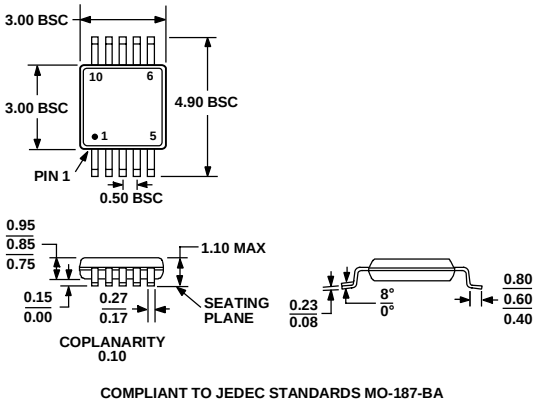

Figure 48. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

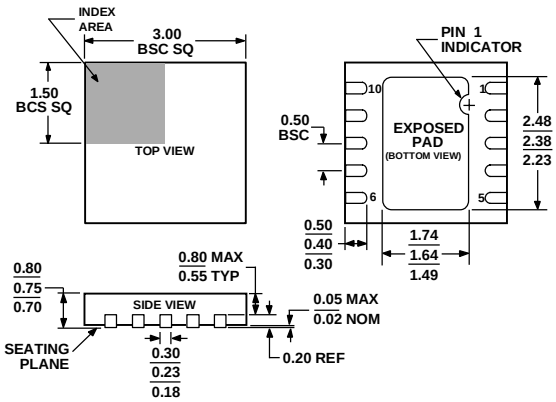

Figure 49. 10-Lead Lead Frame Chip Scale Package [LFCSP_WD]

3 mm × 3 mm Body, Very Very Thin, Dual Lead
(CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model	R_{AB} (Ω)	Temperature	Package Description	Package Option	Branding
AD5259BRMZ5[1]	5 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4P
AD5259BRMZ5-R7[1]	5 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4P
AD5259BCPZ5-R7[1]	5 k	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4P
AD5259BRMZ10[1]	10 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4Q
AD5259BRMZ10-R7[1]	10 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4Q
AD5259BCPZ10-R7[1]	10 k	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4Q
AD5259BRMZ50[1]	50 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4R
AD5259BRMZ50-R7[1]	50 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4R
AD5259BCPZ50-R7[1]	50 k	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4R
AD5259BRMZ100[1]	100 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4S
AD5259BRMZ100-R7[1]	100 k	−40°C to +85°C	10-Lead MSOP	RM-10	D4S
AD5259BCPZ100-R7[1]	100 k	−40°C to +85°C	10-Lead LFCSP_WD	CP-10-9	D4S
AD5259EVAL[2]			Evaluation Board		

[1] Z = Pb-free part.
[2] The evaluation board is shipped with the 10 kΩ R_{AB} resistor option; however, the board is compatible with all available resistor value options.

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