1-/2-Channel 15 V Digital Potentiometers

AD5260/AD5262

FEATURES
256 Positions
AD5260 – 1-Channel
AD5262 – 2-Channel (Independently Programmable)
Potentiometer Replacement
20 kΩ, 50 kΩ, 200 kΩ
Low Temperature Coefficient 35 ppm/°C
4-Wire SPI-Compatible Serial Data Input
5 V to 15 V Single-Supply; ±5.5 V Dual-Supply Operation
Power ON Mid-Scale Preset

APPLICATIONS
Mechanical Potentiometer Replacement
Instrumentation: Gain, Offset Adjustment
Stereo Channel Audio Level Control
Programmable Voltage to Current Conversion
Programmable Filters, Delays, Time Constants
Line Impedance Matching
Low Resolution DAC Replacement

GENERAL DESCRIPTION

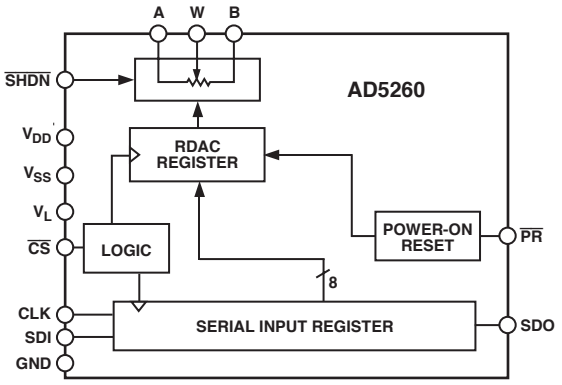
The AD5260/AD5262 provide a single- or dual-channel, 256-position, digitally controlled variable resistor (VR) device.* These devices perform the same electronic adjustment function as a potentiometer or variable resistor. Each channel of the AD5260/AD5262 contains a fixed resistor with a wiper contact that taps the fixed resistor value at a point determined by a digital code loaded into the SPI-compatible serial-input register. The resistance between the wiper and either end point of the fixed resistor varies linearly with respect to the digital code transferred into the VR latch. The variable resistor offers a completely programmable value of resistance, between the A terminal and the wiper or the B terminal and the wiper. The fixed A to B terminal resistance of 20 kΩ, 50 kΩ, or 200 kΩ has a nominal temperature coefficient of 35 ppm/°C. Unlike the majority of the digital potentiometers in the market, these devices can operate up to 15 V or ±5 V provided proper supply voltages are furnished.

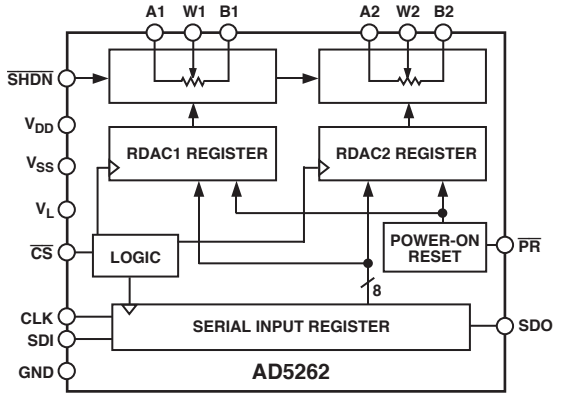
Each VR has its own VR latch, which holds its programmed resistance value. These VR latches are updated from an internal serial-to-parallel shift register, which is loaded from a standard 3-wire serial-input digital interface. The AD5260 contains an 8-bit serial register while the AD5262 contains a 9-bit serial register. Each bit is clocked into the register on the positive edge of the CLK. The AD5262 address bit determines the corresponding VR latch to be loaded with the last 8 bits of the data word during the positive edging of $\overline{CS}$ strobe. A serial data output pin at the opposite end of the serial register enables simple daisy chaining in multiple VR applications without additional external decoding logic. An optional reset pin ($\overline{PR}$) forces the wiper to the mid-scale position by loading 80_H into the VR latch.

*The terms digital potentiometers, VR, and RDAC are used interchangeably.

REV. 0

FUNCTIONAL BLOCK DIAGRAMS





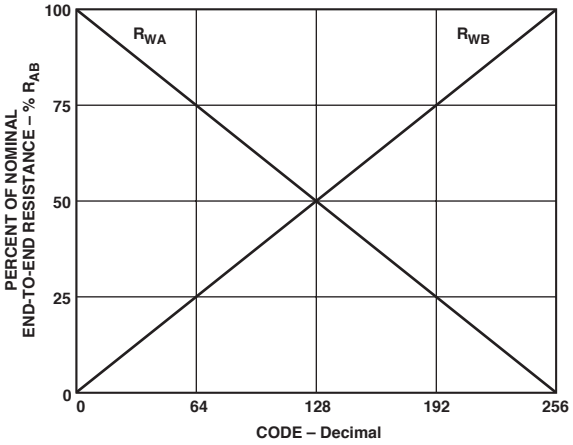


Figure 1. R_{WA} and R_{WB} vs. Code

The AD5260/AD5262 are available in thin surface-mount TSSOP-14 and TSSOP-16 packages. All parts are guaranteed to operate over the extended industrial temperature range of –40°C to +85°C.

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Tel: 781/329-4700 **www.analog.com**
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AD5260/AD5262–SPECIFICATIONS

(V_{DD} = +15 V, V_{SS} = 0 V or, V_{DD} = +5 V, V_{SS} = –5 V, V_L = +5 V, V_A = +5 V, V_B = 0 V, – 40°C < T_A < +85°C unless otherwise noted.)

ELECTRICAL CHARACTERISTICS 20 kΩ, 50 kΩ, 200 kΩ VERSIONS

Parameter	Symbol	Conditions	Min	Typ[1]	Max	Unit
DC CHARACTERISTICS RHEOSTAT MODE Specifications apply to all VRs						
Resistor Differential NL[2]	R-DNL	R_{WB}, V_A = NC	–1	±1/4	+1	LSB
Resistor Nonlinearity[2]	R-INL	R_{WB}, V_A = NC	–1	±1/2	+1	LSB
Nominal Resistor Tolerance[3]	ΔR_{AB}	T_A = 25°C	–30		30	%
Resistance Temperature Coefficient	$\Delta R_{AB}/\Delta T$	Wiper = No Connect		35		ppm/°C
Wiper Resistance	R_W	I_W = 1 V/R_{AB}		60	150	Ω
Channel Resistance Matching (AD5262 only)	$\Delta R_{WB}/R_{WB}$	Ch 1 and 2 R_{WB}, $D_X = 80_H$		0.1		%
Resistance Drift	ΔR_{AB}			0.05		%
DC CHARACTERISTICS POTENTIOMETER DIVIDER MODE Specifications apply to all VRs						
Resolution	N		8			Bits
Differential Nonlinearity[4]	DNL		–1	±1/4	+1	LSB
Integral Nonlinearity[4]	INL		–1	±1/2	+1	LSB
Voltage Divider Temperature Coefficient	$\Delta V_W/\Delta T$	Code = 80_H		5		ppm/°C
Full-Scale Error	V_{WFSE}	Code = FF_H	–2	–1	+0	LSB
Zero-Scale Error	V_{WZSE}	Code = 00_H	0	1	2	LSB
RESISTOR TERMINALS						
Voltage Range[5]	$V_{A, B, W}$		V_{SS}		V_{DD}	V
Capacitance[6] Ax, Bx	$C_{A,B}$	f = 5 MHz, measured to GND, Code = 80_H		25		pF
Capacitance[6] Wx	C_W	f = 1 MHz, measured to GND, Code = 80_H		55		pF
Common-Mode Leakage Current	I_{CM}	V_A = V_B = V_{DD}/2		1		nA
Shut Down Current[7]	I_{SHDN}				5	µA
DIGITAL INPUTS and OUTPUTS						
Input Logic High	V_{IH}		2.4			V
Input Logic Low	V_{IL}				0.8	V
Input Logic High	V_{IH}	V_L = 3 V, V_{SS} = 0 V	2.1			V
Input Logic Low	V_{IL}	V_L = 3 V, V_{SS} = 0 V			0.6	V
Output Logic High (SDO)	V_{OH}	$R_{PULL-UP}$ = 2 kΩ to 5 V	4.9			V
Output Logic Low (SDO)	V_{OL}	I_{OL} = 1.6 mA, V_{LOGIC} = 5 V			0.4	V
Input Current[8]	I_{IL}	V_{IN} = 0 V or 5 V			±1	µA
Input Capacitance[6]	C_{IL}			5		pF
POWER SUPPLIES						
Logic Supply	V_L		2.7		5.5	V
Power Single-Supply Range	$V_{DD\ RANGE}$	V_{SS} = 0 V	4.5		16.5	V
Power Dual-Supply Range	$V_{DD/SS\ RANGE}$		±4.5		±5.5	V
Logic Supply Current	I_L	V_L = 5 V			60	µA
Positive Supply Current	I_{DD}	V_{IH} = 5 V or V_{IL} = 0 V			1	µA
Negative Supply Current	I_{SS}	V_{SS} = –5 V			1	µA
Power Dissipation[9]	P_{DISS}	V_{IH} = 5 V or V_{IL} = 0 V, V_{DD} = +5 V, V_{SS} = –5 V			0.3	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = +5 V, ±10%		0.003	0.01	%/%
DYNAMIC CHARACTERISTICS[6, 10]						
Bandwidth –3 dB	BW	R_{AB} = 20 kΩ/50 kΩ/200 kΩ		310/130/30		kHz
Total Harmonic Distortion	THD_W	V_A = 1 V_{RMS}, V_B = 0 V, f = 1 kHz, R_{AB} = 20 kΩ		0.014		%
V_W Settling Time	t_S	V_A = +5 V, V_B = –5 V, ±1 LSB error band, R_{AB} = 20 kΩ		5		µs
Crosstalk[11]	C_T	V_A = V_{DD}, V_B = 0 V, Measure V_W with Adjacent RDAC Making Full-Scale Code Change (AD5262 only)		1		nV–s
Analog Crosstalk	C_{TA}	V_{A1} = V_{DD}, V_{B1} = 0V, Measure V_{W1} with V_{W2} = 5 V p-p @ f = 10 kHz, R_{AB} = 20 kΩ/200 kΩ (AD5262 only)		–64		dB
Resistor Noise Voltage	e_{N_WB}	R_{WB} = 20 kΩ f = 1 kHz		13		nV/√Hz

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INTERFACE TIMING CHARACTERISTICS apply to all parts[6, 12]						
Clock Frequency	f_{CLK}				25	MHz
Input Clock Pulsewidth	t_{CH}, t_{CL}	Clock level high or low	20			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns
$\overline{CLK}$ to SDO Propagation Delay[13]	t_{PD}	R_L = 1 kΩ, C_L < 20pF	1		160	ns
$\overline{CS}$ Setup Time	t_{CSS}		5			ns
$\overline{CS}$ High Pulsewidth	t_{CSW}		20			ns
Reset Pulsewidth	t_{RS}		50			ns
$\overline{CLK}$ Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
$\overline{CS}$ Rise to Clock Rise Setup	t_{CS1}		10			ns

NOTES

The AD5260/AD5262 contains 1,968 transistors. Die Size: 89 mil. × 105 mil. 9,345 sq. mil.

[1] Typicals represent average readings at 25°C and V_{DD} = +5 V, V_{SS} = –5 V.

[2] Resistor position nonlinearity error R-INL is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic. $I_W = V_{DD}/R$ for both V_{DD} = +5 V, V_{SS} = –5 V.

[3] $V_{AB} = V_{DD}$, Wiper (V_W) = No connect.

[4] INL and DNL are measured at V_W with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter. VA = V_{DD} and V_B = 0V. DNL specification limits of ±1 LSB maximum are Guaranteed Monotonic operating conditions.

[5] Resistor terminals A, B, W have no limitations on polarity with respect to each other.

[6] Guaranteed by design and not subject to production test.

[7] Measured at the Ax terminals. All Ax terminals are open-circuit in shutdown mode.

[8] Worst-case supply current consumed when input all logic-input levels set at 2.4 V, standard characteristic of CMOS logic.

[9] P_{DISS} is calculated from ($I_{DD} \times V_{DD}$). CMOS logic level inputs result in minimum power dissipation.

[10] All dynamic characteristics use V_{DD} = +5 V, V_{SS} = –5 V, V_L = +5 V.

[11] Measured at a V_W pin where an adjacent V_W pin is making a full-scale voltage change.

[12] See timing diagram for location of measured values. All input control voltages are specified with $t_R = t_F$ = 2ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V. Switching characteristics are measured using V_L = 5 V.

[13] Propagation delay depends on value of V_{DD}, R_L, and C_L.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND ..... –0.3 V, +15 V
V_{SS} to GND ..... 0 V, –7 V
V_{DD} to V_{SS} ..... 15 V
V_A, V_B, V_W to GND ..... V_{SS}, V_{DD}
$A_X - B_X$, $A_X - W_X$, $B_X - W_X$
  Intermittent[2] ..... ±20 mA
  Continuous ..... ±5 mA
Digital Inputs and Output Voltage to GND ..... 0 V, 7 V
Operating Temperature Range ..... –40°C to +85°C
Maximum Junction Temperature ($T_{J\,MAX}$) ..... 150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
  Vapor Phase (60 sec) ..... 215°C
  Infrared (15 sec) ..... 220°C
Thermal Resistance[3] θ_{JA}
  TSSOP-14 ..... 206°C/W
  TSSOP-16 ..... 150°C/W

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance setting.

[3] Package Power Dissipation = $(T_{J\,MAX} - T_A)/\theta_{JA}$

ORDERING GUIDE

Model	R_{AB} (kΩ)	Temperature	Package Description	Package Option	No. of Parts per Container	Branding Information*
AD5260BRU20	20	–40°C to +85°C	TSSOP-14	RU-14	96	AD5260B20
AD5260BRU20-REEL7	20	–40°C to +85°C	TSSOP-14	RU-14	1000	AD5260B20
AD5260BRU50	50	–40°C to +85°C	TSSOP-14	RU-14	96	AD5260B50
AD5260BRU50-REEL7	50	–40°C to +85°C	TSSOP-14	RU-14	1000	AD5260B50
AD5260BRU200	200	–40°C to +85°C	TSSOP-14	RU-14	96	AD5260B200
AD5260BRU200-REEL7	200	–40°C to +85°C	TSSOP-14	RU-14	1000	AD5260B200
AD5262BRU20	20	–40°C to +85°C	TSSOP-16	RU-16	96	AD5262B20
AD5262BRU20-REEL7	20	–40°C to +85°C	TSSOP-16	RU-16	1000	AD5262B20
AD5262BRU50	50	–40°C to +85°C	TSSOP-16	RU-16	96	AD5262B50
AD5262BRU50-REEL7	50	–40°C to +85°C	TSSOP-16	RU-16	1000	AD5262B50
AD5262BRU200	200	–40°C to +85°C	TSSOP-16	RU-16	96	AD5262B200
AD5262BRU200-REEL7	200	–40°C to +85°C	TSSOP-16	RU-16	1000	AD5262B200

*Line 1 contains part number, line 2 contains differentiating detail by part type and ADI logo symbol, line 3 contains date code YWW.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD5260/AD5262 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. AD5260 8-Bit Serial-Data Word Format

DATA							
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
D7	D6	D5	D4	D3	D2	D1	D0
MSB							LSB
2^7							2^0

Table II. AD5262 9-Bit Serial-Data Word Format

ADDR	DATA							
B8	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
A0	D7	D6	D5	D4	D3	D2	D1	D0
	MSB							LSB
2^8	2^7							2^0

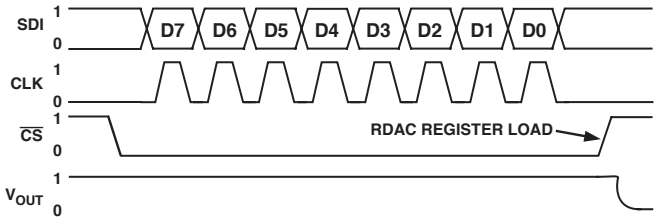


Figure 2a. AD5260 Timing Diagram

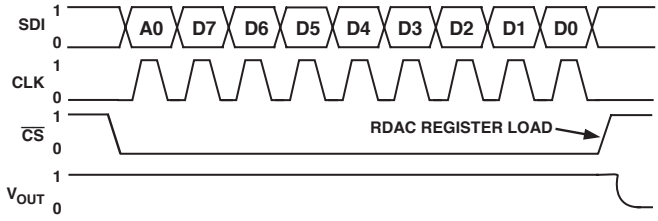


Figure 2b. AD5262 Timing Diagram

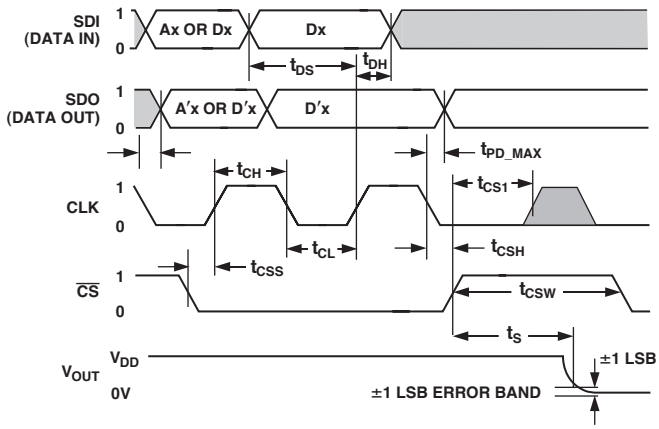


Figure 2c. Detail Timing Diagram

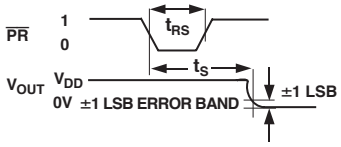
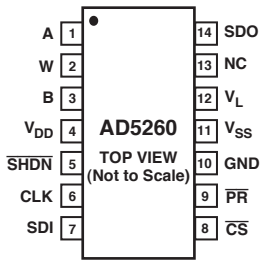
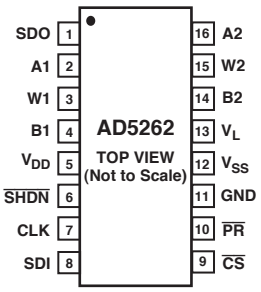


Figure 2d. Preset Timing Diagram

AD5260 PIN CONFIGURATION



AD5262 PIN CONFIGURATION



AD5260 PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1	A	A Terminal
2	W	Wiper Terminal
3	B	B Terminal
4	V_{DD}	Positive power supply, specified for operation at both 5 V or 15 V. (Sum of $\|V_{DD}\| + \|V_{SS}\| \le 15$ V)
5	$\overline{SHDN}$	Active low input. Terminal A open-circuit. Shutdown controls. Variable Resistors of RDAC.
6	CLK	Serial Clock Input, positive edge triggered.
7	SDI	Serial Data Input
8	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data will be loaded into the RDAC register.
9	$\overline{PR}$	Active low preset to mid-scale; sets RDAC registers to 80_H.
10	GND	Ground
11	V_{SS}	Negative Power Supply, specified for operation from 0 V to –5 V.
12	V_L	Logic Supply Voltage, needs to be same voltage as the digital logic controlling the AD5260.
13	NC	No Connect (Users should not connect anything other than dummy pad on this pin)
14	SDO	Serial Data Output, Open Drain transistor requires pull-up resistor.

AD5262 PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1	SDO	Serial Data Output, Open Drain transistor requires pull-up resistor.
2	A1	A Terminal RDAC #1
3	W1	Wiper RDAC #1, address A0 = 0_2
4	B1	B Terminal RDAC #1
5	V_{DD}	Positive power supply, specified for operation at both 5 V or 15 V. (Sum of $\|V_{DD}\|+\|V_{SS}\| \le 15$ V)
6	$\overline{SHDN}$	Active low input. Terminal A open-circuit. Shutdown controls Variable Resistors #1 through #2.
7	CLK	Serial Clock Input, positive edge triggered.
8	SDI	Serial Data Input.
9	$\overline{CS}$	Chip Select Input, Active Low. When $\overline{CS}$ returns high, data in the serial input register is decoded, based on the address Bit A_0, and loaded into the target RDAC register.
10	$\overline{PR}$	Active low preset to mid-scale sets RDAC registers to 80_H.
11	GND	Ground
12	V_{SS}	Negative Power Supply, specified for operation at both 0 V or –5 V (Sum of $\|V_{DD}\| + \|V_{SS}\| < 15$ V).
13	V_L	Logic Supply Voltage, needs to be same voltage as the digital logic controlling the AD5262.
14	B2	B Terminal RDAC #2
15	W2	Wiper RDAC #2, address A0 = 1_2
16	A2	A Terminal RDAC #2

THEORY OF OPERATION

The AD5260/AD5262 provide a single- or dual-channel, 256-position digitally controlled variable resistor (VR) device and operate up to 15 V maximum voltage. Changing the programmed VR settings is accomplished by clocking an 8-/9-bit serial data word into the SDI (Serial Data Input) pin. For the AD5262, the format of this data word is one address bit. A0 represents the first bit B8, then followed by eight data bits B7–B0 with MSB first. Tables I and II provide the serial register data word format. See Table III for the AD5262 address assignment to decode the location of the VR latch receiving the serial register data in bits B7 through B0. VR outputs can be changed one at a time in random sequence. The AD5260/AD5262 presets to a mid-scale, simplifying fault condition recovery at power-up. Mid-scale can also be achieved at any time by asserting the $\overline{PR}$ pin. Both parts have an internal power ON preset that places the wiper in a mid-scale preset condition at power ON. Operation of the power ON preset function depends only on the state of the V_L pin.

The AD5260/AD5262 contains a power shutdown $\overline{SHDN}$ pin, which places the RDAC in an almost zero power consumption state where terminals Ax are open circuited, and the wiper W is connected to B, resulting in only leakage currents being consumed in the VR structure. In the shutdown mode, the VR latch settings are maintained so that, returning to operational mode from power shutdown, the VR settings return to their previous resistance values.

Table III. AD5262 Address Decode Table

A0	Latch Loaded
0	RDAC#1
1	RDAC#2

DIGITAL INTERFACING

The AD5260/AD5262 contains a 4-wire SPI-compatible digital interface (SDI, SDO, $\overline{CS}$, and CLK). For the AD5260, the 8-bit serial word must be loaded with MSB first, and the format of the word is shown in Table I. For the AD5262, the 9-bit serial word must be loaded with address bit A0 first, then MSB of the data. The format of the word is shown in Table II.

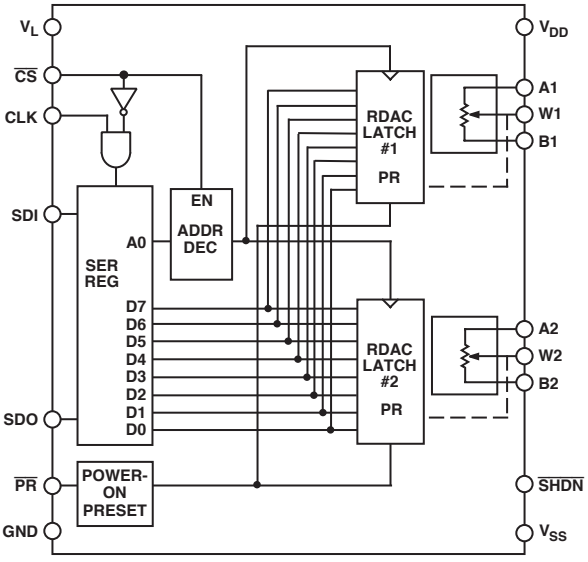


Figure 3. AD5262 Block Diagram

The positive-edge sensitive CLK input requires clean transitions to avoid clocking incorrect data into the serial input register. Standard logic families work well. If mechanical switches are used for product evaluation, they should be debounced by a flip-flop or other suitable means. Figure 3 shows more detail of the internal digital circuitry. When $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge (see Table IV).

Table IV. Truth Table

CLK	$\overline{CS}$	$\overline{PR}$	$\overline{SHDN}$	Register Activity
L	L	H	H	No SR effect, enables SDO pin
↑*	L	H	H	Shift one bit in from the SDI pin. The eighth previously entered bit is shifted out of the SDO pin.
X	↑	H	H	Load SR data into RDAC latch
X	H	H	H	No Operation
X	X	L	H	Sets all RDAC latches to Mid-Scale, wiper centered, and SDO latch cleared.
X	H	↑	H	Latches all RDAC latches to 80_H.
X	H	H	L	Open circuits all resistor A–terminals, connects W to B, turns off SDO output transistor.

*↑ = positive edge, X = don't care, SR = shift register

The data setup and data hold times in the specification table determine the data valid time requirements. The AD5260 uses an 8-bit serial input data register word that is transferred to the internal RDAC register when the $\overline{CS}$ line returns to logic high. For the AD5262 the last 9 bits of the data word entered into the serial register are held when $\overline{CS}$ returns high. Any extra bits are ignored. At the same time $\overline{CS}$ goes high, it gates the address decoder enabling AD5262 one of two positive edge-triggered AD5262 RDAC latches (see Figure 4).

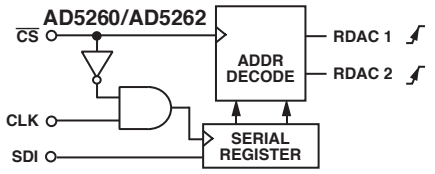


Figure 4. Equivalent Input Control Logic

The target RDAC latch is loaded with the last 8 bits of the serial data word completing one RDAC update. For the AD5262, two separate 9-bit data words must be clocked in to change both VR settings.

During shutdown ($\overline{SHDN}$) the SDO output pin is forced to the off (logic high state) to disable power dissipation in the pull-up resistor. See Figure 5 for equivalent SDO output circuit schematic.

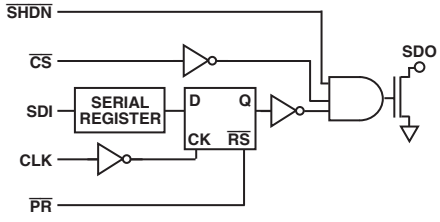


Figure 5. Detail SDO Output Schematic of the AD5260

All digital inputs are protected with a series input resistor and parallel Zener ESD structure as shown in Figure 6. This applies to digital input pins $\overline{CS}$, SDI, SDO, $\overline{PR}$, $\overline{SHDN}$, and CLK.

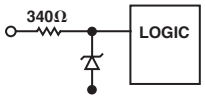


Figure 6. ESD Protection of Digital Pins

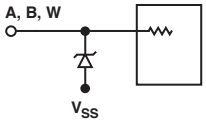


Figure 7. ESD Protection of Resistor Terminals

LAYOUT AND POWER SUPPLY BYPASSING

It is a good practice to employ compact, minimum-lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance.

Similarly, it is also a good practice to bypass the power supplies with quality capacitors for optimum stability. Supply leads to the device should be bypassed with 0.01 µF–0.1 µF disc or chip ceramics capacitors. Low-ESR 1 µF to 10 µF tantalum or electrolytic capacitors should also be applied at the supplies to minimize any transient disturbance (see Figure 8). Notice the digital ground should also be joined remotely to the analog ground to minimize the ground bounce.

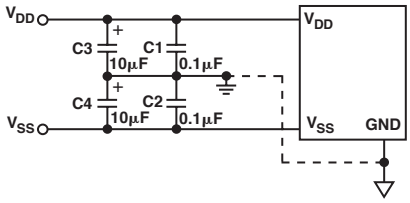


Figure 8. Power Supply Bypassing

TERMINAL VOLTAGE OPERATING RANGE

The AD5260/AD5262 positive V_{DD} and negative V_{SS} power supply defines the boundary conditions for proper 3-terminal digital potentiometer operation. Supply signals present on terminals A, B, and W that exceed V_{DD} or V_{SS} will be clamped by the internal forward biased diodes (see Figure 9).

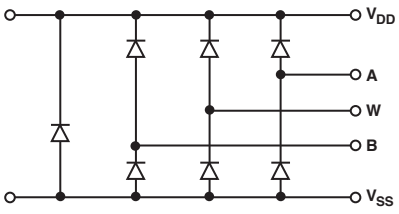


Figure 9. Maximum Terminal Voltages Set by V_{DD} and V_{SS}

The ground pin of the AD5260/AD5262 device is primarily used as a digital ground reference, which needs to be tied to the PCB's common ground. The digital input control signals to the AD5260/AD5262 must be referenced to the device ground pin (GND), and must satisfy the logic level defined in the specification table of this data sheet. An internal level shift circuit ensures that the common-mode voltage range of the three terminals extends from V_{SS} to V_{DD} regardless of the digital input level.

POWER-UP SEQUENCE

Since there are diodes to limit the voltage compliance at terminals A, B, and W (see Figure 9), it is important to power V_{DD}/V_{SS} first before applying any voltage to terminals A, B, and W. Otherwise, the diode will be forward biased such that V_{DD}/V_{SS} will be powered unintentionally and may affect the rest of the user's circuit. The ideal power-up sequence is in the following order: GND, V_{DD}, V_{SS}, V_L, Digital Inputs, and $V_{A/B/W}$. The order of powering V_A, V_B, V_W, and Digital Inputs is not important as long as they are powered after V_{DD}/V_{SS}.

Daisy-Chain Operation

The serial-data output (SDO) pin contains an open drain n-channel FET. This output requires a pull-up resistor to transfer data to the next package's SDI pin. This allows for daisy chaining several RDACs from a single processor serial data line. The pull-up resistor termination voltage can be larger than the V_{DD} supply voltage. It is recommended to increase the Clock period when using a pull-up resistor to the SDI pin of the following device in series because capacitive loading at the daisy-chain node SDO-SDI between devices may induce time delay to subsequent devices. Users should be aware of this potential problem to achieve data transfer successfully (see Figure 10). If two AD5260s are daisy-chained, this requires a total of 16 bits of data. The first 8 bits, complying with the format shown in Table I, go to U2, and the second 8 bits with the same format go to U1. The $\overline{CS}$ should be kept low until all 16 bits are clocked into their respective serial registers, and the $\overline{CS}$ is then pulled high to complete the operation.

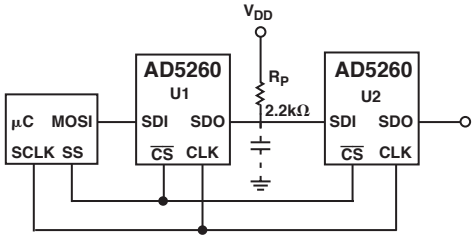


Figure 10. Daisy-Chain Configuration

RDAC STRUCTURE

The RDAC contains a string of equal resistor segments, with an array of analog switches, that act as the wiper connection. The number of positions is the resolution of the device. The AD5260/AD5262 have 256 connection points allowing it to provide better than 0.4% set-ability resolution. Figure 11 shows an equivalent structure of the connections between the three terminals that make up one channel of the RDAC. The SW_A and SW_B will always be ON, while one of the switches SW(0) to SW($2^N - 1$) will be ON one at a time depending on the resistance position decoded from the data bits. Since the switch is not ideal, there is a 60 Ω wiper resistance, R_W. Wiper resistance is a function of supply voltage and temperature. The lower the supply voltage, the higher the wiper resistance. Similarly, the higher the temperature, the higher the wiper resistance. Users should be aware of the contribution of the wiper resistance when accurate prediction of the output resistance is needed.

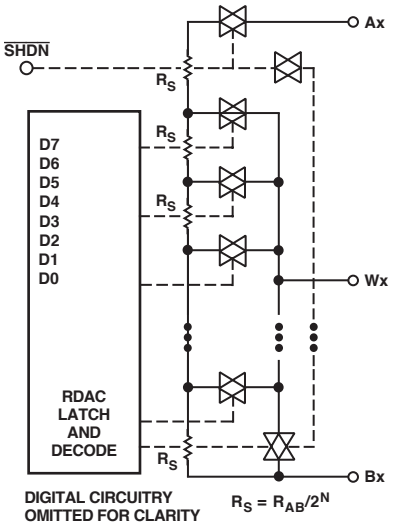


Figure 11. Simplified RDAC Architecture

PROGRAMMING THE VARIABLE RESISTOR

Rheostat Operation

The nominal resistances of the RDAC between terminals A and B are available with values of 20 kΩ, 50 kΩ, and 200 kΩ. The final three digits of the part number determine the nominal resistance value, e.g., 20 kΩ = 20; 50 kΩ = 50; 200 kΩ = 200. The nominal resistance (R_{AB}) of the VR has 256 contact points accessed by the wiper terminal, plus the B terminal contact. The 8-bit data in the RDAC latch is decoded to select one of the 256 possible settings. Assuming a 20 kΩ part is used, the wiper's first connection starts at the B terminal for data 00_H. Since there is a 60 Ω wiper contact resistance, such connection yields a minimum of 60 Ω resistance between terminals W and B. The second connection is the first tap point corresponds to 138 Ω (R_{WB} = R_{AB}/256 + R_W = 78 Ω + 60 Ω) for data 01_H. The third connection is the next tap point representing 216 Ω (78 × 2 + 60) for data 02_H and so on. Each LSB data value increase moves the wiper up the resistor ladder until the last tap point is reached at 19982 Ω [R_{AB} − 1 LSB + R_W]. The wiper does not directly connect to the B terminal. See Figure 11 for a simplified diagram of the equivalent RDAC circuit.

The general equation determining the digitally programmed output resistance between W and B is:

$$R_{WB}(D) = \frac{D}{256} \times R_{AB} + R_W \quad (1)$$

where D is the decimal equivalent of the binary code which is loaded in the 8-bit RDAC register, and R_{AB} is the nominal end-to-end resistance.

For example, R_{AB} = 20 kΩ, when V_B = 0 V and A–terminal is open circuit, the following output resistance values R_{WB} will be set for the following RDAC latch codes. The result will be the same if terminal A is tied to W:

D (DEC)	R_{WB} (Ω)	Output State
256	19982	Full-Scale (R_{AB} – 1 LSB + R_W)
128	10060	Mid-Scale
1	138	1 LSB
0	60	Zero-Scale (wiper contact resistance)

Note that in the zero-scale condition a finite wiper resistance of 60 Ω is present. Care should be taken to limit the current flow between W and B in this state to no more than 20 mA to avoid degradation or possible destruction of the internal switches.

Like the mechanical potentiometer the RDAC replaces, the AD5260/AD5262 parts are totally symmetrical. The resistance between the wiper W and terminal A also produces a digitally controlled complementary resistance R_{WA}. Figure 12 shows the symmetrical programmability of the various terminal connections. When R_{WA} is used, the B–terminal can be let floating or tied to the wiper. Setting the resistance value for R_{WA} starts at a maximum value of resistance and decreases as the data loaded in the latch is increased in value. The general equation for this operation is:

$$R_{WA}(D) = \frac{256 - D}{256} \times R_{AB} + R_W \quad (2)$$

For example, R_{AB} = 20 kΩ, when V_A = 0 V and B–terminal is open, the following output resistance R_{WA} will be set for the following RDAC latch codes. The result will be the same if terminal B is tied to W:

D (DEC)	R_{WA} (Ω)	Output State
256	60	Full-Scale
128	10060	Mid-Scale
1	19982	1 LSB
0	20060	Zero-Scale

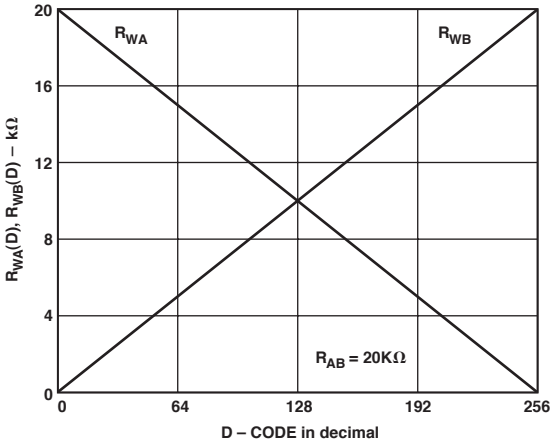
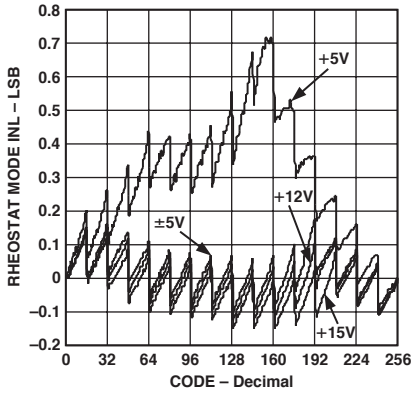


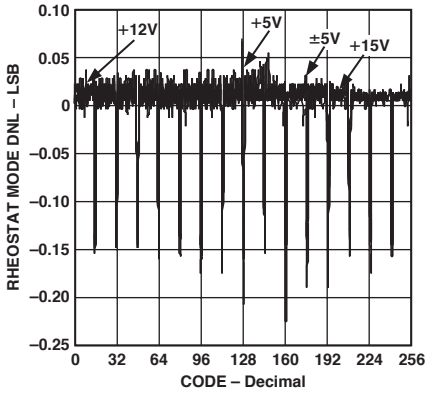
Figure 12. AD5260/AD5262 Equivalent RDAC Circuit

The typical distribution of the nominal resistance R_{AB} from channel to channel matches within ±1%. Device-to-device matching is process lot dependent with the worst case of ±30% variation. On the other hand, since the resistance element is processed in thin film technology, the change in R_{AB} with temperature has a low 35 ppm/°C temperature coefficient.

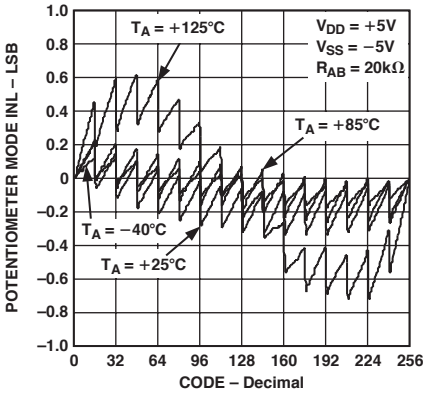
AD5260/AD5262—Typical Performance Characteristics



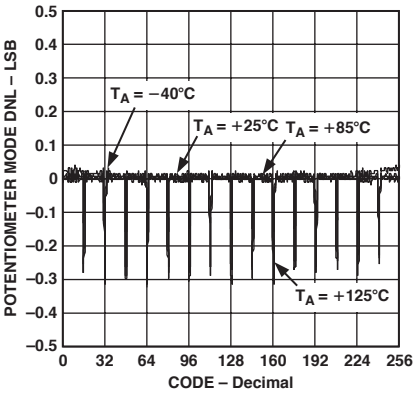
TPC 1. R-INL vs. Code vs. Supply Voltages



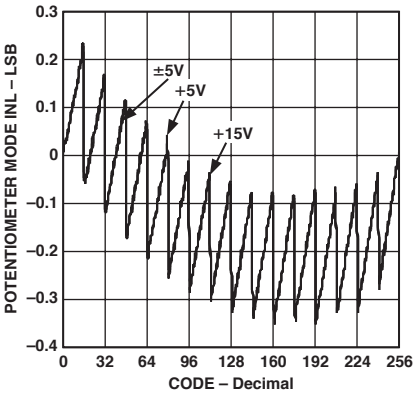
TPC 2. R-DNL vs. Code vs. Supply Voltages



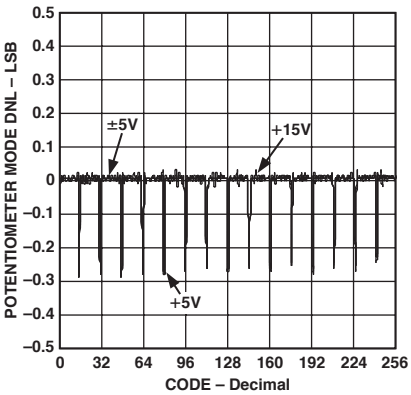
TPC 3. INL vs. Code, V_{DD}/V_{SS} = ±5 V



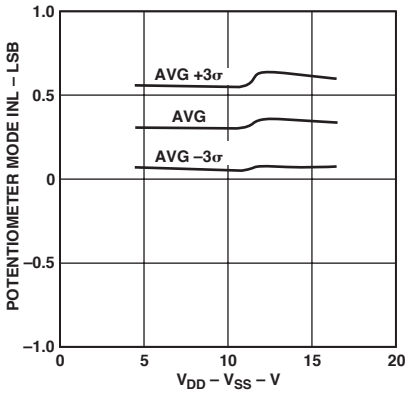
TPC 4. DNL vs. Code, V_{DD}/V_{SS} = ±5 V



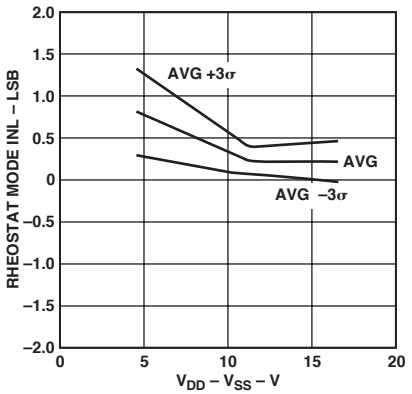
TPC 5. INL vs. Code vs. Supply Voltages



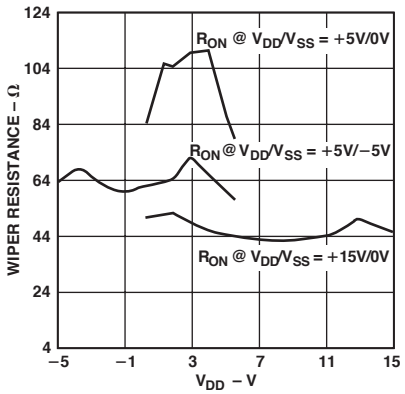
TPC 6. DNL vs. Code vs. Supply Voltages



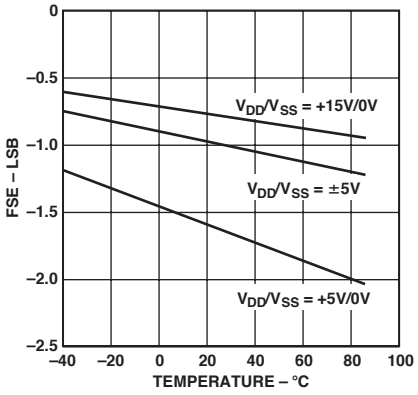
TPC 7. INL vs. Supply Voltages



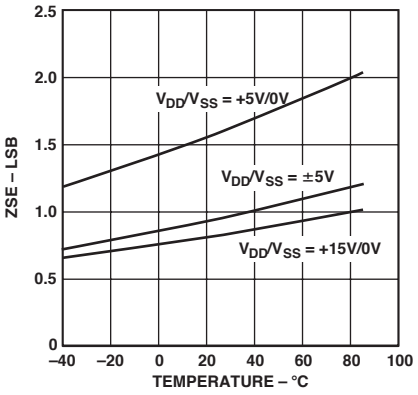
TPC 8. R-INL vs. Supply Voltages



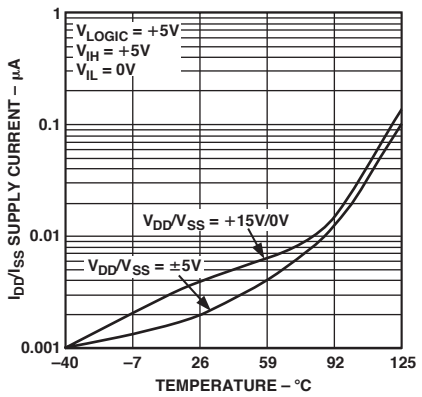
TPC 9. Wiper ON Resistance vs. Bias Voltage



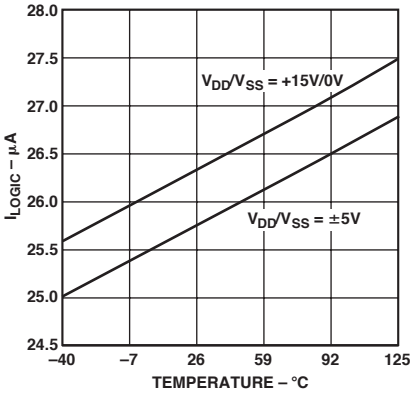
TPC 10. Full-Scale Error



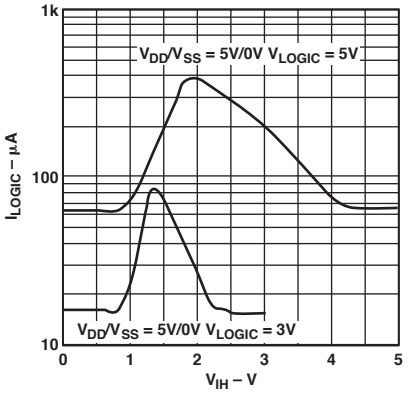
TPC 11. Zero-Scale Error



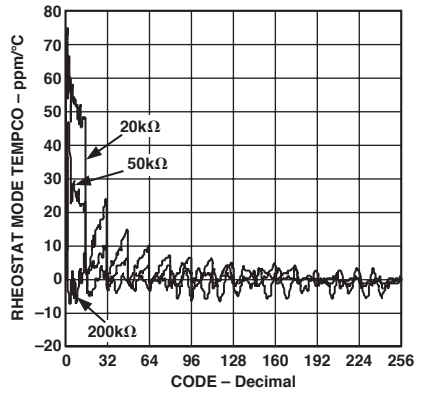
TPC 12. Supply Current vs. Temperature



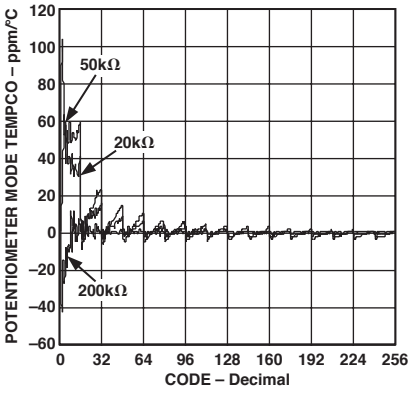
TPC 13. I_{LOGIC} vs. Temperature



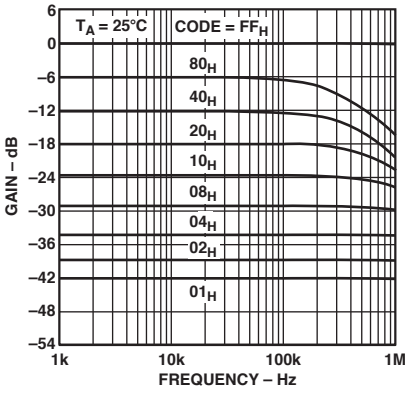
TPC 14. I_{LOGIC} vs. Digital Input Voltage



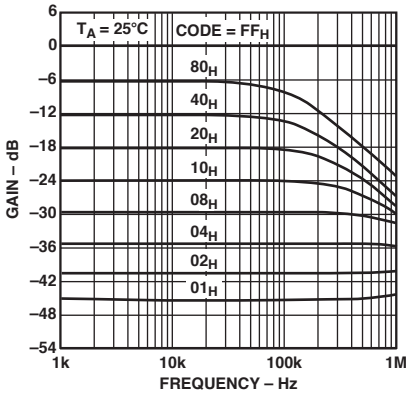
TPC 15. Rheostat Mode Tempco $\Delta R_{WB}/\Delta T$ vs. Code



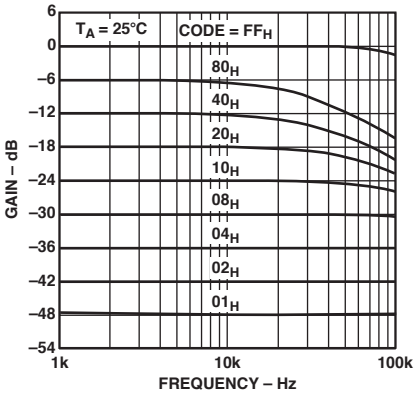
TPC 16. Potentiometer Mode $\Delta V_{WB}/\Delta T$ vs. Code



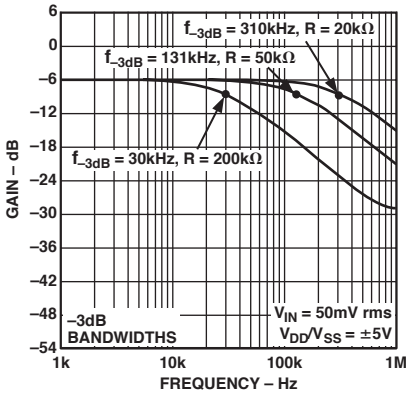
TPC 17. Gain vs. Frequency vs. Code, R_{AB} = 20 kΩ



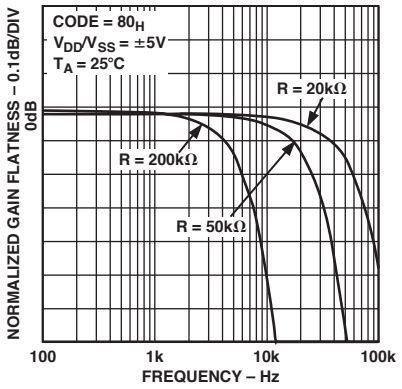
TPC 18. Gain vs. Frequency vs. Code R_{AB} = 50 kΩ



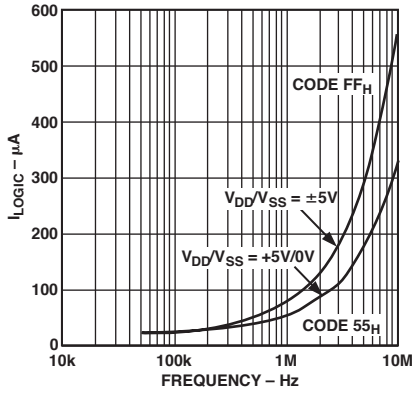
TPC 19. Gain vs. Frequency vs. Code R_{AB} = 200 kΩ



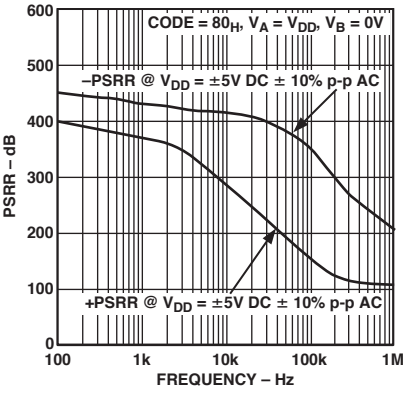
TPC 20. –3 dB Bandwidth



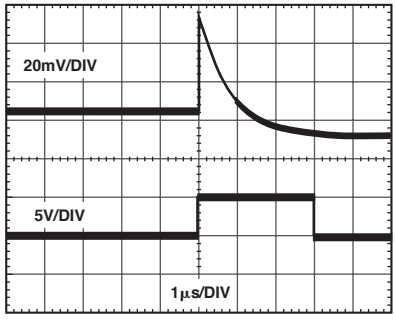
TPC 21. Normalized Gain Flatness vs. Frequency



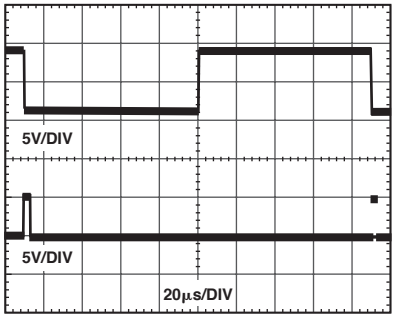
TPC 22. I_{LOGIC} vs. Frequency



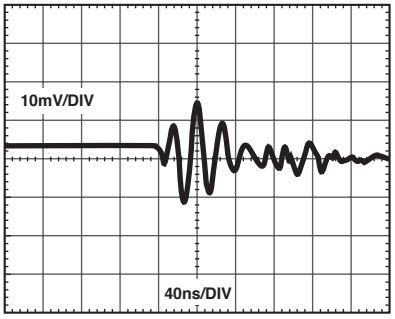
TPC 23. PSRR vs. Frequency



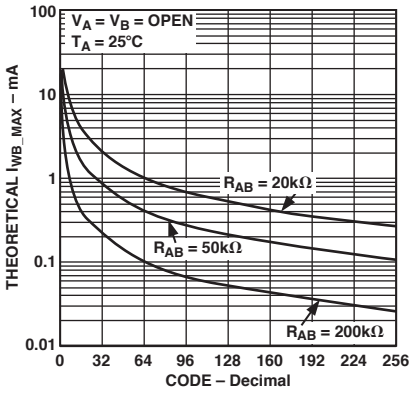
TPC 24. Mid-Scale Glitch Energy, Code 80_H to $7F_H$



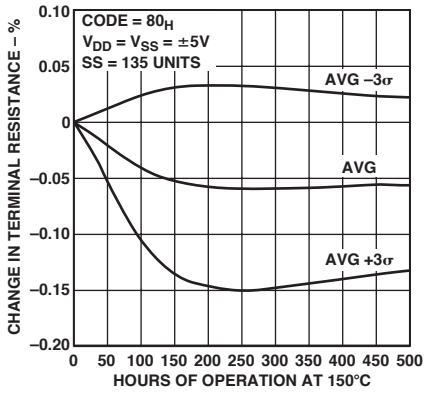
TPC 25. Large Signal Settling Time



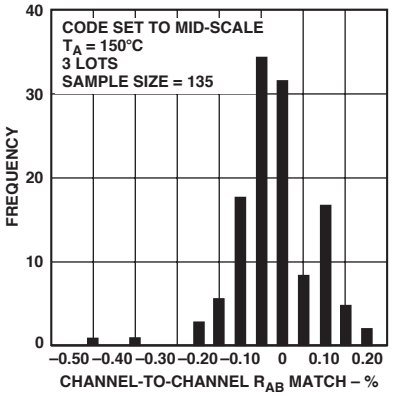
TPC 26. Digital Feedthrough vs. Time



TPC 27. I_{MAX} vs. Code



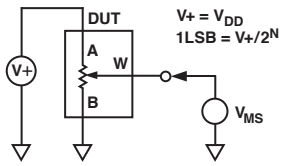
TPC 28. Long-Term Resistance Drift



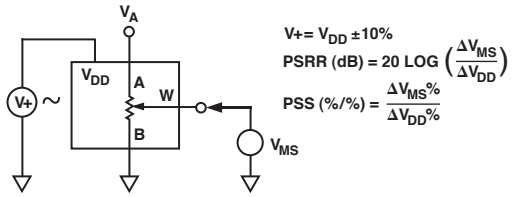
TPC 29. Channel-to-Channel Resistance Matching (AD5262)

TEST CIRCUITS

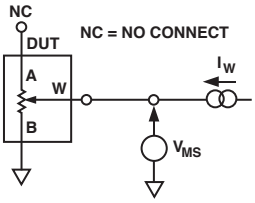
Test Circuits 1 to 9 define the test conditions used in the product specification table.



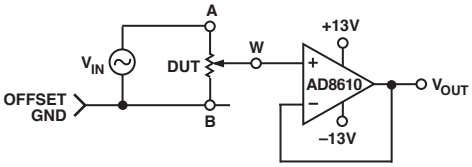
Test Circuit 1. Potentiometer Divider Nonlinearity Error (INL, DNL)



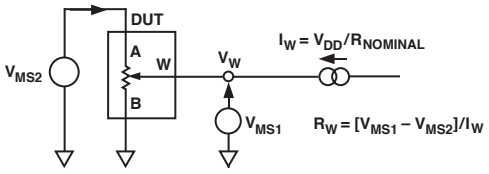
Test Circuit 4. Power Supply Sensitivity (PSS, PSSR)



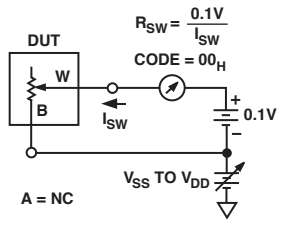
Test Circuit 2. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)



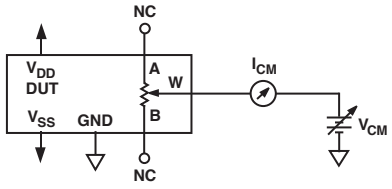
Test Circuit 5. Gain vs. Frequency



Test Circuit 3. Wiper Resistance

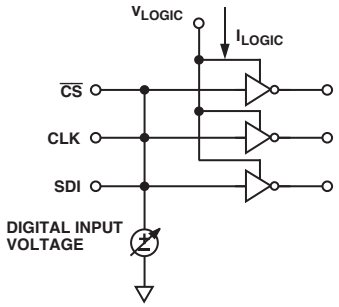


Test Circuit 6. Incremental ON Resistance

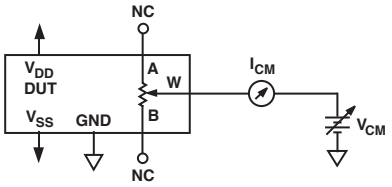


Test Circuit 7. Common-Mode Leakage Current

TEST CIRCUITS (continued)



Test Circuit 8. V_{LOGIC} Current vs. Digital Input Voltage



Test Circuit 9. Analog Crosstalk

PROGRAMMING THE POTENTIOMETER DIVIDER

Voltage Output Operation

The digital potentiometer easily generates output voltages at wiper-to-B and wiper-to-A to be proportional to the input voltage at A-to-B. Ignore the effect of the wiper resistance at the moment. For example, connecting A-terminal to 5 V and B-terminal to ground produces an output voltage at the wiper-to-B starting at zero volts up to 1 LSB less than 5 V. Each LSB of voltage is equal to the voltage applied across terminal AB divided by the 256 position of the potentiometer divider. Since the AD5260/AD5262 operates from dual supplies, the general equation defining the output voltage at V_W with respect to ground for any given input voltage applied to terminals AB is:

$$V_W(D) = \frac{D}{256} \times V_{AB} + V_B \quad (3)$$

Operation of the digital potentiometer in the divider mode results in more accurate operation over temperature. Unlike the rheostat mode, the output voltage is dependent on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values; therefore, the drift reduces to 5 ppm/°C.

APPLICATIONS

Bipolar DC or AC Operation from Dual Supplies

The AD5260/AD5262 can be operated from dual supplies enabling control of ground referenced AC signals or bipolar operation. The AC signal, as high as V_{DD}/V_{SS}, can be applied directly across terminals A–B with output taken from terminal W. See Figure 13 for a typical circuit connection.

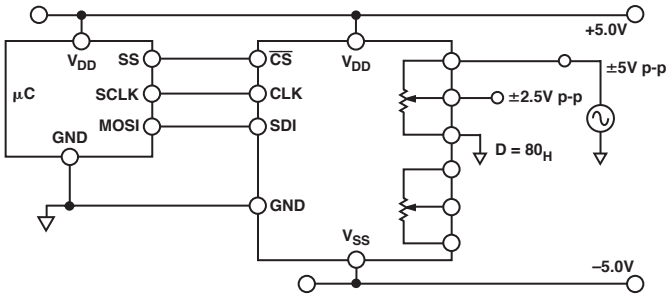


Figure 13. Bipolar Operation from Dual Supplies

Gain Control Compensation

Digital potentiometers are commonly used in gain control as in the noninverting gain amplifier shown in Figure 14.

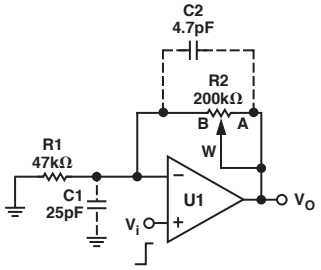


Figure 14. Typical Noninverting Gain Amplifier

Notice that when the RDAC B terminal parasitic capacitance is connected to the op amp noninverting node, it introduces a zero for the $1/\beta_O$ term with +20 dB/dec, whereas a typical op amp GBP has –20 dB/dec characteristics. A large R2 and finite C1 can cause this Zero's frequency to fall well below the crossover frequency. Hence the rate of closure becomes 40 dB/dec and the system has 0° phase margin at the crossover frequency. The output may ring or oscillate if the input is a rectangular pulse or step function. Similarly, it is also likely to ring when switching between two gain values because this is equivalent to a step change at the input.

Depending on the op amp GBP, reducing the feedback resistor may extend the Zero's frequency far enough to overcome the problem. A better approach, however, is to include a compensation capacitor C2 to cancel the effect caused by C1. Optimum compensation occurs when R1 × C1 = R2 × C2. This is not an option because of the variation of R2. As a result, one may use the relationship above and scale C2 as if R2 is at its maximum value. Doing so may overcompensate and compromise the performance slightly when R2 is set at low values. However, it will avoid the ringing or oscillation at the worst case. For critical applications, C2 should be found empirically to suit the need. In general, C2 in the range of a few pF to no more than a few tenths of pF is usually adequate for the compensation.

Similarly, there are W and A terminal capacitances connected to the output (not shown). Fortunately their effect at this node is less significant, and the compensation can be avoided in most cases.

Programmable Voltage Reference

For voltage divider mode operation, Figure 15, it is common to buffer the output of the digital potentiometer unless the load is much larger than R_{WB}. Not only does the buffer serve the purpose of impedance conversion, but it also allows a heavier load to be driven.

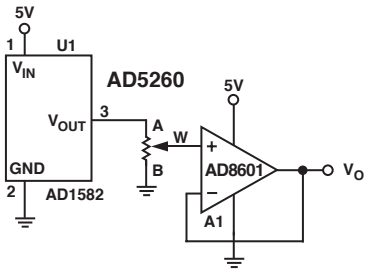


Figure 15. Programmable Voltage Reference

8-Bit Bipolar DAC

Figure 16 shows a low cost 8-bit bipolar DAC. It offers the same number of adjustable steps but not the precision of conventional DACs. The linearity and temperature coefficients, especially at low values codes, are skewed by the effects of the digital potentiometer wiper resistance. The output of this circuit is:

$$V_O = \left(\frac{2D}{256} - 1\right) \times V_{REF} \tag{4}$$

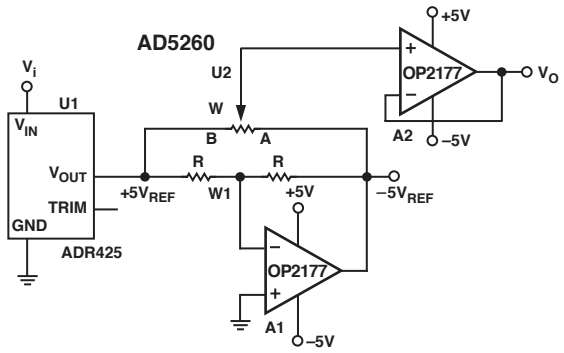


Figure 16. 8-Bit Bipolar DAC

Bipolar Programmable Gain Amplifier

For applications that require bipolar gain, Figure 17 shows one implementation. Digital potentiometer U1 sets the adjustment range. The wiper voltage at W2 can therefore be programmed between V_i and $-KV_i$ at a given U2 setting. Configuring A2 in the noninverting mode allows linear gain and attenuation. The transfer function is:

$$\frac{V_O}{V_i} = \left(1 + \frac{R2}{R1}\right) \times \left(\frac{D2}{256} \times (1 + K) - K\right) \tag{5}$$

where K is the ratio of R_{WB1}/R_{WA1} set by U1.

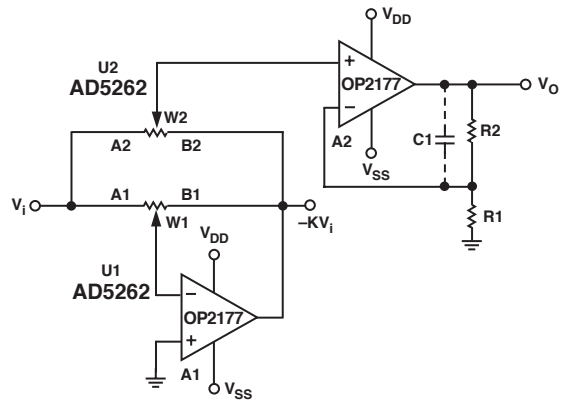


Figure 17. Bipolar Programmable Gain Amplifier

Similar to the previous example, in the simpler (and much more usual) case, where $K = 1$, a single digital pot AD5260, and U1 is replaced by a matched pair of resistors to apply V_i and $-V_i$ at the ends of the digital pot. The relationship becomes:

$$V_O = \left(1 + \frac{R2}{R1}\right)\left(\frac{2D2}{256} - 1\right) \times V_i \tag{6}$$

If R2 is large, a few picofarad compensation capacitors may be needed to avoid any gain peaking.

Table VIII shows the result of adjusting D, with A2 configured as a unity gain, a gain of 2, and a gain of 10. The result is a bipolar amplifier with linearly programmable gain and 256-step resolution.

Table VIII. Result of Bipolar Gain Amplifier

D	R1 = ∞, R2 = 0	R1 = R2	R2 = 9R1
0	–1	–2	–10
64	–0.5	–1	–5
128	0	0	0
192	0.5	1	5
255	0.968	1.937	9.680

Programmable Voltage Source with Boosted Output

For applications that require high current adjustment such as a laser diode driver or turnable laser, a boosted voltage source can be considered (see Figure 18).

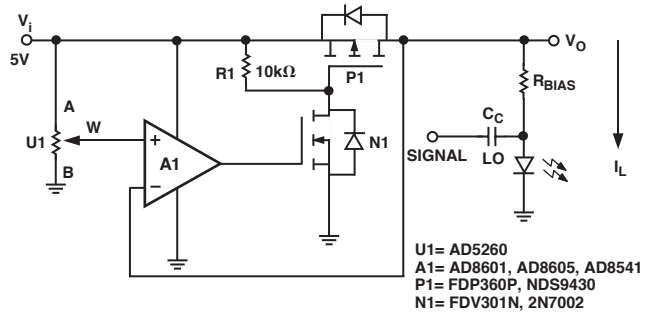


Figure 18. Programmable Boosted Voltage Source

In this circuit, the inverting input of the op amp forces the V_O to be equal to the wiper voltage set by the digital potentiometer. The load current is then delivered by the supply via the P-Ch FET P1. The N-Ch FET N_1 simplifies the op amp driving requirement. A1 needs to be the rail-to-rail input type. Resistor R1 is needed to prevent P1 from not turning off once it is on. The choice of R1 is a balance between the power loss of this resistor and the output turn-off time. N1 can be any general-purpose signal FET; on the other hand, P1 is driven in the saturation state, and therefore its power handling must be adequate to dissipate $(V_i - V_O) \times I_L$ power. This circuit can source a maximum of 100 mA at 5 V supply. Higher current can be achieved with P1 in a larger package. Note, a single N-Ch FET can replace P1, N1, and R1 altogether. However, the output swing will be limited unless separate power supplies are used. For precision application, a voltage reference such as ADR423, ADR292, and AD1584 can be applied at the input of the digital potentiometer.

Programmable 4-to-20 mA Current Source

A programmable 4-to-20 mA current source can be implemented with the circuit shown in Figure 19. REF191 is a unique low supply headroom and high current handling precision reference

that can deliver 20 mA at 2.048 V. The load current is simply the voltage across terminals B-to-W of the digital pot divided by R_S.

$$I_L = \frac{V_{REF} \times D}{R_S} \quad (7)$$

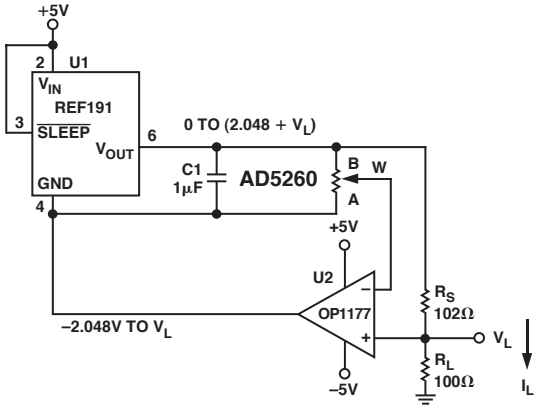


Figure 19. Programmable 4-to-20 mA Current Source

The circuit is simple, but be aware that dual-supply op amps are ideal because the ground potential of REF191 can swing from –2.048 V at zero scale to V_L at full scale of the potentiometer setting. Although the circuit works under single supply, the programmable resolution of the system will be reduced.

Programmable Bidirectional Current Source

For applications that require bidirectional current control or higher voltage compliance, a Howland current pump can be a solution (see Figure 20). If the resistors are matched, the load current is:

$$I_L = \frac{(R2A + R2B)/R1}{R2B} \times V_W \quad (8)$$

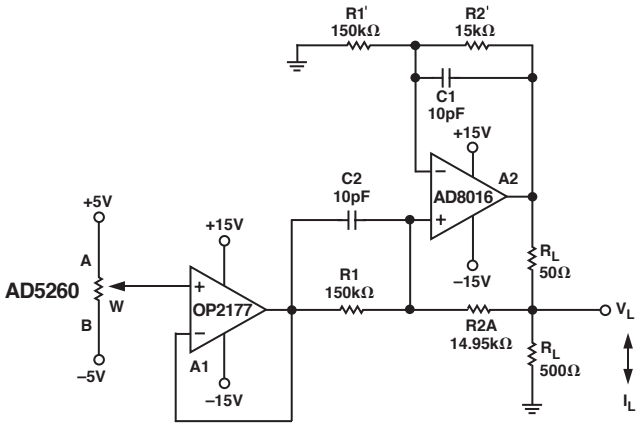


Figure 20. Programmable Bidirectional Current Source

Programmable Low-Pass Filter

Digital potentiometer AD5262 can be used to construct a second order Sallen Key Low-Pass Filter (see Figure 21). The design equations are:

$$\frac{V_O}{V_i} = \frac{\omega_O{}^2}{S^2 + \frac{\omega_O}{Q}S + \omega_O{}^2} \quad (9)$$

$$\omega_O = \sqrt{\frac{1}{R1R2C1C2}} \quad (10)$$

$$Q = \frac{1}{R1C1} + \frac{1}{R2C2} \quad (11)$$

Users can first select some convenient values for the capacitors. To achieve maximally flat bandwidth where Q = 0.707, let C1 be twice the size of C2 and let R1 = R2. As a result, users can adjust R1 and R2 to the same settings to achieve the desirable bandwidth.

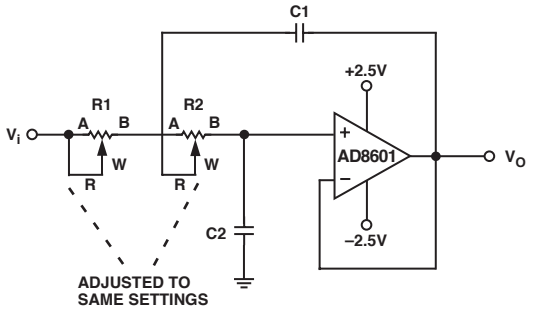


Figure 21. Sallen Key Low-Pass Filter

Programmable Oscillator

In a classic Wien-bridge oscillator, Figure 22, the Wien network (R, R′, C, C′) provides positive feedback, while R1 and R2 provide negative feedback. At the resonant frequency, f_o, the overall phase shift is zero, and the positive feedback causes the circuit to oscillate. With R = R′, C = C′, and R2 = R2A//(R2B+ R_{DIODE}), the oscillation frequency is:

$$\omega_O = \frac{1}{RC} \quad or \quad f_O = \frac{1}{2\pi RC} \quad (12)$$

where R is equal to R_{WA} such that:

$$R = \frac{256 - D}{256} R_{AB} \quad (13)$$

At resonance, setting

$$\frac{R2}{R1} = 2 \quad (14)$$

balances the bridge. In practice, R2/R1 should be set slightly larger than 2 to ensure the oscillation can start. On the other hand, the alternate turn-on of the diodes D1 and D2 ensures R2/R1 to be smaller than 2 momentarily and therefore stabilizes the oscillation.

Once the frequency is set, the oscillation amplitude can be tuned by R2B since:

$$\frac{2}{3}V_O = I_D R2B + V_D \quad (15)$$

V_O, I_D, and V_D are interdependent variables. With proper selection of R2B, an equilibrium will be reached such that V_O converges. R2B can be in series with a discrete resistor to increase the amplitude, but the total resistance cannot be too large to saturate the output.

In both circuits in Figures 21 and 22, the frequency tuning requires that both RDACs be adjusted to the same settings. Since the two channels will be adjusted one at a time, an intermediate state will occur that may not be acceptable for certain applications. As a result, different devices can also be used in daisy-chained mode so that parts can be programmed to the same setting simultaneously.

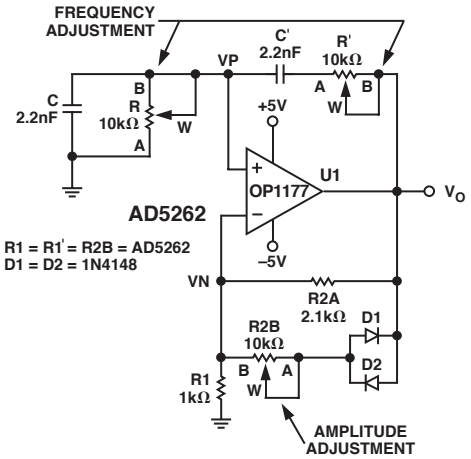


Figure 22. Programmable Oscillator with Amplitude Control

Resistance Scaling

The AD5260/AD5262 offer 20 kΩ, 50 kΩ, and 200 kΩ nominal resistance. For users who need lower resistance and still maintain the numbers of step adjustment, they can parallel multiple devices. For example, Figure 23 shows a simple scheme of paralleling both channels of the AD5262. To adjust half of the resistance linearly per step, users need to program both channels coherently with the same settings.

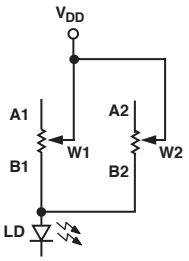


Figure 23. Reduce Resistance by Half with Linear Adjustment Characteristics

In voltage divider mode, a much lower resistance can be achieved by paralleling a discrete resistor as shown in Figure 24. The equivalent resistance becomes:

$$R_{WB\_eq} = \frac{D}{256}\left(R1 /\!/ R2\right) + R_W \quad (16)$$

$$R_{WA\_eq} = \left(1 - \frac{D}{256}\right)\left(R1 /\!/ R2\right) + R_W \quad (17)$$

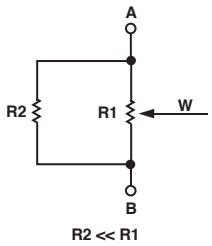


Figure 24. Lowering the Nominal Resistance

Figures 23 and 24 show that the digital potentiometers change steps linearly. On the other hand, log taper adjustment is usually preferred in applications like audio control. Figure 25 shows another way of resistance scaling. In this circuit, the smaller the R2 with respect to R_{AB}, the more the pseudo-log taper characteristic behaves.

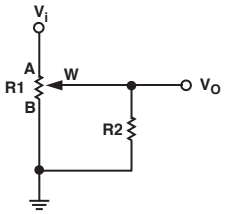


Figure 25. Resistor Scaling with Log Adjustment Characteristics

RDAC CIRCUIT SIMULATION MODEL

The internal parasitic capacitances and the external capacitive loads dominate the ac characteristics of the RDACs. Configured as a potentiometer divider, the –3 dB bandwidth of the AD5260 (20 kΩ resistor) measures 310 kHz at half scale. TPC 20 provides the large signal BODE plot characteristics of the three available resistor versions 20 kΩ, 50 kΩ, and 200 kΩ. A parasitic simulation model is shown in Figure 26. Listing I provides a macro model net list for the 20 kΩ RDAC.

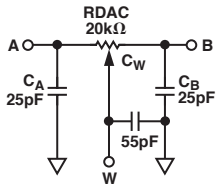


Figure 26. RDAC Circuit Simulation Model for RDAC = 20 kΩ

Listing I. Macro Model Net List for RDAC

```
PARAM D=256, RDAC=20E3
*
SUBCKT DPOT (A,W,B)
*
CA      A       0       25E-12
RWA     A       W       {(1-D/256)*RDAC+60}
CW      W       0       55E-12
RWB     W       B       {D/256*RDAC+60}
CB      B       0       25E-12
*
.ENDS DPOT
```

DIGITAL POTENTIOMETER FAMILY SELECTION GUIDE[1]

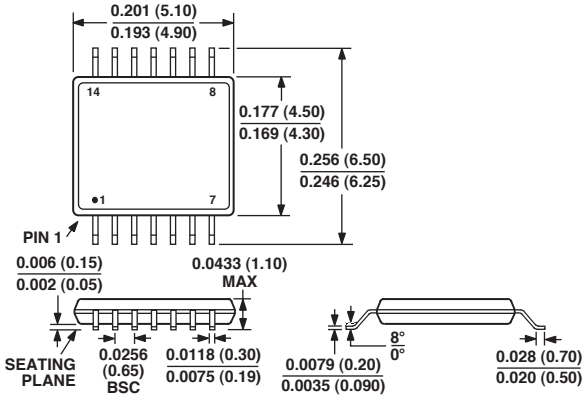
Part Number	Number of VRs per Package	Terminal Voltage Range (V)	Interface Data Control	Nominal Resistance (kΩ)	Resolution (No. of Wiper Positions)	Power Supply Current (I_{DD}) (μA)	Packages	Comments
AD5201	1	±3, 5.5	3-Wire	10, 50	33	40	μSOIC-10	Full AC Specs, Dual Supply, Power-On-Reset, Low Cost
AD5220	1	5.5	UP/DOWN	10, 50, 100	128	40	PDIP, SO-8, μSOIC-8	No Rollover, Power-On-Reset
AD7376	1	±15, 28	3-Wire	10, 50, 100, 1000	128	100	PDIP-14, SOL-16, TSSOP-14	Single 28 V or Dual ±15 V Supply Operation
AD5200	1	±3, 5.5	3-Wire	10, 50	256	40	μSOIC-10	Full AC Specs, Dual Supply, Power-On-Reset
AD8400	1	5.5	3-Wire	1, 10, 50, 100	256	5	SO-8	Full AC Specs
AD5260	1	±5, 15	3-Wire	20, 50, 200	256	60	TSSOP-14	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5241	1	±3, 5.5	2-Wire	10, 100, 1000	256	50	SO-14, TSSOP-14	I^2C Compatible, TC < 50 ppm/°C
AD5231	1	±2.75, 5.5	3-Wire	10, 50, 100	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB settability
AD5222	2	±3, 5.5	UP/DOWN	10, 50, 100, 1000	128	80	SO-14, TSSOP-14	No Rollover, Stereo, Power-On-Reset, TC < 50 ppm/°C
AD8402	2	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SO-14, TSSOP-14	Full AC Specs, nA Shutdown Current
AD5207	2	±3, 5.5	3-Wire	10, 50, 100	256	40	TSSOP-14	Full AC Specs, Dual Supply, Power-On-Reset, SDO
AD5232	2	±2.75, 5.5	3-Wire	10, 50, 100	256	20	TSSOP-16	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5235[2]	2	±2.75, 5.5	3-Wire	25, 250	1024	20	TSSOP-16	Nonvolatile Memory, Direct Program, TC < 50 ppm/°C
AD5242	2	±3, 5.5	2-Wire	10, 100, 1000	256	50	SO-16, TSSOP-16	I^2C Compatible, TC < 50 ppm/°C
AD5262	2	±5, 15	3-Wire	20, 50, 200	256	60	TSSOP-16	5 V to 15 V or ±5 V Operation, TC < 50 ppm/°C
AD5203	4	5.5	3-Wire	10, 100	64	5	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5233	4	±2.75, 5.5	3-Wire	10, 50, 100	64	20	TSSOP-24	Nonvolatile Memory, Direct Program, I/D, ±6 dB Settability
AD5204	4	±3, 5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On-Reset
AD8403	4	5.5	3-Wire	1, 10, 50, 100	256	5	PDIP, SOL-24, TSSOP-24	Full AC Specs, nA Shutdown Current
AD5206	6	±3, 5.5	3-Wire	10, 50, 100	256	60	PDIP, SOL-24, TSSOP-24	Full AC Specs, Dual Supply, Power-On-Reset

[1]For the most current information on digital potentiometers, check the website at: www.analog.com/DigitalPotentiometers
[2]Future product, consult factory for latest status.

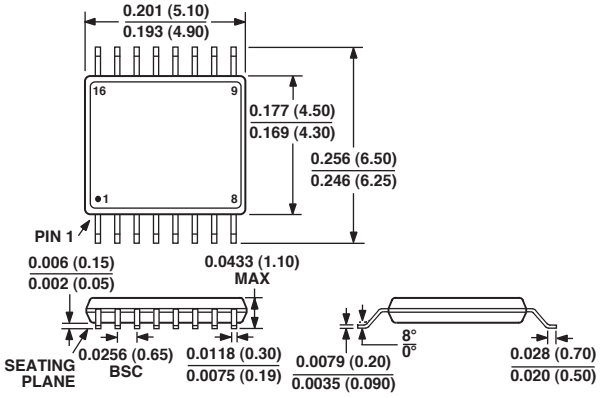
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead TSSOP
(RU-14)



16-Lead TSSOP
(RU-16)



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