

FEATURES

- Dual 12-bit, 3-channel ADC**
- Fast throughput rate: 2 MSPS**
- Specified for V_{DD} of 2.7 V to 5.25 V**
- Low power: 12 mW max at 1.5 MSPS with 3 V supplies**
30 mW max at 2 MSPS with 5 V supplies
- Wide input bandwidth**
- 70 dB SNR at 100 kHz input frequency**
- On-chip reference: 2.5 V**
- 40°C to +125°C operation**
- Flexible power/throughput rate management**
- Simultaneous conversion/read**
- No pipeline delays**
- High speed serial interface SPI®/QSPI™/MICROWIRE™/DSP compatible**
- Shutdown mode: 1 μ A max**
- 32-lead LFCSP and TQFP packages**

GENERAL DESCRIPTION

The AD7266¹ is a dual, 12-bit, high speed, low power, successive approximation ADC that operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 2 MSPS. The device contains two ADCs, each preceded by a 3-channel multiplexer, and a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 10 MHz.

The conversion process and data acquisition are controlled using standard control inputs, allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of \overline{CS} ; conversion is also initiated at this point. The conversion time is determined by the SCLK frequency. There are no pipelined delays associated with the part.

The AD7266 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 5 V supplies and a 2 MSPS throughput rate, the part consumes 4 mA maximum. The part also offers flexible power/throughput rate management when operating in sleep mode.

The analog input range for the part can be selected to be a 0 V to V_{REF} range or a $2V_{REF}$ range with either straight binary or twos complement output coding. The AD7266 has an on-chip 2.5 V reference that can be overdriven if an external reference is preferred. This external reference range is 100 mV to 2.5 V. The AD7266 is available in 32-lead lead frame chip scale (LFCSP) and thin quad flat (TQFP) packages.

¹Protected by U.S. Patent No. 6,681,332.

Rev. PrG

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FUNCTIONAL BLOCK DIAGRAM

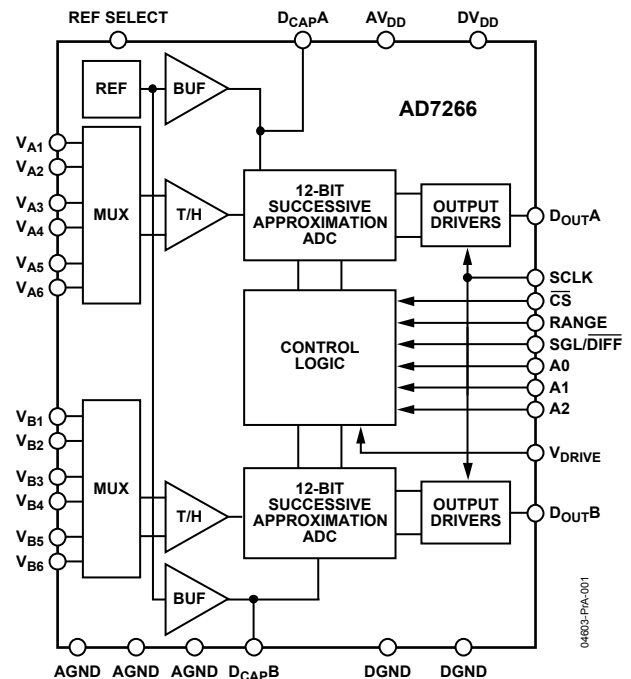


Figure 1

PRODUCT HIGHLIGHTS

1. The AD7266 features two complete ADC functions that allow simultaneous sampling and conversion of two channels. Each ADC has 2 analog inputs, 3 fully differential pairs, or 6 single-ended channels as programmed. The conversion result of both channels is available simultaneously on separate data lines, or in succession on one data line if only one serial port is available.
2. High Throughput with Low Power Consumption
The AD7266 offers a 1.5 MSPS throughput rate with 8 mW maximum power consumption when operating at 3 V.
3. Flexible Power/Throughput Rate Management
The conversion rate is determined by the serial clock, allowing power consumption to be reduced as conversion time is reduced through an SCLK frequency increase. Power efficiency can be maximized at lower throughput rates if the part enters sleep between conversions.
4. No Pipeline Delay
The part features two standard successive approximation ADCs with accurate control of the sampling instant via a \overline{CS} input and once off conversion control.

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REVISION HISTORY

Revision PrG: Preliminary Version

AD7266—SPECIFICATIONS¹

Table 1. $T_A = T_{MIN}$ to T_{MAX} , $V_{DD} = 2.7$ V to 3.3 V, $f_{SCLK} = 25$ MHz, $f_s = 1.5$ MSPS, $V_{DRIVE} = 2.7$ V to 3.3 V; $V_{DD} = 4.75$ V to 5.25 V, $f_{SCLK} = 32$ MHz, $f_s = 2$ MSPS, $V_{DRIVE} = 2.7$ V to 5.25 V; Reference = 2.5 V \pm 1%, unless otherwise noted

Parameter	Specification	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal-to-Noise + Distortion Ratio (SINAD) ²	70	dB min	$f_{IN} = 100$ kHz sine wave
Total Harmonic Distortion (THD) ²	-75	dB max	$f_{IN} = 100$ kHz sine wave
Spurious Free Dynamic Range (SFDR) ²	-76	dB max	$f_{IN} = 100$ kHz sine wave
Intermodulation Distortion (IMD) ²			
Second Order Terms	-88	dB typ	
Third Order Terms	-88	dB typ	
Channel to Channel Isolation	-88	dB typ	
SAMPLE AND HOLD			
Aperture Delay ³	10	ns max	
Aperture Jitter ³	50	ps typ	
Aperture Delay Matching ³	200	ps max	
Full Power Bandwidth	20	MHz typ	@ 3 dB
	2.5	MHz typ	@0.1 dB
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity ²	± 1	LSB max	± 0.5 LSB typ; differential configuration
	± 1.5	LSB max	± 0.5 LSB typ; single-ended configuration
Differential Nonlinearity ²	± 0.95	LSB max	Guaranteed no missed codes to 12 bits
0 V to V_{REF} Input Range			Straight binary output coding
Offset Error	± 3	LSB max	
Offset Error Match	± 0.5	LSB typ	
Gain Error	± 2	LSB max	
Gain Error Match	± 0.6	LSB typ	
0 V to $2 \times V_{REF}$ Input Range			Twos complement output coding
Positive Gain Error	± 2	LSB max	
Zero Code Error	± 3	LSB max	
Zero Code Error Match	± 1	LSB typ	
Negative Gain Error	± 1	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 V to V_{REF}	V	RANGE pin low upon \overline{CS} falling edge
	0 V to $2 \times V_{REF}$	V	RANGE pin high upon \overline{CS} falling edge
DC Leakage Current	± 500	nA max	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	± 1	μA max	$85^\circ\text{C} < T_A \leq 125^\circ\text{C}$
Input Capacitance	30	pF typ	When in track
	10	pF typ	When in hold
REFERENCE INPUT/OUTPUT			
Reference Output Voltage ⁴	2.49/2.51	V min/V max	
Reference Input Voltage Range	0.1/2.5	V min/V max	See Typical Performance plots
DC Leakage Current	± 30	μA max	V_{REF} pin
	± 160	μA max	D_{CAPA} , D_{CAPB} pins
Input Capacitance	20	pF typ	
V_{REF} Output Impedance ⁵	25	Ω typ	
Reference Temperature Coefficient	25	ppm/ $^\circ\text{C}$ max	
	10	ppm/ $^\circ\text{C}$ typ	
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	± 1	μA max	Typically 15 nA, $V_{IN} = 0$ V or V_{DRIVE}
Input Capacitance, C_{IN}^3	10	pF max	

Parameter	Specification	Unit	Test Conditions/Comments
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	$V_{DRIVE} - 0.2$	V min	
Output Low Voltage, V_{OL}	0.4	V max	
Floating State Leakage Current	± 1	μA max	
Floating State Output Capacitance ³	10	pF max	
Output Coding	Straight (Natural) Binary Twos Complement		$SGL/\overline{DIFF} = 1$ with 0 V to V_{REF} range selected $SGL/\overline{DIFF} = 0$; $SGL/\overline{DIFF} = 1$ with 0 V to $2 \times V_{REF}$ range
CONVERSION RATE			
Conversion Time	14	SCLK Cycles	437.5 ns with SCLK = 32 MHz
Track/Hold Acquisition Time ³	100	ns max	
Throughput Rate	2	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.7/5.25	V min/V max	
V_{DRIVE}	2.7/5.25	V min/V max	
I_{DD} ⁶			Digital I/Ps = 0 V or V_{DRIVE}
Normal Mode (Static)	2	mA max	
Operational, $f_s = 2$ MSPS	6	mA max	$V_{DD} = 5$ V
	4	mA max	$V_{DD} = 3$ V
Partial Power-Down Mode	TBD	mA max	$f_s = 200$ kSPS
Partial Power-Down Mode	500	μA max	Static
Full Power-Down Mode	1	μA max	
Power Dissipation ⁶			
Normal Mode (Operational)	30	mW max	$V_{DD} = 5$ V
Partial Power-Down (Static)	2.5	mW max	$V_{DD} = 5$ V
Full Power-Down (Static)	5	μW max	$V_{DD} = 5$ V

NOTES

¹ Temperature ranges as follows: -40°C to +125°C

² See Terminology section.

³ Sample tested during initial release to ensure compliance.

⁴ Relates to Pins D_{CAPA} or D_{CAPB} .

⁵ See Reference section for D_{CAPA} , D_{CAPB} output impedances.

⁶ See Power Versus Throughput Rate section.

TIMING SPECIFICATIONS

Table 2. $AV_{DD} = DV_{DD} = 2.7$ V to 5.25 V, $V_{DRIVE} = 2.7$ V to 5.25 V, $T_A = T_{MAX}$ to T_{MIN} , unless otherwise noted

Parameter	Limit at T_{MIN} , T_{MAX}	Unit	Description
f_{SCLK}	10 34	kHz min MHz max	
$t_{CONVERT}$	$14 \times t_{SCLK}$ 437.5 560	ns max ns max ns max	$t_{SCLK} = 1/f_{SCLK}$ $f_{SCLK} = 32$ MHz, $V_{DD} = 5$ V, $F_{SAMPLE} = 2$ MSPS $f_{SCLK} = 25$ MHz, $V_{DD} = 3$ V, $F_{SAMPLE} = 1.5$ MSPS
t_{QUIET}	35	ns max	Minimum time between end of serial read and next falling edge of \overline{CS}
t_2	10	ns min	\overline{CS} to SCLK setup time
t_3	25	ns max	Delay from \overline{CS} until D_{OUTA} and D_{OUTB} are three-state disabled
t_4	25	ns max	Data access time after SCLK falling edge.
t_5	$0.4t_{SCLK}$	ns min	SCLK low pulse width
t_6	$0.4t_{SCLK}$	ns min	SCLK high pulse width
t_7	5	ns min	SCLK to data valid hold time
t_8	25	ns max	\overline{CS} rising edge to D_{OUTA} , D_{OUTB} , high impedance
t_9	60	ns min	\overline{CS} rising edge to falling edge pulsewidth
t_{10}	5 30	ns min ns max	SCLK falling edge to D_{OUTA} , D_{OUTB} , high impedance SCLK falling edge to D_{OUTA} , D_{OUTB} , high impedance

All timing specifications given are with a 25 pF load capacitance. With a load capacitance greater than this value, a digital buffer or latch must be used.

ABSOLUTE MAXIMUM RATINGS

Table 3. AD7266 Stress Ratings

Parameter	Rating
V _{DD} to AGND	-0.3 V to +7 V
DV _{DD} to DGND	-0.3 V to +7 V
V _{DRIVE} to DGND	-0.3 V to DV _{DD}
V _{DRIVE} to AGND	-0.3 V to AV _{DD}
AV _{DD} to DV _{DD}	-0.3 V to +0.3 V
AGND to DGND	-0.3 V to +0.3 V
Analog Input Voltage to AGND	-0.3 V to AV _{DD} +0.3 V
Digital Input Voltage to DGND	-0.3 V to +7 V
Digital Output Voltage to GND	-0.3 V to V _{DRIVE} +0.3 V
V _{REF} to AGND	-0.3 V to AV _{DD} +0.3 V
Input Current to Any Pin Except Supplies ¹	±10 mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	150°C
LFCSP Package	
θ _{JA} Thermal Impedance	108.2°C/W
θ _{JC} Thermal Impedance	32.71°C/W
Lead Temperature, Soldering	
Reflow Temperature (10- 30 sec)	255°C
ESD	TBD

¹ Transient currents of up to 100 mA will not cause SCR latch up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTIONAL DESCRIPTIONS

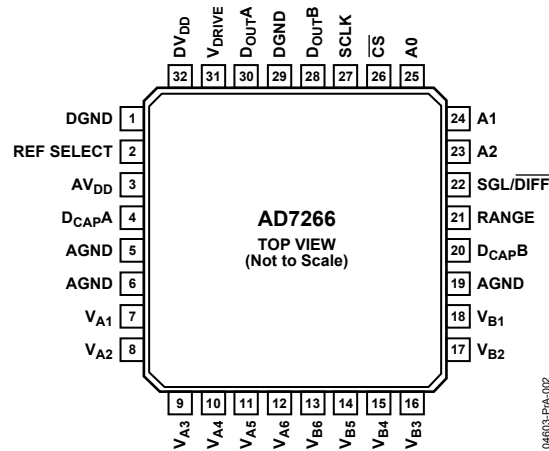


Figure 2. AD7266 Pin Configuration

Table 4. AD7266 Pin Function Descriptions

Pin No.	Mnemonic	Description
4, 20	D_{CAPA} , D_{CAPB}	Decoupling capacitors (470nF recommended) are connected to these pins to decouple the reference buffer for each respective ADC. The on-chip reference can be taken from these pins and applied externally to the rest of a system. The range of the external reference is dependent on the analog input range selected. See the Reference Configuration Options section.
7–12	V_{A1} – V_{A6}	Analog Inputs of ADC A. These may be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 6.
18–13	V_{B1} – V_{B6}	Analog Inputs of ADC B. These may be programmed as six single-ended channels or three true differential analog input channel pairs. See Table 6.
27	SCLK	Serial Clock. Logic Input. A serial clock input provides the SCLK for accessing the data from the AD7266. This clock is also used as the clock source for the conversion process.
5, 6, 19	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7266. All analog input signals and any external reference signal should be referred to this AGND voltage. All three of these AGND pins should connect to the AGND plane of a system. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
32	DVDD	Digital Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for all digital circuitry on the AD7266. The DVDD and AVDD voltages should ideally be at the same potential and must not be more than 0.3 V apart even on a transient basis. This supply should be decoupled to DGND.
31	VDRIVE	Logic power supply input. The voltage supplied at this pin determines at what voltage the interface will operate. This pin should be decoupled to DGND. The voltage at this pin may be different to that at AVDD and DVDD but should never exceed either by more than 0.3 V.
1, 29	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7266. Both DGND pins should connect to the DGND plane of a system. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
3	AVDD	Analog Supply Voltage, 2.7 V to 5.25 V. This is the only supply voltage for all analog circuitry on the AD7266. The AVDD and DVDD voltages should ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. This supply should be decoupled to AGND.
26	\overline{CS}	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7266 and frames the serial data transfer.
30, 28	D_{OUTA} , D_{OUTB}	Serial Data Outputs. The data output is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input and 14 SCLKs are required to access the data. The data appears on both pins simultaneously from the simultaneous conversions of both ADCs. The data stream consists of two leading zeros followed by the 12 bits of conversion data. The data is provided MSB first. If \overline{CS} is held low for 16 SCLK cycles rather than 14, then two trailing zeros will appear after the 12 bits of data. If \overline{CS} is held low for a further 16 SCLK cycles after this on either D_{OUTA} or D_{OUTB} , the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either D_{OUTA} or D_{OUTB} alone using only one serial port. See the Serial Interface section.

Pin No.	Mnemonic	Description
21	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin will determine what input range the analog input channels will have. On the falling edge of \overline{CS} , the polarity of this pin is checked to determine the analog input range of the next conversion. If this pin is tied to a logic low, the analog input range is 0 V to VREF. If this pin is tied to a logic high when \overline{CS} goes low, the analog input range is $2 \times V_{REF}$.
25–23	A0–A2	Multiplexer Select. Logic inputs. These inputs are used to select the pair of channels to be converted simultaneously, i.e., Channel 1 of both ADC A and ADC B, Channel 2 of both ADC A and ADC, and so on. The pair of channels selected may be two single ended channels or two differential pairs. The logic states of these pins are checked upon the falling edge of \overline{CS} , and the multiplexer is set up for the next conversion. See Table 6 for multiplexer address decoding.
22	SGL/ \overline{DIFF}	Logic Input. This pin selects whether the analog inputs are configured as differential pairs or single ended. A logic low selects differential operation while a logic high selects single ended operation.
2	REF SELECT	Internal/External reference Selection. Logic Input. If this pin is tied to GND, the on-chip 2.5 V reference is used as the reference source for both ADC A and ADC B. In addition, Pins D _{CAP A} and D _{CAP B} must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, an external reference can be supplied to the AD7266 through the D _{CAP A} and/or D _{CAP B} pins.

TERMINOLOGY

Differential Nonlinearity

This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity

This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Offset Error

This applies to Straight Binary output coding. It is the deviation of the first code transition (00...000) to (00...001) from the ideal, i.e., AGND + 1 LSB.

Offset Error Match

This is the difference in Offset Error between the two channels.

Gain Error

This applies to Straight Binary output coding. It is the deviation of the last code transition (111...110) to (111...111) from the ideal (i.e., $V_{REF} - 1$ LSB) after the offset error has been adjusted out.

Gain Error Match

This is the difference in Gain Error between the two channels.

Zero Code Error

This applies when using twos complement output coding in particular with the $2 \times V_{REF}$ input range as $-V_{REF}$ to $+V_{REF}$ biased about the V_{REF} point. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal V_{IN} voltage, i.e., $V_{REF} - 1$ LSB.

Zero Code Error Match

This refers to the difference in Zero Code Error between the two channels.

Positive Gain Error

This applies when using twos complement output coding in particular with the $2 \times V_{REF}$ input range as $-V_{REF}$ to $+V_{REF}$ biased about the V_{REF} point. It is the deviation of the last code transition (011...110) to (011...111) from the ideal (i.e., $+V_{REF} - 1$ LSB) after the Zero Code Error has been adjusted out.

Track-and-Hold Acquisition Time

The track-and-hold amplifier returns into track mode after the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within $\pm 1/2$ LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio

This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_s/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

$$\text{Signal to (Noise + Distortion)} = (6.02N + 1.76) \text{ dB}$$

Thus for a 12-bit converter, this is 74 dB.

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7266 it is defined as:

$$\text{THD(dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise

Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_s/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Channel-to-Channel Isolation

Channel-to-channel isolation is a measure of the level of crosstalk between channels. It is measured by applying a full-scale ($2 \times V_{REF}$), 455kHz sine wave signal to all unselected input channels and determining how much that signal is attenuated in the selected channel with a 10 kHz signal (0 V to V_{REF}). The figure given is the worst-case across all twelve channels for the AD7266.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, f_a and f_b , any active device with nonlinearities will create distortion products at sum and difference frequencies of $m f_a \pm n f_b$ where $m, n = 0, 1, 2, 3$, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, while the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$.

The AD7266 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies.

As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSR (Power Supply Rejection)

Variations in power supply will affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. See Typical Performance Curves.

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7266 is a fast, micropower, dual 12-bit, single supply, A/D converter that operates from a 2.7 V to 5.25 V supply. When operated from a 5 V supply, the AD7266 is capable of throughput rates of 2 MSPS when provided with a TBD MHz clock, and a throughput rate of 1.5 MSPS at 3 V.

The AD7266 contains two on-chip differential track-and-hold amplifiers, two successive approximation A/D converters, and a serial interface with two separate data output pins, and is housed in a 32-lead LFCSP package, which offers the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for each successive approximation ADC. The analog input range for the part can be selected to be a 0 V to V_{REF} input or a $2 \times V_{REF}$ input with the analog inputs configured as either single ended or differential. The AD7266 has an on-chip 2.5 V reference that can be overdriven if an external reference is preferred.

The AD7266 also features power-down options to allow power saving between conversions. The power-down feature is implemented across the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7266 has two successive approximation analog-to-digital converters, each based around two capacitive DACs. Figure 3 and Figure 4 show simplified schematics of one of these ADCs in acquisition and conversion phase, respectively. The ADC is comprised of control logic, a SAR, and two capacitive DACs. In Figure 3 (the acquisition phase), SW3, is closed, SW1 and SW2 are in position A, the comparator is held in a balanced condition, and the sampling capacitor arrays acquire the differential signal on the input.

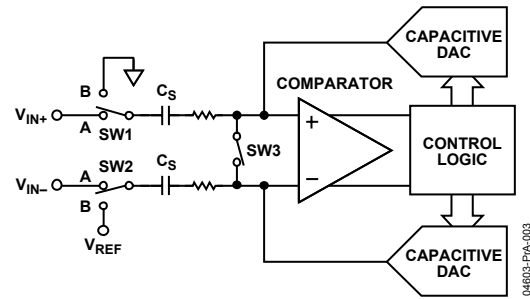


Figure 3. ADC Acquisition Phase

When the ADC starts a conversion (Figure 4), SW3 opens and SW1 and SW2 move to position B, causing the comparator to become unbalanced. Both inputs are disconnected once the conversion begins. The control logic and the charge redistribution DACs are used to add and subtract fixed amounts of charge from the sampling capacitor arrays to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. The output impedances of the sources driving the V_{IN+} and V_{IN-} pins must be matched; otherwise, the two inputs will have different settling times, resulting in errors.

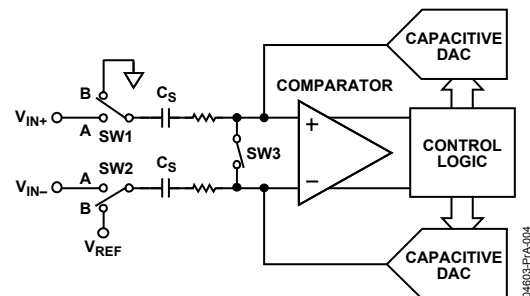


Figure 4. ADC Conversion Phase

ANALOG INPUT

The analog inputs of the AD7266 may be configured as single ended or true differential via the $\overline{\text{SGL/DIFF}}$ pin, as shown in Figure 5. On the falling edge of $\overline{\text{CS}}$, point A, the logic level of the $\overline{\text{SGL/DIFF}}$ pin is checked to determine the configuration of the analog input channels for the *next* conversion. If this pin is tied to a logic low, the analog input channels to each on-chip ADC are set up as three true differential pairs. If this pin is at a logic high when $\overline{\text{CS}}$ goes low, the analog input channels to each on-chip ADC are set up as six single-ended analog inputs. In Figure 5 at point A, the $\overline{\text{SGL/DIFF}}$ pin is at a logic high so the analog inputs are configured as single-ended for the next conversion, i.e. sampling point B. At point B, the logic level of the $\overline{\text{SGL/DIFF}}$ pin has changed to low; therefore, the analog inputs are configured as differential for the next conversion after this one, even though this current conversion is on single ended configured inputs.

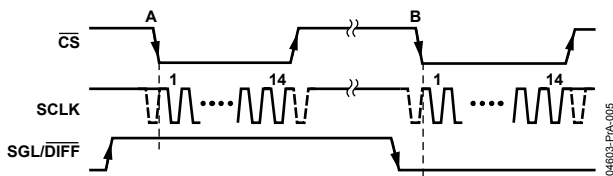


Figure 5. Selecting Differential or Single Ended Configuration

The channels to be converted on simultaneously are selected via the multiplexer address inputs A0 to A2. The logic states of these pins are also checked upon the falling edge of $\overline{\text{CS}}$ and the channels are chosen for the *next* conversion. The selected input channels are decoded as shown in Table 6.

The analog input range of the AD7266 can be selected as 0 V to V_{REF} or 0 V to $2 \times V_{\text{REF}}$ via the RANGE pin. This selection is made in a similar fashion to that of the $\overline{\text{SGL/DIFF}}$ pin by checking the logic state of the RANGE pin upon the falling edge of $\overline{\text{CS}}$. The analog input range is set up for the *next* conversion. If this pin is tied to a logic low upon the falling edge of $\overline{\text{CS}}$, the analog input range for the next conversion is 0 V to V_{REF} . If this pin is tied to a logic high upon the falling edge of $\overline{\text{CS}}$, the analog input range for the next conversion is 0 V to $2 \times V_{\text{REF}}$.

OUTPUT CODING

The AD7266 output coding is set to either twos complement or straight binary depending on which analog input configuration is selected for a conversion. Table 5 shows which output coding scheme is used for each possible analog input configuration.

Table 5 AD7266 Output Coding

SGL/DIFF	Range	Output Coding
DIFF	0 V to V_{REF}	Twos Complement
DIFF	0 V to $2 \times V_{\text{REF}}$	Twos Complement
SGL	0 V to V_{REF}	Straight Binary
SGL	0 V to $2 \times V_{\text{REF}}$	Twos Complement
PSUEDO DIFF	0 V to V_{REF}	Straight Binary
PSUEDO DIFF	0 V to $2 \times V_{\text{REF}}$	Twos Complement

Table 6. Analog Input Type and Channel Selection

SGL/DIFF	A2	A1	A0	ADC A		ADC B		Comment
				V _{IN+}	V _{IN-}	V _{IN+}	V _{IN-}	
1	0	0	0	V _{A1}	AGND	V _{B1}	AGND	Single Ended
1	0	0	1	V _{A2}	AGND	V _{B2}	AGND	Single Ended
1	0	1	0	V _{A3}	AGND	V _{B3}	AGND	Single Ended
1	0	1	1	V _{A4}	AGND	V _{B4}	AGND	Single Ended
1	1	0	0	V _{A5}	AGND	V _{B5}	AGND	Single Ended
1	1	0	1	V _{A6}	AGND	V _{B6}	AGND	Single Ended
0	0	0	0	V _{A1}	V _{A2}	V _{B1}	V _{B2}	Fully Differential
0	0	0	1	V _{A1}	V _{A2}	V _{B1}	V _{B2}	Pseudodifferential
0	0	1	0	V _{A3}	V _{A4}	V _{B3}	V _{B4}	Fully Differential
0	0	1	1	V _{A3}	V _{A4}	V _{B3}	V _{B4}	Pseudodifferential
0	1	0	0	V _{A5}	V _{A6}	V _{B5}	V _{B6}	Fully Differential
0	1	0	1	V _{A5}	V _{A6}	V _{B5}	V _{B6}	Pseudodifferential

MODES OF OPERATION

The mode of operation of the AD7266 is selected by controlling the (logic) state of the \overline{CS} signal during a conversion. There are three possible modes of operation: normal mode, partial power-down mode, and full power-down mode. The point at which \overline{CS} is pulled high after the conversion has been initiated determines which power-down mode, if any, the device enters. Similarly, if already in a power-down mode, \overline{CS} can control whether the device returns to normal operation or remains in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

NORMAL MODE

This mode is intended for fastest throughput rate performance since the user does not have to worry about any power-up times with the AD7266 remaining fully powered all the time. Figure 8 shows the general diagram of the operation of the AD7266 in this mode.

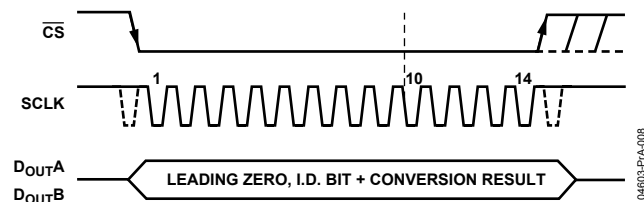


Figure 8. Normal Mode Operation

The conversion is initiated on the falling edge of \overline{CS} , as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, \overline{CS} must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of \overline{CS} . If \overline{CS} is brought high any time after the 10th SCLK falling edge but before the 14th SCLK falling edge, the part remains powered up but the conversion is terminated and D_{OUTA} and D_{OUTB} go back into three-state. Fourteen serial clock cycles are required to complete the conversion and access the conversion result. The D_{OUT} line does not return to three-state after 14 SCLK cycles have elapsed, but instead does so when \overline{CS} is brought high again. If \overline{CS} is left low for another 2 SCLK cycles (e.g. if only a 16 SCLK burst is available), two trailing zeros are clocked out after the data. If \overline{CS} is left low for a further 16 SCLK cycles again, the result from the other ADC on board is also

accessed on the same D_{OUT} line, as shown in Figure TBD (see the Serial Interface section). The identification bit provided prior to each conversion result identifies which on-board ADC the following result is from. Once 32 SCLK cycles have elapsed, the D_{OUT} line returns to three-state on the 32nd SCLK falling edge. If \overline{CS} is brought high prior to this, the D_{OUT} line returns to three-state at that point. Thus, \overline{CS} may idle low after 32 SCLK cycles until it is brought high again sometime prior to the next conversion (effectively idling \overline{CS} low), if so desired, since the bus still returns to three-state upon completion of the dual result read.

Once a data transfer is complete and D_{OUTA} and D_{OUTB} have returned to three-state, another conversion can be initiated after the quiet time, t_{QUIET} , has elapsed by bringing \overline{CS} low again.

PARTIAL POWER-DOWN MODE

This mode is intended for use in applications where slower throughput rates are required. Either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7266 is in partial power-down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter partial power-down, the conversion process must be interrupted by bringing \overline{CS} high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 9. Once \overline{CS} has been brought high in this window of SCLKs, the part enters partial power-down, the conversion that was initiated by the falling edge of \overline{CS} is terminated, and D_{OUTA} and D_{OUTB} go back into three-state. If \overline{CS} is brought high before the second SCLK falling edge, the part remains in normal mode and does not power down. This avoids accidental power-down due to glitches on the \overline{CS} line.

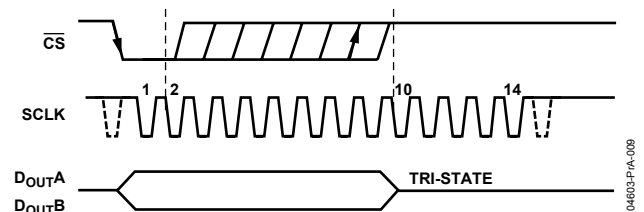


Figure 9. Entering Partial Power-Down Mode

To exit this mode of operation and power up the AD7266 again, a dummy conversion is performed. On the falling edge of \overline{CS} , the device begins to power up, and continues to power up as long as \overline{CS} is held low until after the falling edge of the 10th SCLK. The device is fully powered up after approximately 1 μ s has elapsed, and valid data results from the next conversion, as shown in Figure 10. If \overline{CS} is brought high before the second falling edge of SCLK, the AD7266 again goes into partial power-down. This avoids accidental power-up due to glitches on the \overline{CS} line. Although the device may begin to power up on the falling edge of \overline{CS} , it powers down again on the rising edge of \overline{CS} . If the AD7266 is already in partial power-down mode and \overline{CS} is brought high between the second and 10th falling edges of SCLK, the device enters full power-down mode.

FULL POWER-DOWN MODE

This mode is intended for use in applications where throughput rates slower than those in the partial power-down mode are required, as power-up from a full power-down takes substantially longer than that from partial power-down. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate are followed by a long period of inactivity and thus power-down. When the

AD7266 is in full power-down, all analog circuitry is powered down. Full power-down is entered in a similar way as partial power-down, except the timing sequence shown in Figure 9 must be executed twice. The conversion process must be interrupted in a similar fashion by bringing \overline{CS} high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK. The device enters partial power-down at this point. To reach full power-down, the next conversion cycle must be interrupted in the same way, as shown in Figure TBD. Once \overline{CS} has been brought high in this window of SCLKs, the part powers down completely.

Note that it is not necessary to complete the 14 SCLKs once \overline{CS} has been brought high to enter a power-down mode.

To exit full power-down and power the AD7266 up again, a dummy conversion is performed, as when powering up from partial power-down. On the falling edge of \overline{CS} , the device begins to power up and continues to power up as long as \overline{CS} is held low until after the falling edge of the 10th SCLK. The power-up time required must elapse before a conversion can be initiated, as shown in Figure TBD. See the Power-Up Times section for the power-up times associated with the AD7266.

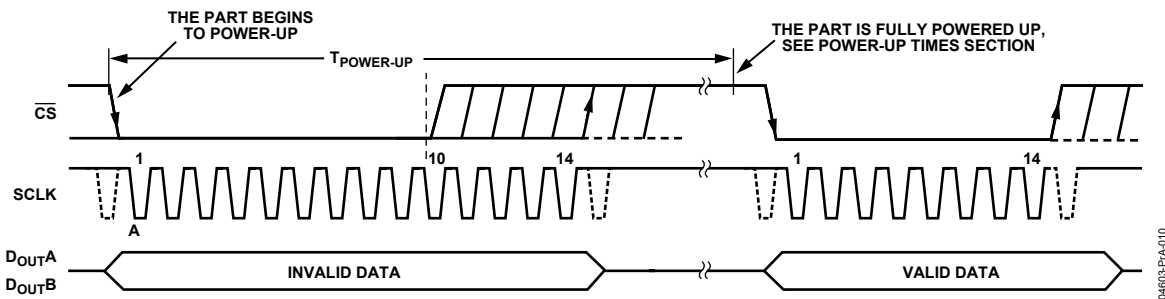


Figure 10. Exiting Partial Power-Down Mode

SERIAL INTERFACE

Figure 11 shows the detailed timing diagram for serial interfacing to the AD7266. The serial clock provides the conversion clock and controls the transfer of information from the AD7266 during conversion.

The \overline{CS} signal initiates the data transfer and conversion process. The falling edge of \overline{CS} puts the track and hold into hold mode and takes the bus out of three-state; the analog input is sampled at this point. The conversion is also initiated at this point and requires a minimum of 14 SCLKs to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold will go back into track on the next SCLK rising edge, as shown in Figure 11 at point B. If a 16 SCK transfer is used then 2 trailing zeros will appear after the final LSB. On the rising edge of \overline{CS} , the conversion will be terminated and D_{OUTA} and D_{OUTB} will go back into three-state. If \overline{CS} is not brought high but is instead held low for a further 14 (or 16) SCLK cycles on D_{OUTA} , the data from conversion B will be output on D_{OUTA} (followed by 2 trailing zeros). Likewise, if \overline{CS} is held low for a further 14 (or 16) SCLK cycles on D_{OUTB} , the data from conversion A will be output on D_{OUTB} . This is illustrated in Figure 12 where the case

for D_{OUTA} is shown. Note that in this case, the D_{OUT} line in use will go back into three-state on the 32nd SCLK falling edge or the rising edge of \overline{CS} , whichever occurs first.

A minimum of fourteen serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the AD7266. \overline{CS} going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with a second leading zero. Thus the first falling clock edge on the serial clock has the leading zero provided and also clocks out the second leading zero. The 12 bit result then follows with the final bit in the data transfer valid on the fourteenth falling edge, having being clocked out on the previous (thirteenth) falling edge. In applications with a slower SCLK, it may be possible to read in data on each SCLK rising edge depending on the SCLK frequency used, i.e., the first rising edge of SCLK after the \overline{CS} falling edge would have the leading zero provided and the thirteenth rising SCLK edge would have DB0 provided.

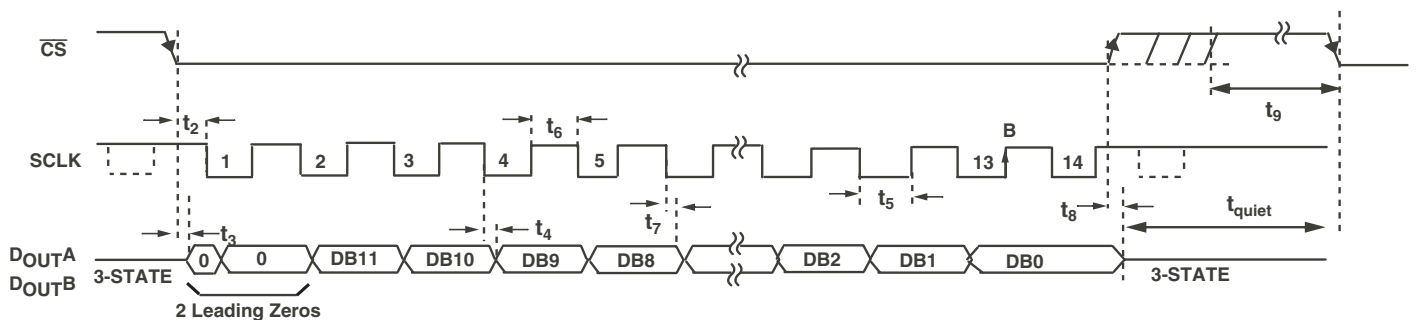


Figure 11 Serial Interface Timing Diagram

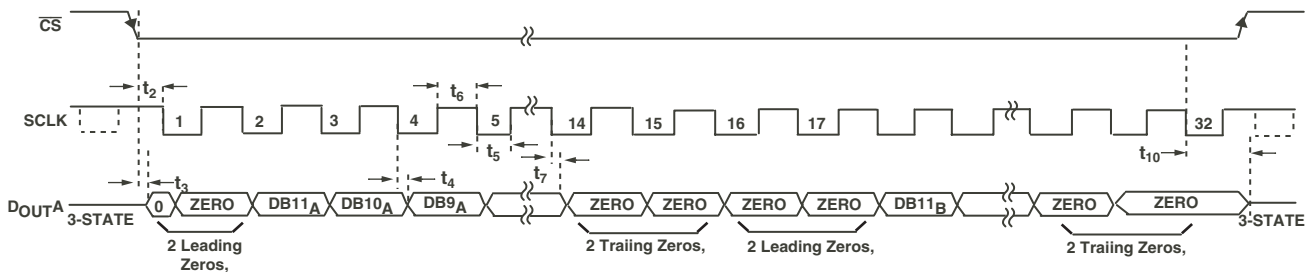


Figure 12. Reading data from Both ADCs on One D_{OUT} Line with 32 SCLKs

ORDERING GUIDE

AD7266 Products	Temperature Package	Package Description	Package Outline
AD7266ACP	-40°C to +125°C	Lead Frame Chip Scale Package	CP-32
AD7266BCP	-40°C to +125°C	Lead Frame Chip Scale Package	CP-32
AD7266ASU	-40°C to +125°C	Thin Quad Flat Package	SU-32
AD7266BSU	-40°C to +125°C	Thin Quad Flat Package	SU-32
EVAL-AD7266CB ¹		Evaluation Board	
EVAL-CONTROL BRD ²		Controller Board	

¹ This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL Board for evaluation/demonstration purposes.

² This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators. To order a complete evaluation kit, the particular ADC evaluation board, e.g., EVAL-AD7266CB, the EVAL-CONTROL BRD2, and a 12V transformer must be ordered. See relevant Evaluation Board Technical note for more information.

