2.35 V to 5.25 V, 1 MSPS, 12-/10-/8-Bit ADCs in 6-Lead SC70

AD7476A/AD7477A/AD7478A*

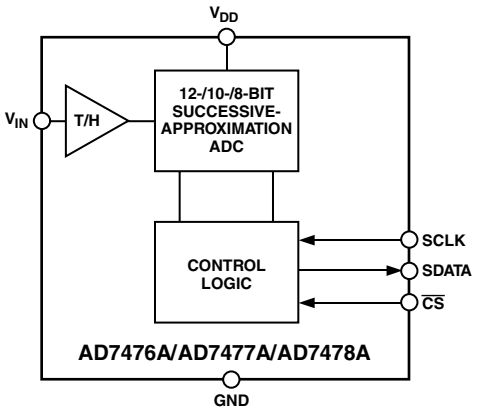
FEATURES

- Fast Throughput Rate: 1 MSPS
- Specified for V_{DD} of 2.35 V to 5.25 V
- Low Power:
  - 3.6 mW Typ at 1 MSPS with 3 V Supplies
  - 12.5 mW Typ at 1 MSPS with 5 V Supplies
- Wide Input Bandwidth:
  - 71 dB SNR at 100 kHz Input Frequency
- Flexible Power/Serial Clock Speed Management
- No Pipeline Delays
- High Speed Serial Interface
  - SPI®/QSPI™/MICROWIRE™/DSP Compatible
- Standby Mode: 1 μA Max
- 6-Lead SC70 Package
- 8-Lead MSOP Package

APPLICATIONS

- Battery-Powered Systems
  - Personal Digital Assistants
  - Medical Instruments
  - Mobile Communications
- Instrumentation and Control Systems
- Data Acquisition Systems
- High Speed Modems
- Optical Sensors

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7476A/AD7477A/AD7478A are 12-bit, 10-bit, and 8-bit high speed, low power, successive-approximation ADCs, respectively. The parts operate from a single 2.35 V to 5.25 V power supply and feature throughput rates up to 1 MSPS. The parts contain a low noise, wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 13 MHz.

The conversion process and data acquisition are controlled using $\overline{CS}$ and the serial clock, allowing the devices to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$, and the conversion is also initiated at this point. There are no pipeline delays associated with the parts.

The AD7476A/AD7477A/AD7478A use advanced design techniques to achieve low power dissipation at high throughput rates.

The reference for the part is taken internally from V_{DD}, which allows the widest dynamic input range to the ADC. Thus, the analog input range for the part is 0 to V_{DD}. The conversion rate is determined by the SCLK.

PRODUCT HIGHLIGHTS

1. First 8-/10-/12-bit ADCs in an SC70 package.
2. High throughput with low power consumption.
3. Flexible power/serial clock speed management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced when a power-down mode is used while not converting. The parts also feature a power-down mode to maximize power efficiency at lower throughput rates. Current consumption is 1 μA max and 50 nA typically when in power-down mode.
4. Reference derived from the power supply.
5. No pipeline delay. The parts feature a standard successive-approximation ADC with accurate control of the sampling instant via a $\overline{CS}$ input and once-off conversion control.

*Protected by U.S.Patent No. 6,681,332.

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD7476A–SPECIFICATIONS[1] (V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[2]	B Grade[2]	Y Grade[2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	70	70	70	dB min	V_{DD} = 2.35 V to 3.6 V, T_A = 25°C
	69	69	69	dB min	V_{DD} = 2.4 V to 3.6 V
	71.5	71.5	71.5	dB typ	V_{DD} = 2.35 V to 3.6 V
	69	69	69	dB min	V_{DD} = 4.75 V to 5.25 V, T_A = 25°C
	68	68	68	dB min	V_{DD} = 4.75 V to 5.25 V
Signal-to-Noise Ratio (SNR)[3]	71	71	71	dB min	V_{DD} = 2.35 V to 3.6 V, T_A = 25°C
	70	70	70	dB min	V_{DD} = 2.4 V to 3.6 V
	70	70	70	dB min	V_{DD} = 4.75 V to 5.25 V, T_A = 25°C
	69	69	69	dB min	V_{DD} = 4.75 V to 5.25 V
Total Harmonic Distortion (THD)[3]	–80	–80	–80	dB typ	
Peak Harmonic or Spurious Noise (SFDR)[3]	–82	–82	–82	dB typ	
Intermodulation Distortion (IMD)[3]					
Second-Order Terms	–84	–84	–84	dB typ	fa = 100.73 kHz, fb = 90.72 kHz
Third-Order Terms	–84	–84	–84	dB typ	fa = 100.73 kHz, fb = 90.72 kHz
Aperture Delay	10	10	10	ns typ	
Aperture Jitter	30	30	30	ps typ	
Full Power Bandwidth	13.5	13.5	13.5	MHz typ	@ 3 dB
	2	2	2	MHz typ	@ 0.1 dB
DC ACCURACY					B and Y Grades[4]
Resolution	12	12	12	Bits	
Integral Nonlinearity[3]		±1.5	±1.5	LSB max	
	±0.75			LSB typ	
Differential Nonlinearity		–0.9/+1.5	–0.9/+1.5	LSB max	Guaranteed No Missed Codes to 12 Bits
	±0.75			LSB typ	
Offset Error[3, 5]		±1.5	±1.5	LSB max	
	±1.5	±0.2	±0.2	LSB typ	
Gain Error[3, 5]		±1.5	±1.5	LSB max	
	±1.5	±0.5	±0.5	LSB typ	
Total Unadjusted Error (TUE)[3, 5]		±2	±2	LSB max	
ANALOG INPUT					
Input Voltage Range	0 to V_{DD}	0 to V_{DD}	0 to V_{DD}	V	
DC Leakage Current	±0.5	±0.5	±0.5	µA max	
Input Capacitance	20	20	20	pF typ	Track-and-Hold in Track; 6 pF typ when in Hold
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4	2.4	2.4	V min	
	1.8	1.8	1.8	V min	V_{DD} = 2.35 V
Input Low Voltage, V_{INL}	0.8	0.8	0.8	V max	V_{DD} = 5 V
	0.4	0.4	0.4	V max	V_{DD} = 3 V
Input Current, I_{IN}, SCLK Pin	±0.5	±0.5	±0.5	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±10	±10	±10	nA typ	
Input Capacitance, C_{IN}[6]	5	5	5	pF max	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DD} – 0.2	V_{DD} – 0.2	V_{DD} – 0.2	V min	I_{SOURCE} = 200 µA; V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	0.4	0.4	V max	I_{SINK} = 200 µA
Floating-State Leakage Current	±1	±1	±1	µA max	
Floating-State Output Capacitance[6]	5	5	5	pF max	
Output Coding	Straight (Natural) Binary				
CONVERSION RATE					
Conversion Time	800	800	800	ns max	16 SCLK Cycles
Track-and-Hold Acquisition Time[3]	250	250	250	ns max	
Throughput Rate	1	1	1	MSPS max	See Serial Interface Section

Parameter	A Grade[2]	B Grade[2]	Y Grade[2]	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
V_{DD}	2.35/5.25	2.35/5.25	2.35/5.25	V min/max	
I_{DD}					Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2.5	2.5	2.5	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK ON or OFF
	1.2	1.2	1.2	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK ON or OFF
Normal Mode (Operational)	3.5	3.5	3.5	mA max	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS
	1.7	1.7	1.7	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode (Static)	1	1	1	μA max	Typically 50 nA
Full Power-Down Mode (Dynamic)	0.6	0.6	0.6	mA typ	V_{DD} = 5 V, f_{SAMPLE} = 100 kSPS
	0.3	0.3	0.3	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
Power Dissipation[7]					
Normal Mode (Operational)	17.5	17.5	17.5	mW max	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS
	5.1	5.1	5.1	mW max	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode	5	5	5	μW max	V_{DD} = 5 V
	3	3	3	μW max	V_{DD} = 3 V

NOTES
[1]Temperature ranges as follows: A, B Grades: –40°C to +85°C, Y Grade: –40°C to +125°C.
[2]Operational from V_{DD} = 2.0 V, with input low voltage (V_{INL}) 0.35 V max.
[3]See Terminology section.
[4]B and Y Grades, maximum specifications apply as typical figures when V_{DD} = 4.75 V to 5.25 V.
[5]SC70 values guaranteed by characterization.
[6]Guaranteed by characterization.
[7]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7477A–SPECIFICATIONS[1] (V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	61	dB min	
Total Harmonic Distortion (THD)[3]	–72	dB max	
Peak Harmonic or Spurious Noise (SFDR)[3]	–73	dB max	
Intermodulation Distortion (IMD)[3]			
Second-Order Terms	–82	dB typ	fa = 100.73 kHz, fb = 90.7 kHz
Third-Order Terms	–82	dB typ	fa = 100.73 kHz, fb = 90.7 kHz
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	13.5	MHz typ	@ 3 dB
	2	MHz typ	@ 0.1 dB
DC ACCURACY			
Resolution	10	Bits	
Integral Nonlinearity	±0.5	LSB max	
Differential Nonlinearity	±0.5	LSB max	Guaranteed No Missed Codes to 10 Bits
Offset Error[3, 4]	±1	LSB max	
Gain Error[3, 4]	±1	LSB max	
Total Unadjusted Error (TUE)[3, 4]	±1.2	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{DD}	V	
DC Leakage Current	±0.5	μA max	
Input Capacitance	20	pF typ	Track-and-Hold in Track; 6 pF typ when in Hold

Parameter	A Grade[2]	Unit	Test Conditions/Comments
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
	1.8	V min	V_{DD} = 2.35 V
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
Input Current, I_{IN}, SCLK Pin	±0.5	μA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±10	nA typ	
Input Capacitance, C_{IN}[5]	5	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 μA, V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 μA
Floating-State Leakage Current	±1	μA max	
Floating-State Output Capacitance[5]	5	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	700	ns max	14 SCLK Cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time[3]	250	ns max	
Throughput Rate	1	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2.5	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK ON or OFF
	1.2	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK ON or OFF
Normal Mode (Operational)	3.5	mA max	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS
	1.7	mA max	V_{DD} = 2.35 V to 3.6 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode (Static)	1	μA max	Typically 50 nA
Full Power-Down Mode (Dynamic)	0.6	mA typ	V_{DD} = 5 V, f_{SAMPLE} = 100 kSPS
	0.3	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
Power Dissipation[6]			
Normal Mode (Operational)	17.5	mW max	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS
	5.1	mW max	V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS
Full Power-Down Mode	5	μW max	V_{DD} = 5 V

NOTES
[1]Temperature range from –40°C to +85°C.
[2]Operational from V_{DD} = 2.0 V, with input high voltage (V_{INH}) 1.8 V min.
[3]See Terminology section.
[4]SC70 values guaranteed by characterization.
[5]Guaranteed by characterization.
[6]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

AD7478A–SPECIFICATIONS[1] (V_{DD} = 2.35 V to 5.25 V, f_{SCLK} = 20 MHz, f_{SAMPLE} = 1 MSPS, unless otherwise noted; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A Grade[2]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			f_{IN} = 100 kHz Sine Wave
Signal-to-Noise + Distortion (SINAD)[3]	49	dB min	
Total Harmonic Distortion (THD)[3]	–65	dB max	
Peak Harmonic or Spurious Noise (SFDR)[3]	–65	dB max	
Intermodulation Distortion (IMD)[3]			
Second-Order Terms	–76	dB typ	fa = 100.73 kHz, fb = 90.7 kHz
Third-Order Terms	–76	dB typ	fa = 100.73 kHz, fb = 90.7 kHz
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	13.5	MHz typ	@ 3 dB
	2	MHz typ	@ 0.1 dB

Parameter	A Grade[2]	Unit	Test Conditions/Comments
DC ACCURACY			
Resolution	8	Bits	
Integral Nonlinearity[3]	±0.3	LSB max	
Differential Nonlinearity[3]	±0.3	LSB max	Guaranteed No Missed Codes to Eight Bits
Offset Error[3, 4]	±0.3	LSB max	
Gain Error[3, 4]	±0.3	LSB max	
Total Unadjusted Error (TUE)[3, 4]	±0.5	LSB max	
ANALOG INPUT			
Input Voltage Range	0 to V_{DD}	V	
DC Leakage Current	±0.5	μA max	
Input Capacitance	20	pF typ	Track-and-Hold in Track; 6 pF typ when in Hold
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.4	V min	
	1.8	V min	V_{DD} = 2.35 V
Input Low Voltage, V_{INL}	0.8	V max	V_{DD} = 5 V
	0.4	V max	V_{DD} = 3 V
Input Current, I_{IN}, SCLK Pin	±0.5	μA max	Typically 10 nA, V_{IN} = 0 V or V_{DD}
Input Current, I_{IN}, $\overline{CS}$ Pin	±10	nA typ	
Input Capacitance, C_{IN}[5]	5	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DD} – 0.2	V min	I_{SOURCE} = 200 μA, V_{DD} = 2.35 V to 5.25 V
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 200 μA
Floating-State Leakage Current	±1	μA max	
Floating-State Output Capacitance[5]	5	pF max	
Output Coding	Straight (Natural) Binary		
CONVERSION RATE			
Conversion Time	600	ns max	12 SCLK Cycles with SCLK at 20 MHz
Track-and-Hold Acquisition Time[3]	225	ns max	
Throughput Rate	1.2	MSPS max	
POWER REQUIREMENTS			
V_{DD}	2.35/5.25	V min/max	
I_{DD}			Digital I/Ps = 0 V or V_{DD}
Normal Mode (Static)	2.5	mA typ	V_{DD} = 4.75 V to 5.25 V, SCLK ON or OFF
	1.2	mA typ	V_{DD} = 2.35 V to 3.6 V, SCLK ON or OFF
Normal Mode (Operational)	3.5	mA max	V_{DD} = 4.75 V to 5.25 V
	1.7	mA max	V_{DD} = 2.35 V to 3.6 V
Full Power-Down Mode (Static)	1	μA max	Typically 50 nA
Full Power-Down Mode (Dynamic)	0.6	mA typ	V_{DD} = 5 V, f_{SAMPLE} = 100 kSPS
	0.3	mA typ	V_{DD} = 3 V, f_{SAMPLE} = 100 kSPS
Power Dissipation[6]			
Normal Mode (Operational)	17.5	mW max	V_{DD} = 5 V
	5.1	mW max	V_{DD} = 3 V
Full Power-Down Mode	5	μW max	V_{DD} = 5 V

NOTES
[1]Temperature range from –40°C to +85°C.
[2]Operational from V_{DD} = 2.0 V, with input high voltage (V_{INH}) 1.8 V min.
[3]See Terminology section.
[4]SC70 values guaranteed by characterization.
[5]Guaranteed by characterization.
[6]See Power vs. Throughput Rate section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = 2.35 V to 5.25 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7476A/AD7477A/AD7478A	Unit	Description
f_{SCLK} [2]	10	kHz min[3]	A, B Grades
	20	kHz min[3]	Y Grade
	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}		AD7476A
	14 × t_{SCLK}		AD7477A
	12 × t_{SCLK}		AD7478A
t_{QUIET}	50	ns min	Minimum Quiet Time Required between Bus Relinquish and Start of Next Conversion
t_1	10	ns min	Minimum $\overline{CS}$ Pulse Width
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3 [4]	22	ns max	Delay from $\overline{CS}$ until SDATA Three-State Disabled
t_4 [4]	40	ns max	Data Access Time after SCLK Falling Edge
t_5	0.4 t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4 t_{SCLK}	ns min	SCLK High Pulse Width
t_7 [5]			SCLK to Data Valid Hold Time
	10	ns min	$V_{DD} \leq 3.3$ V
	9.5	ns min	3.3 V < $V_{DD} \leq 3.6$ V
	7	ns min	$V_{DD} > 3.6$ V
t_8 [6]	36	ns max	SCLK Falling Edge to SDATA High Impedance
	See Note 7	ns min	SCLK Falling Edge to SDATA High Impedance
$t_{POWER-UP}$ [8]	1	µs max	Power-Up Time from Full Power-Down

NOTES

[1]Guaranteed by characterization. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 V.

[2]Mark/space ratio for the SCLK input is 40/60 to 60/40.

[3]Minimum f_{SCLK} at which specifications are guaranteed.

[4]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 1.8 V when V_{DD} = 2.35 V and 0.8 V or 2.0 V for V_{DD} > 2.35 V.

[5]Measured with 50 pF load capacitor.

[6]t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

[7]t_7 values also apply to t_8 minimum values.

[8]See Power-Up Time section.

Specifications subject to change without notice.

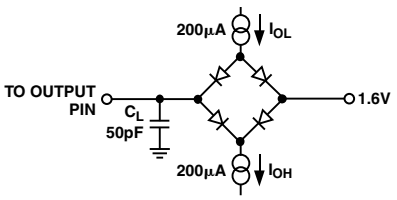


Figure 1. Load Circuit for Digital Output Timing Specifications

Timing Example 1

Having f_{SCLK} = 20 MHz and a throughput of 1 MSPS gives a cycle time of t_2 + 12.5 ($1/f_{SCLK}$) + t_{ACQ} = 1 µs. With t_2 = 10 ns min, this leaves t_{ACQ} to be 365 ns. This 365 ns satisfies the requirement of 250 ns for t_{ACQ}. From Figure 3, t_{ACQ} is comprised of 2.5 ($1/f_{SCLK}$) + t_8 + t_{QUIET}, where t_8 = 36 ns max. This allows a value of 204 ns for t_{QUIET}, satisfying the minimum requirement of 50 ns.

Timing Example 2

Having f_{SCLK} = 5 MHz and a throughput of 315 kSPS gives a cycle time of t_2 + 12.5 ($1/f_{SCLK}$) + t_{ACQ} = 3.174 µs. With t_2 = 10 ns min, this leaves t_{ACQ} to be 664 ns. This 664 ns satisfies the requirement of 250 ns for t_{ACQ}. From Figure 3, t_{ACQ} is comprised of 2.5 ($1/f_{SCLK}$) + t_8 + t_{QUIET}, t_8 = 36 ns max. This allows a value of 128 ns for t_{QUIET}, satisfying the minimum requirement of 50 ns. As in this example and with other slower clock values, the signal may already be acquired before the conversion is complete, but it is still necessary to leave 50 ns minimum t_{QUIET} between conversions. In Example 2, the signal should be fully acquired at approximately Point C in Figure 3.

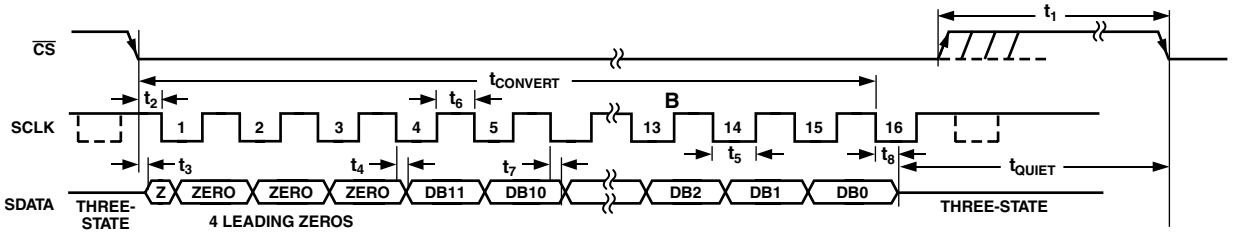


Figure 2. AD7476A Serial Interface Timing Diagram

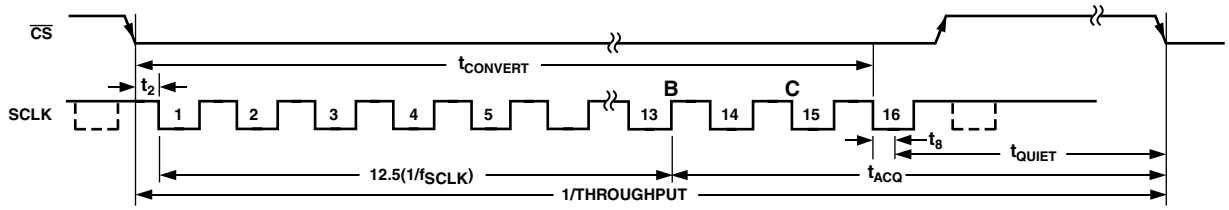


Figure 3. Serial Interface Timing Example

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +7 V
Analog Input Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to GND . . . . . –0.3 V to +7 V
Digital Output Voltage to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Input Current to Any Pin except Supplies[2] . . . . . ±10 mA
Operating Temperature Range
  Commercial (A and B Grades) . . . . . –40°C to +85°C
  Industrial (Y Grade) . . . . . –40°C to +125°C
  Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
MSOP Package
  θ_{JA} Thermal Impedance . . . . . 205.9°C/W
  θ_{JC} Thermal Impedance . . . . . 43.74°C/W
SC70 Package
  θ_{JA} Thermal Impedance . . . . . 340.2°C/W
  θ_{JC} Thermal Impedance . . . . . 228.9°C/W
Lead Temperature, Soldering
  Reflow (10 sec to 30 sec) . . . . . 235 (0/+5)°C
Pb-free Temperature Soldering
  Reflow . . . . . 255 (0/+5)°C
ESD . . . . . 3.5 kV

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Transient currents of up to 100 mA will not cause SCR latch-up.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment, and can discharge without detection. Although the AD7476A/AD7477A/AD7478A feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Linearity Error (LSB)[1]	Package Option[2]	Branding
AD7476AAKS-500RL7	–40°C to +85°C	±0.75 typ	KS-6	CEZ
AD7476AAKS-REEL	–40°C to +85°C	±0.75 typ	KS-6	CEZ
AD7476AAKS-REEL7	–40°C to +85°C	±0.75 typ	KS-6	CEZ
AD7476ABKS-500RL7	–40°C to +85°C	±1.5 max	KS-6	CEY
AD7476ABKS-REEL	–40°C to +85°C	±1.5 max	KS-6	CEY
AD7476ABKS-REEL7	–40°C to +85°C	±1.5 max	KS-6	CEY
AD7476ABKSZ-REEL[3]	–40°C to +85°C	±1.5 max	KS-6	CEY
AD7476ABKSZ-REEL7[3]	–40°C to +85°C	±1.5 max	KS-6	CEY
AD7476ABRM	–40°C to +85°C	±1.5 max	RM-8	CEY
AD7476ABRM-REEL	–40°C to +85°C	±1.5 max	RM-8	CEY
AD7476ABRM-REEL7	–40°C to +85°C	±1.5 max	RM-8	CEY
AD7476AYKS-500RL7	–40°C to +125°C	±1.5 max	KS-6	CEW
AD7476AYKS-REEL7	–40°C to +125°C	±1.5 max	KS-6	CEW
AD7476AYKSZ-500RL7[3]	–40°C to +125°C	±1.5 max	KS-6	CEW
AD7476AYKSZ-REEL7[3]	–40°C to +125°C	±1.5 max	KS-6	CEW
AD7476AYRM	–40°C to +125°C	±1.5 max	RM-8	CEW
AD7476AYRM-REEL7	–40°C to +125°C	±1.5 max	RM-8	CEW
EVAL-AD7476ACB[4]			Evaluation Board	
AD7477AAKS-500RL7	–40°C to +85°C	±0.5 max	KS-6	CFZ
AD7477AAKS-REEL	–40°C to +85°C	±0.5 max	KS-6	CFZ
AD7477AAKS-REEL7	–40°C to +85°C	±0.5 max	KS-6	CFZ
AD7477AAKSZ-REEL[3]	–40°C to +85°C	±0.5 max	KS-6	CFZ
AD7477AAKSZ-REEL7[3]	–40°C to +85°C	±0.5 max	KS-6	CFZ
AD7477AARM	–40°C to +85°C	±0.5 max	RM-8	CFZ
AD7477AARM-REEL	–40°C to +85°C	±0.5 max	RM-8	CFZ
AD7477AARM-REEL7	–40°C to +85°C	±0.5 max	RM-8	CFZ
EVAL-AD7477ACB[4]			Evaluation Board	
AD7478AAKS-500RL7	–40°C to +85°C	±0.3 max	KS-6	CJZ
AD7478AAKS-REEL	–40°C to +85°C	±0.3 max	KS-6	CJZ
AD7478AAKS-REEL7	–40°C to +85°C	±0.3 max	KS-6	CJZ
AD7478AAKSZ-500RL7[3]	–40°C to +85°C	±0.3 max	KS-6	CJZ
AD7478AAKSZ-REEL[3]	–40°C to +85°C	±0.3 max	KS-6	CJZ
AD7478AAKSZ-REEL7[3]	–40°C to +85°C	±0.3 max	KS-6	CJZ
AD7478AARM	–40°C to +85°C	±0.3 max	RM-8	CJZ
AD7478AARM-REEL	–40°C to +85°C	±0.3 max	RM-8	CJZ
AD7478AARM-REEL7	–40°C to +85°C	±0.3 max	RM-8	CJZ
EVAL-CONTROL BRD2[5]			Evaluation Control Board	

NOTES

[1]Linearity error here refers to integral nonlinearity.

[2]KS = SC70; RM = MSOP.

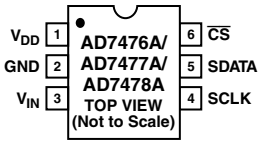
[3]Z = Pb-free part.

[4]This can be used as a standalone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.

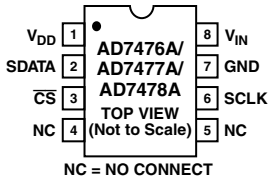
[5]This board is a complete unit, allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designator. To order a complete evaluation kit, you will need to order the particular ADC evaluation board, e.g., EVAL-AD7476ACB, the EVAL-CONTROLBRD2, and a 12 V ac transformer. See relevant evaluation board application note for more information.

PIN CONFIGURATIONS

6-Lead SC70



8-Lead MSOP



PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476A/AD7477A/AD7478A and also frames the serial data transfer.
V_{DD}	Power Supply Input. The V_{DD} range for the AD7476A/AD7477A/AD7478A is from 2.35 V to 5.25 V.
GND	Analog Ground. Ground reference point for all circuitry on the AD7476A/AD7477A/AD7478A. All analog input signals should be referred to this GND voltage.
V_{IN}	Analog Input. Single-ended analog input channel. The input range is 0 V to V_{DD}.
SDATA	Data Out. Logic output. The conversion result from the AD7476A/AD7477A/AD7478A is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476A consists of four leading zeros followed by the 12 bits of conversion data, which are provided MSB first. The data stream from the AD7477A consists of four leading zeros followed by the 10 bits of conversion data followed by two trailing zeros, provided MSB first. The data stream from the AD7478A consists of four leading zeros followed by the 8 bits of conversion data followed by four trailing zeros, which are provided MSB first.
SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476A/AD7477A/AD7478A's conversion process.
NC	No Connect.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. For the AD7476A/AD7477A/AD7478A, the endpoints of the transfer function are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e., AGND + 1 LSB.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal, i.e., V_{REF} – 1 LSB after the offset error has been adjusted out.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±0.5 LSB, after the end of conversion. See the Serial Interface section for more details.

Signal-to-(Noise + Distortion) Ratio (SINAD)
This is the measured ratio of signal-to-(noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\textit{Signal-to-(Noise + Distortion)} = (6.02\ N + 1.76)\ \text{dB}$$

Thus, it is 74 dB for a 12-bit converter, 62 dB for a 10-bit converter, and 50 dB for an 8-bit converter.

Total Unadjusted Error (TUE)
This is a comprehensive specification that includes the gain, linearity, and offset errors.

Total Harmonic Distortion (THD)
Total harmonic distortion is the ratio of the rms sum of harmonics to the fundamental. It is defined as

$$THD\,(\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise (SFDR)
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum. But for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion (IMD)
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second-order terms include (fa + fb) and (fa – fb), while the third-order terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb).

The AD7476A/AD7477A/AD7478A are tested using the CCIF standard where two input frequencies are used (see fa and fb on the specification pages). In this case, the second-order terms are usually distanced in frequency from the original sine waves, while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

AD7476A/AD7477A/AD7478A–Typical Performance Characteristics

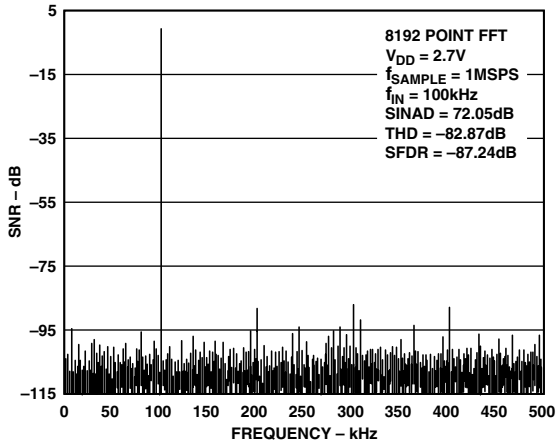
TPC 1, TPC 2, and TPC 3 each show a typical FFT plot for the AD7476A, AD7477A, and AD7478A, respectively, at a 1 MSPS sample rate and 100 kHz input frequency.

TPC 4 shows the signal-to-(noise + distortion) ratio performance versus the input frequency for various supply voltages while sampling at 1 MSPS with an SCLK frequency of 20 MHz for the AD7476A.

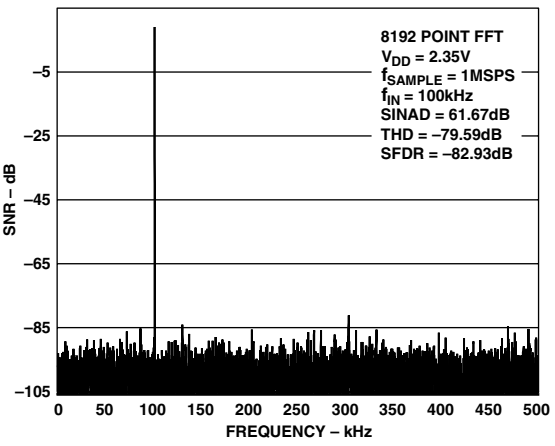
TPC 5 and TPC 6 show INL and DNL performance for the AD7476A.

TPC 7 shows a graph of the total harmonic distortion versus the analog input frequency for different source impedances when using a supply voltage of 3.6 V and sampling at a rate of 1 MSPS (see Analog Input section).

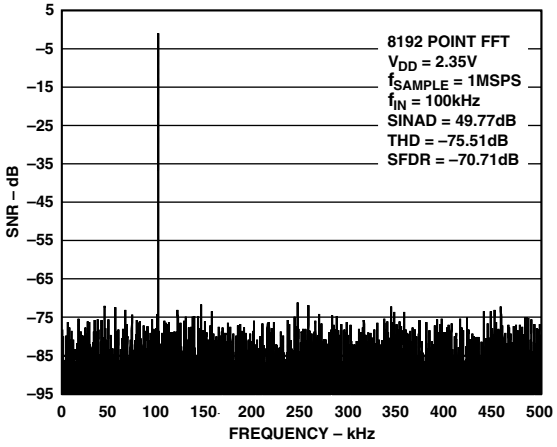
TPC 8 shows a graph of the total harmonic distortion versus the analog input signal frequency for various supply voltages while sampling at 1 MSPS with an SCLK frequency of 20 MHz.



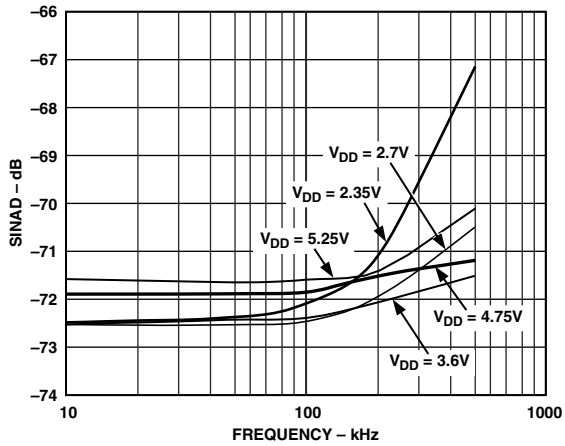
TPC 1. AD7476A Dynamic Performance at 1 MSPS



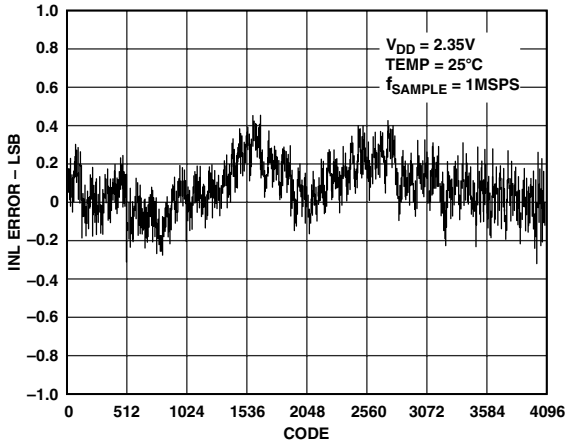
TPC 2. AD7477A Dynamic Performance at 1 MSPS



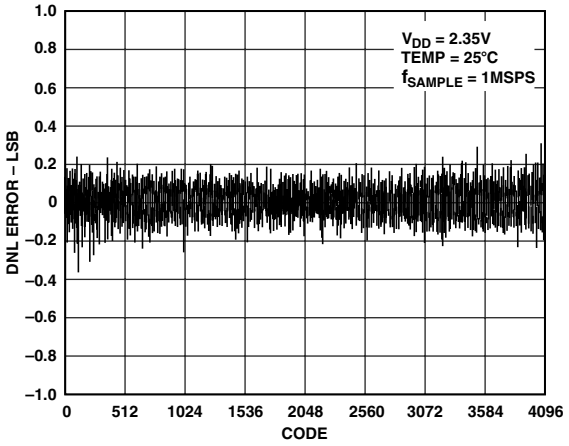
TPC 3. AD7478A Dynamic Performance at 1 MSPS



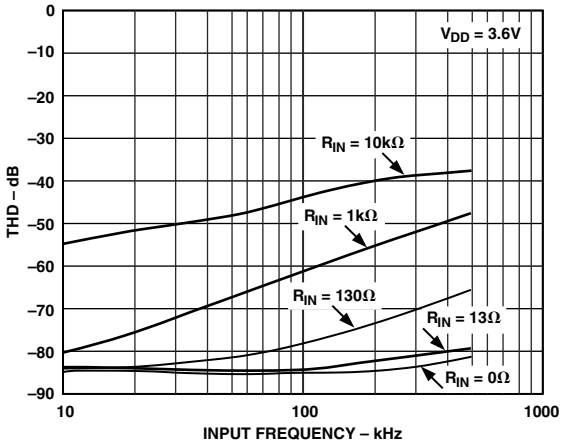
TPC 4. AD7476A SINAD vs. Input Frequency at 1 MSPS



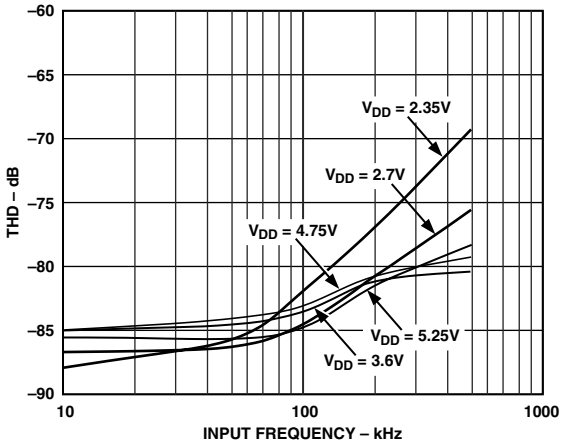
TPC 5. AD7476A INL Performance



TPC 6. AD7476A DNL Performance



TPC 7. THD vs. Analog Input Frequency for Various Source Impedances



TPC 8. THD vs. Analog Input Frequency for Various Supply Voltages

CIRCUIT INFORMATION

The AD7476A/AD7477A/AD7478A are fast, micropower, 12-/10-/8-bit, single-supply A/D converters, respectively. The parts can be operated from a 2.35 V to 5.25 V supply. When operated from either a 5 V supply or a 3 V supply, the AD7476A/AD7477A/AD7478A are capable of throughput rates of 1 MSPS when provided with a 20 MHz clock.

The AD7476A/AD7477A/AD7478A provide the user with an on-chip, track-and-hold A/D converter and a serial interface housed in a tiny 6-lead SC70 or 8-lead MSOP package, which offer the user considerable space-saving advantages over alternative solutions. The serial clock input accesses data from the part but also provides the clock source for the successive-approximation A/D converter. The analog input range is 0 V to V_{DD}. The ADC does not require an external reference or an on-chip reference. The reference for the AD7476A/AD7477A/AD7478A is derived from the power supply and thus gives the widest dynamic input range.

The AD7476A/AD7477A/AD7478A also feature a power-down option to allow power saving between conversions. The power-down feature is implemented across the standard serial interface, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7476A/AD7477A/AD7478A is a successive-approximation, analog-to-digital converter based around a charge redistribution DAC. Figures 4 and 5 show simplified schematics of the ADC. Figure 4 shows the ADC during its acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on V_{IN}.

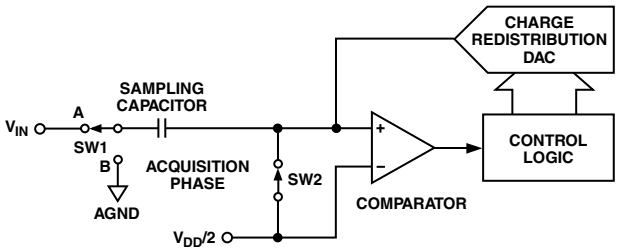


Figure 4. ADC Acquisition Phase

When the ADC starts a conversion, see Figure 5, SW2 will open and SW1 will move to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 6 shows the ADC transfer function.

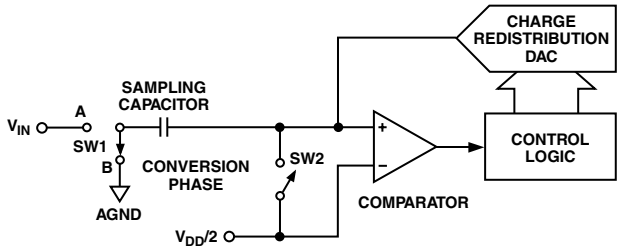


Figure 5. ADC Conversion Phase

ADC TRANSFER FUNCTION

The output coding of the AD7476A/AD7477A/AD7478A is straight binary.

The designed code transitions occur at the successive integer LSB values, i.e., 1 LSB, 2 LSB, and so on. The LSB size is $V_{DD}/4096$ for the AD7476A, $V_{DD}/1024$ for the AD7477A, and $V_{DD}/256$ for the AD7478A. The ideal transfer characteristic for the AD7476A/AD7477A/AD7478A is shown in Figure 6.

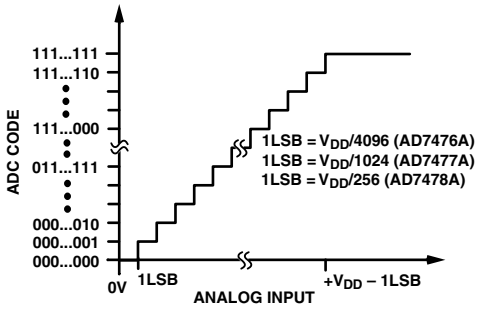


Figure 6. AD7476A/AD7477A/AD7478A Transfer Characteristic

TYPICAL CONNECTION DIAGRAM

Figure 7 shows a typical connection diagram for the AD7476A/AD7477A/AD7478A. V_{REF} is taken internally from V_{DD} and, as such, V_{DD} should be well decoupled. This provides an analog input range of 0 V to V_{DD}. The conversion result is output in a 16-bit word with four leading zeros followed by the MSB of the 12-bit, 10-bit, or 8-bit result. The 10-bit result from the AD7477A will be followed by two trailing zeros, and the 8-bit result from the AD7478A will be followed by four trailing zeros.

Alternatively, because the supply current required by the AD7476A/AD7477A/AD7478A is so low, a precision reference can be used as the supply source to the AD7476A/AD7477A/AD7478A. A REF19x voltage reference (REF195 for 5 V or REF193 for 3 V) can be used to supply the required voltage to the ADC (see Figure 7). This configuration is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V (e.g., 15 V). The REF19x will output a steady voltage to the AD7476A/AD7477A/AD7478A. If the low dropout REF193 is used, the current it needs to supply to the AD7476A/AD7477A/AD7478A is typically 1.2 mA. When the ADC is converting at a rate of 1 MSPS, the REF193 will need to supply a maximum of 1.7 mA to the AD7476A/AD7477A/AD7478A. The load regulation of the REF193 is typically 10 ppm/mA (V_S = 5 V), which results in an error of 17 ppm (51 μV) for the 1.7 mA drawn from it. This corresponds to a 0.069 LSB error for the AD7476A with V_{DD} = 3 V from the REF193, a 0.017 LSB error for the AD7477A, and a 0.0043 LSB error for the AD7478A. For applications where power consumption is of concern, the power-down mode of the ADC and the sleep mode of the REF19x reference should be used to improve power performance. See the Modes of Operation section.

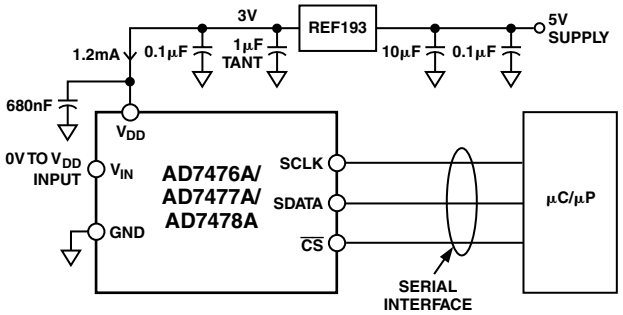


Figure 7. REF193 as Power Supply to AD7476A/AD7477A/AD7478A

Table I provides some typical performance data with various references used as a V_{DD} source for a 100 kHz input tone at room temperature under the same setup conditions.

Table I. AD7476A Typical Performance for Various Voltage References IC

Reference Tied to V_{DD}	AD7476A SNR Performance (dB)
AD780 @ 3 V	72.65
REF193	72.35
AD780 @ 2.5 V	72.5
REF192	72.2
REF43	72.6

Analog Input

Figure 8 shows an equivalent circuit of the analog input structure of the AD7476A/AD7477A/AD7478A. The two diodes, D1 and D2, provide ESD protection for the analog input. Care must be taken to ensure that the analog input signal never exceeds the supply rails by more than 300 mV. This will cause these diodes to become forward-biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the part is 10 mA. The capacitor C1 in Figure 8 is typically about 6 pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on resistance of a switch. This resistor is typically about 100 Ω. The capacitor C2 is the ADC sampling capacitor and has a capacitance of 20 pF typically. For ac applications, removing high frequency components from the analog input signal is recommended by use of a band-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op amp will be a function of the particular application.

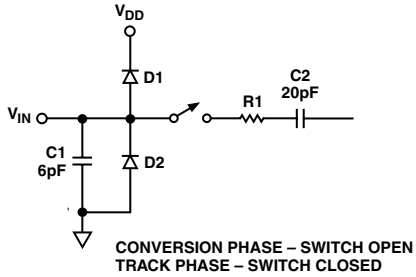


Figure 8. Equivalent Analog Input Circuit

Table II provides some typical performance data with various op amps used as the input buffer for a 100 kHz input tone at room temperature under the same setup conditions.

Table II. AD7476A Typical Performance with Various Input Buffers, V_{DD} = 3 V

Op Amp in the Input Buffer	AD7476A SNR Performance (dB)
AD711	72.3
AD797	72.5
AD845	71.4

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion (THD) that can be tolerated. The THD will increase as the source impedance increases and the performance will degrade. See TPC 7.

Digital Inputs

The digital inputs applied to the AD7476A/AD7477A/AD7478A are not limited by the maximum ratings that limit the analog input. Instead, the digital inputs applied can go to 7 V and are not restricted by the V_{DD} + 0.3 V limit as on the analog input. For example, if the AD7476A/AD7477A/AD7478A were operated with a V_{DD} of 3 V, then 5 V logic levels could be used on the digital inputs. However, it is important to note that the data output on SDATA will still have 3 V logic levels when V_{DD} = 3 V. Another advantage of SCLK and $\overline{CS}$ not being restricted by the V_{DD} + 0.3 V limit is the fact that power supply sequencing issues are avoided. If $\overline{CS}$ or SCLK is applied before V_{DD}, there is no risk of latch-up as there would be on the analog input if a signal greater than 0.3 V was applied prior to V_{DD}.

MODES OF OPERATION

The mode of operation of the AD7476A/AD7477A/AD7478A is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are two possible modes of operation: normal and power-down. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine whether the AD7476A/AD7477A/AD7478A will enter power-down mode or not. Similarly, if already in power-down, $\overline{CS}$ can control whether the device will return to normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for different application requirements.

Normal Mode

This mode is intended for the fastest throughput rate performance; the user does not have to worry about any power-up times with the AD7476A/AD7477A/AD7478A remaining fully powered all the time. Figure 9 shows the general diagram of the operation of the AD7476A/AD7477A/AD7478A in this mode.

The conversion is initiated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure that the part remains fully powered up at all times, $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the end of the $t_{CONVERT}$, the part will remain powered up, but the conversion will be terminated and SDATA will go back into three-state.

For the AD7476A, 16 serial clock cycles are required to complete the conversion and access the complete conversion results. For the AD7477A and AD7478A, a minimum of 14 and 12 serial clock cycles are required to complete the conversion and access the complete conversion results, respectively.

$\overline{CS}$ may idle high until the next conversion or may idle low until $\overline{CS}$ returns high sometime prior to the next conversion (effectively idling $\overline{CS}$ low).

Once a data transfer is complete (SDATA has returned to three-state), another conversion can be initiated after the quiet time, t_{QUIET}, has elapsed by bringing $\overline{CS}$ low again.

Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions is performed at a high throughput rate and the ADC is then powered down for a relatively long duration between these bursts of several conversions. When the AD7476A/AD7477A/AD7478A is in power-down, all analog circuitry is powered down.

To enter power-down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the 10th falling edge of SCLK, as shown in Figure 10. Once $\overline{CS}$ has been brought high in this window of SCLKs, the part will enter power-down, the conversion that was initiated by the falling edge of $\overline{CS}$ will be terminated, and SDATA will go back into three-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, the part will remain in normal mode and will not power down. This will avoid accidental power-down due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power up the AD7476A/AD7477A/AD7478A again, a dummy conversion is performed. On the falling edge of $\overline{CS}$, the device will begin to power up and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the 10th SCLK. The device will be fully powered up once 16 SCLKs have elapsed, and valid data will result from the next conversion as shown in Figure 11. If $\overline{CS}$ is brought high before the 10th falling edge of SCLK, then the AD7476A/AD7477A/AD7478A will go back into power-down. This avoids accidental power-up due to glitches on the $\overline{CS}$ line or an inadvertent burst of eight SCLK cycles while $\overline{CS}$ is low. So although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$ as long as it occurs before the 10th SCLK falling edge.

Power-Up Time

The power-up time of the AD7476A/AD7477A/AD7478A is 1 μs, which means that with any frequency of SCLK up to 20 MHz, one dummy cycle will always be sufficient to allow the device to power up. Once the dummy cycle is complete, the ADC will be fully powered up and the input signal will be acquired properly. The quiet time, t_{QUIET}, must still be allowed from the point where the bus goes back into three-state after the dummy conversion to the next falling edge of $\overline{CS}$. When running at a 1 MSPS throughput rate, the AD7476A/AD7477A/AD7478A will power up and acquire a signal within ±0.5 LSB in one dummy cycle, i.e., 1 μs.

When powering up from the power-down mode with a dummy cycle, as in Figure 11, the track-and-hold that was in hold mode while the part was powered down returns to track mode after the first SCLK edge the part receives after the falling edge of $\overline{CS}$. This is shown as Point A in Figure 11. Although at any

SCLK frequency one dummy cycle is sufficient to power up the device and acquire V_{IN}, it does not necessarily mean that a full dummy cycle of 16 SCLKs must always elapse to power up the device and acquire V_{IN} fully; 1 µs will be sufficient to power up the device and acquire the input signal. If, for example, a 5 MHz SCLK frequency was applied to the ADC, the cycle time would be 3.2 µs. In one dummy cycle, 3.2 µs, the part would be powered up and V_{IN} acquired fully. However, after 1 µs with a 5 MHz SCLK, only five SCLK cycles would have elapsed. At this stage, the ADC would be fully powered up and the signal acquired. In this case, the $\overline{CS}$ can be brought high after the 10th SCLK falling edge and brought low again after a time, t_{QUIET}, to initiate the conversion.

When power supplies are first applied to the AD7476A/AD7477A/AD7478A, the ADC may power up in either the power-down or normal mode. Because of this, it is best to allow a dummy cycle to elapse to ensure that the part is fully powered up before attempting a valid conversion. Likewise, if it is intended to keep the part in the power-down mode while not in use and the user wishes the part to power up in power-down mode, the dummy cycle may be used to ensure that the device is in power-down by executing a cycle such as that shown in Figure 10. Once supplies are applied to the AD7476A/AD7477A/AD7478A, the power-up time is the same as that when powering up from the power-down mode. It takes approximately 1 µs to power up fully if the part powers up in normal mode. It is not necessary to wait 1 µs before executing a dummy cycle to ensure the desired mode of operation. Instead, the dummy cycle can occur directly after power is supplied to the ADC. If the first valid conversion is performed directly after the dummy conversion, care must be taken to ensure that an adequate acquisition time has been allowed. As mentioned earlier, when powering up from the power-down mode, the part will return to track upon the first SCLK edge applied after the falling edge of $\overline{CS}$. However, when the ADC powers up initially after supplies are applied, the track-and-hold will already be in track. This means, assuming one has the facility to monitor the ADC supply current, if the ADC powers up in the desired mode of operation and thus a dummy cycle is not required to change the mode, a dummy cycle is not required to place the track-and-hold into track.

POWER VS. THROUGHPUT RATE

By using the power-down mode on the AD7476A/AD7477A/AD7478A when not converting, the average power consumption of the ADC decreases at lower throughput rates. Figure 12 shows how as the throughput rate is reduced, the device remains in its power-down state longer and the average power consumption over time drops accordingly.

For example, if the AD7476A/AD7477A/AD7478A are operated in a continuous sampling mode with a throughput rate of 100 kSPS and an SCLK of 20 MHz (V_{DD} = 5 V) and the devices are placed in the power-down mode between conversions, the power consumption is calculated as follows. The power dissipation during normal operation is 17.5 mW (V_{DD} = 5 V). If the power-up time is one dummy cycle, i.e., 1 µs, and the remaining conversion

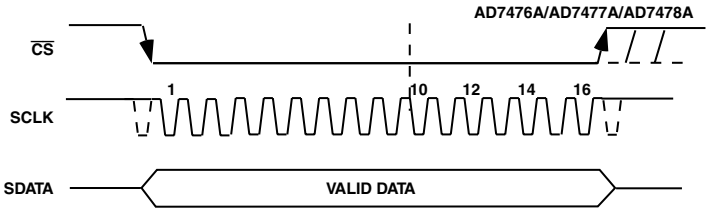


Figure 9. Normal Mode Operation

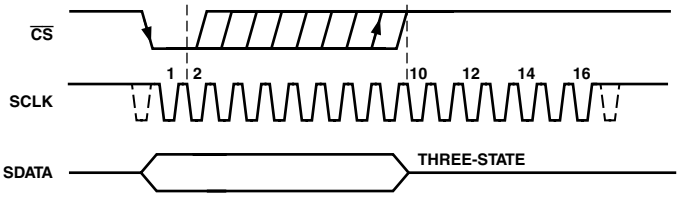


Figure 10. Entering Power-Down Mode

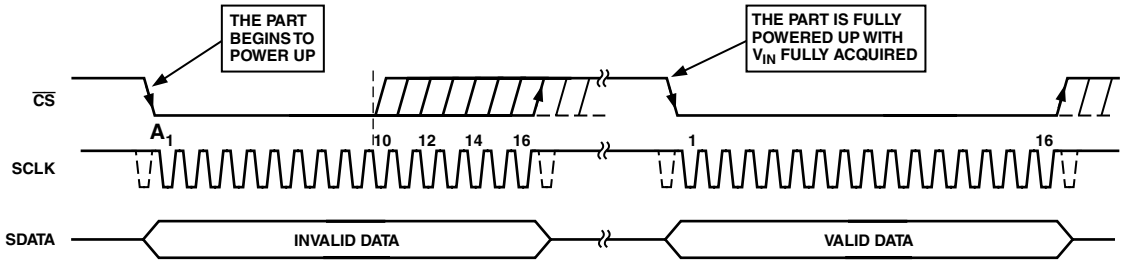


Figure 11. Exiting Power-Down Mode

time is another cycle, i.e., 1 µs, the AD7476A/AD7477A/AD7478A can be said to dissipate 17.5 mW for 2 µs during each conversion cycle. If the throughput rate is 100 kSPS, the cycle time is 10 µs and the average power dissipated during each cycle is (2/10) × (17.5 mW) = 3.5 mW. If V_{DD} = 3 V, SCLK = 20 MHz, and the devices are again in power-down mode between conversions, then the power dissipation during normal operation is 5.1 mW. The AD7476A/AD7477A/AD7478A can now be said to dissipate 5.1 mW for 2 µs during each conversion cycle. With a throughput rate of 100 kSPS, the average power dissipated during each cycle is (2/10) × (5.1 mW) = 1.02 mW. Figure 12 shows the power versus the throughput rate when using the power-down mode between conversions with both 5 V and 3 V supplies.

The power-down mode is intended for use with throughput rates of approximately 333 kSPS and under, since at higher sampling rates there is no power saving made by using the power-down mode.

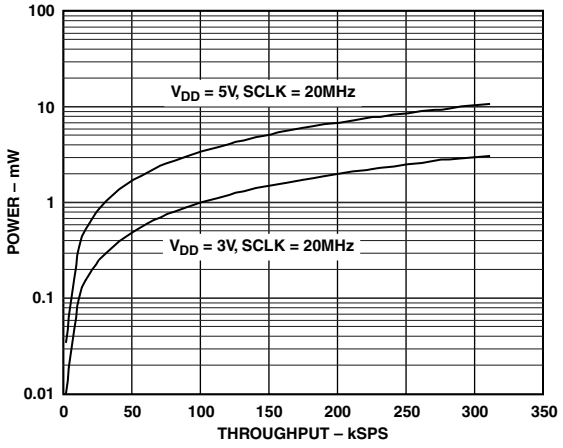


Figure 12. Power vs. Throughput

SERIAL INTERFACE

Figures 13, 14, and 15 show the detailed timing diagrams for serial interfacing to the AD7476A, AD7477A, and AD7478A, respectively. The serial clock provides the conversion clock and also controls the transfer of information from the AD7476A/AD7477A/AD7478A during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track-and-hold into hold mode and takes the bus out of three-state; the analog input is sampled at this point. Also, the conversion is initiated at this point.

For the AD7476A, the conversion will require 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold will go back into track on the next SCLK rising edge, as shown in Figure 13 at Point B. On the 16th SCLK falling edge, the SDATA line will go back into three-state. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated and the SDATA line will go back into three-state; otherwise, SDATA returns to three-state on the 16th SCLK falling edge, as shown in Figure 13. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7476A.

For the AD7477A, the conversion will require 14 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, the track-and-hold will go back into track on the next rising edge as shown in Figure 14 at Point B. If the rising edge of $\overline{CS}$ occurs before 14 SCLKs have elapsed, the conversion will be terminated and the SDATA line will go back into three-state. If 16 SCLKs are considered in the cycle, SDATA will return to three-state on the 16th SCLK falling edge, as shown in Figure 14.

For the AD7478A, the conversion will require 12 SCLK cycles to complete. The track-and-hold will go back into track on the rising edge after the 11th falling edge, as shown in Figure 15 at Point B. If the rising edge of $\overline{CS}$ occurs before 12 SCLKs have

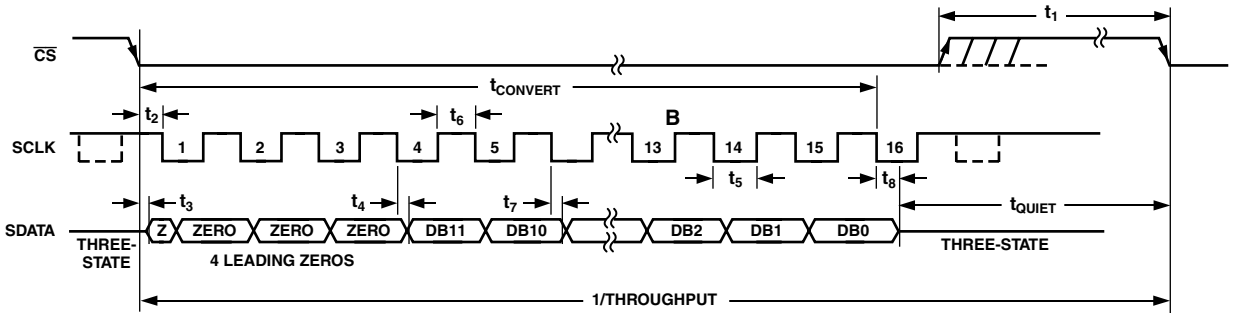


Figure 13. AD7476A Serial Interface Timing Diagram

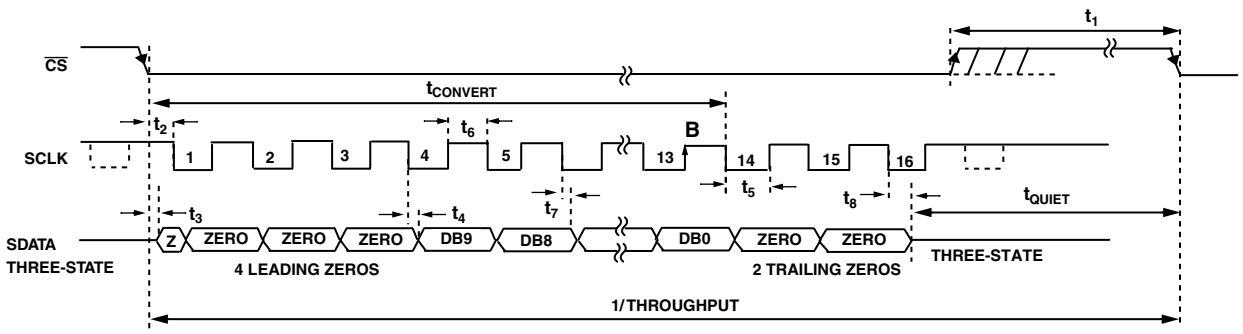


Figure 14. AD7477A Serial Interface Timing Diagram

elapsed, the conversion will be terminated and the SDATA line will go back into three-state. If 16 SCLKs are considered in the cycle, SDATA will return to three-state on the 16th SCLK falling edge, as shown in Figure 15.

$\overline{CS}$ going low clocks out the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the second leading zero. Thus, the first falling clock edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. For the AD7476A, the final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge. In this case, the first falling edge of SCLK will clock out the second leading zero, which can be read in the first rising edge. However, the first leading zero that was clocked out when $\overline{CS}$ went low will be missed, unless it was not read in the first falling edge. The 15th falling edge of SCLK will clock out the last bit and it could be read in the 15th rising SCLK edge.

If $\overline{CS}$ goes low just after one SCLK falling edge has elapsed, $\overline{CS}$ will clock out the first leading zero as it did before, and it may be read in the SCLK rising edge. The next SCLK falling edge will clock out the second leading zero, and it may be read in the following rising edge.

AD7478A in a 12 SCLK Cycle Serial Interface

For the AD7478A, if $\overline{CS}$ is brought high in the 12th rising edge after the four leading zeros and the eight bits of the conversion have been provided, the part can achieve a 1.2 MSPS throughput rate. For the AD7478A, the track-and-hold goes back into track in the 11th rising edge. In this case, a f_{SCLK} = 20 MHz and a throughput of 1.2 MSPS give a cycle time of t_2 +10.5 ($1/f_{SCLK}$) + t_{ACQ} = 833 ns. With t_2 = 10 ns min, this leaves t_{ACQ} to be 298 ns. This 298 ns satisfies the requirement of 225 ns for t_{ACQ}. From Figure 16, t_{ACQ} is comprised of 0.5 ($1/f_{SCLK}$) + t_8 + t_{QUIET}, where t_8 = 36 ns max. This allows a value of 237 ns for t_{QUIET}, satisfying the minimum requirement of 50 ns.

MICROPROCESSOR INTERFACING

The serial interface on the AD7476A/AD7477A/AD7478A allows the part to be directly connected to a range of different microprocessors. This section explains how to interface the AD7476A/AD7477A/AD7478A with some of the more common microcontroller and DSP serial interface protocols.

AD7476A/AD7477A/AD7478A to TMS320C541 Interface

The serial interface on the TMS320C541 uses a continuous serial clock and frame synchronization signals to synchronize the data transfer operations with peripheral devices, such as the AD7476A/AD7477A/AD7478A. The $\overline{CS}$ input allows easy interfacing between the TMS320C541 and the AD7476A/AD7477A/AD7478A without any glue logic required. The serial port of the TMS320C541 is set up to operate in burst mode (FSM = 1 in the serial port control register, SPC) with internal serial clock CLKX (MCM = 1 in the SPC register) and internal frame signal (TXM = 1 in the SPC register), so both pins are configured as outputs. For the AD7476A, the word length should be set to 16 bits (FO = 0 in the SPC register). This DSP only allows frames with a word length of 16 bits or 8 bits. Therefore, in the case of the AD7477A and AD7478A where 14 bits and 12 bits were required, the FO bit would be set up to 16 bits. This means to obtain the conversion result, 16 SCLKs are needed. In both situations, the remaining SCLKs will clock out trailing zeros. For the AD7477A, two trailing zeros will be clocked out in the last two clock cycles; for the AD7478A, four trailing zeros will be clocked out.

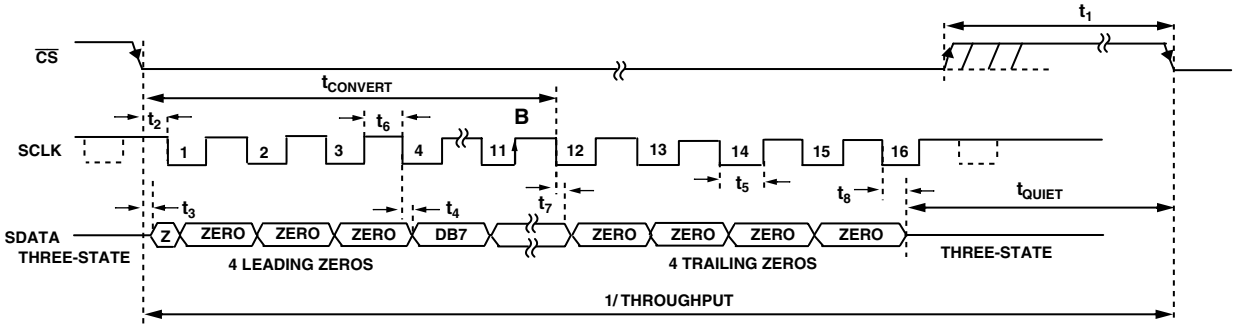


Figure 15. AD7478A Serial Interface Timing Diagram

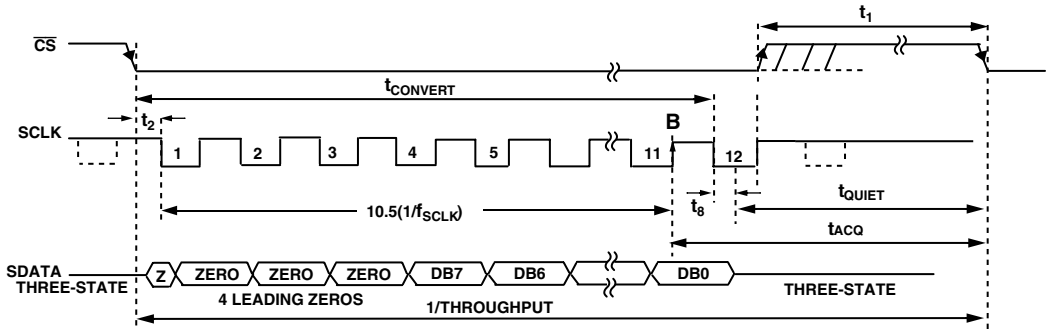


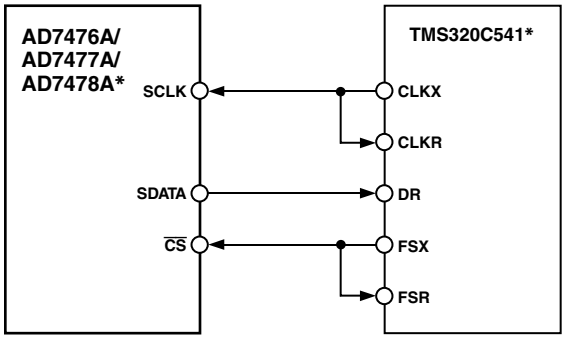
Figure 16. AD7478A in a 12 SCLK Cycle Serial Interface

To summarize, the values in the SPC register are

FO = 0
FSM = 1
MCM = 1
TXM = 1

The format bit, FO, may be set to 1 to set the word length to eight bits in order to implement the power-down mode on the AD7476A/AD7477A/AD7478A.

The connection diagram is shown in Figure 17. It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the TMS320C541 provides equidistant sampling.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 17. Interfacing to the TMS320C541

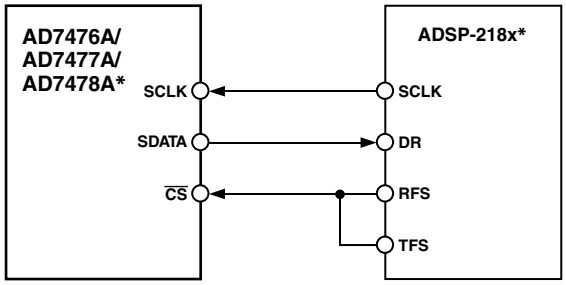
AD7476A/AD7477A/AD7478A to ADSP-218x
The ADSP-218x family of DSPs are interfaced directly to the AD7476A/AD7477A/AD7478A without any glue logic required. The SPORT control register should be set up as follows:

TFSW = RFSW = 1, Alternate Framing
INVRFS = INVTFS = 1, Active Low Frame Signal
DTYPE = 00, Right Justify Data
ISCLK = 1, Internal Serial Clock
TFSR = RFSR = 1, Frame Every Word
IRFS = 0, Sets Up RFS as an Input
ITFS = 1, Sets Up TFS as an Output
SLEN = 1111, 16 Bits for the AD7476A
SLEN = 1101, 14 Bits for the AD7477A
SLEN = 1011, 12 Bits for the AD7478A

To implement the power-down mode, SLEN should be set to 0111 to issue an 8-bit SCLK burst. The connection diagram is shown in Figure 18. The ADSP-218x has the TFS and RFS of the SPORT tied together, with TFS set as an output and RFS set as an input. The DSP operates in alternate framing mode, and the SPORT control register is set up as described. The frame synchronization signal generated on the TFS is tied to $\overline{CS}$, and, as with all signal processing applications, equidistant sampling is necessary. However, in this example, the timer interrupt is used to control the sampling rate of the ADC and, under certain conditions, equidistant sampling may not be achieved.

The timer registers, for example, are loaded with a value that will provide an interrupt at the required sample interval. When an interrupt is received, a value is transmitted with TFS/DT (ADC control word). The TFS is used to control the RFS and thus the reading of data. The frequency of the serial clock is set in the SCLKDIV register. When the instruction to transmit with TFS is given, i.e., TX0 = AX0, the state of the SCLK is checked. The DSP will wait until the SCLK has gone high, low, and high before transmission will start. If the timer and SCLK values are chosen such that the instruction to transmit occurs on or near the rising edge of SCLK, the data may be transmitted or it may wait until the next clock edge.

For example, the ADSP-2111 has a master clock frequency of 16 MHz. If the SCLKDIV register is loaded with the value 3, an SCLK of 2 MHz is obtained and eight master clock periods will elapse for every one SCLK period. If the timer registers are loaded with the value 803, 100.5 SCLKs will occur between interrupts and subsequently between transmit instructions. This situation will result in nonequidistant sampling as the transmit instruction is occurring on an SCLK edge. If the number of SCLKs between interrupts is a whole integer figure of N, equidistant sampling will be implemented by the DSP.



*ADDITIONAL PINS OMITTED FOR CLARITY.

Figure 18. Interfacing to the ADSP-218x

AD7476A/AD7477A/AD7478A to DSP563xx Interface
The connection diagram in Figure 19 shows how the AD7476A/AD7477A/AD7478A can be connected to the SSI (synchronous serial interface) of the DSP563xx family of DSPs from Motorola. The SSI is operated in synchronous and normal mode (SYN = 1 and MOD = 0 in Control Register B, CRB) with internally generated word frame sync for both Tx and Rx (Bits FSL1 = 0 and FSL0 = 0 in CRB). Set the word length in Control Register A (CRA) to 16 by setting Bits WL2 = 0, WL1 = 1, and WL0 = 0 for the AD7476A. The word length for the AD7478A can be set to 12 bits (WL2 = 0, WL1 = 0, and WL0 = 1). This DSP does not offer the option for a 14-bit word length, so the AD7477A word length will be set up to 16 bits, the same as the AD7476A. For the AD7477A, the conversion process will use 16 SCLK cycles, with the last two clock periods clocking out two trailing zeros to fill the 16-bit word.

To implement the power-down mode on the AD7476A/AD7477A/AD7478A, the word length can be changed to eight bits by setting Bits WL2 = 0, WL1 = 0, and WL0 = 0 in CRA. The FSP bit in the CRB register can be set to 1, meaning the frame goes low and a conversion starts. Likewise, by means of the Bits SCD2, SCKD, and SHFD in the CRB register, it will be established that the Pins SC2 (the frame sync signal) and SCK in the serial port will be configured as outputs and the MSB will be shifted first.

To summarize,
MOD = 0
SYN = 1
WL2, WL1, and WL0 depend on the word length
FSL1 = 1 and FSL0 = 0
FSP = 1, Negative Frame Sync
SCD2 = 1
SCKD = 1
SHFD = 0

It should be noted that for signal processing applications, it is imperative that the frame synchronization signal from the DSP563xx will provide equidistant sampling.

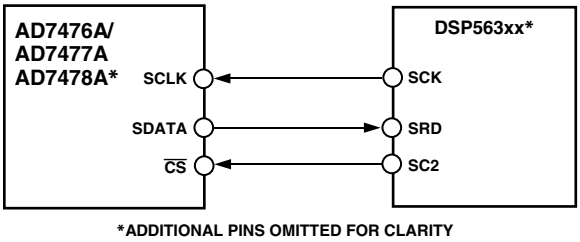


Figure 19. Interfacing to the DSP563xx

APPLICATION HINTS

Grounding and Layout

The printed circuit board that houses the AD7476A/AD7477A/AD7478A should be designed such that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined at only one place. If the AD7476A/AD7477A/AD7478A is in a system where multiple devices require an AGND to DGND connection, the connection should still be made at one point only, a star ground point that should be established as close as possible to the AD7476A/AD7477A/AD7478A.

Avoid running digital lines under the device as these will couple noise onto the die. The analog ground plane should be allowed to run under the AD7476A/AD7477A/AD7478A to avoid noise coupling. The power supply lines to the AD7476A/AD7477A/AD7478A should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital grounds to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is also very important. The supply should be decoupled with, for instance, a 680 nF 0805 to GND. When using the SC70 package in applications where the size of the components is of concern, a 220 nF 0603 capacitor, for example, could be used instead. However, in that case, the decoupling may not be as effective and may result in an approximate SINAD degradation of 0.3 dB. To achieve the best performance from these decoupling components, the user should endeavor to keep the distance between the decoupling capacitor and the V_{DD} and GND pins to a minimum with short track lengths connecting the respective pins. Figures 20 and 21 show the recommended positions of the decoupling capacitor for the MSOP and SC70 packages, respectively.

As can be seen in Figure 20, for the MSOP package, the decoupling capacitor has been placed as close as possible to the IC with short track lengths to V_{DD} and GND pins. The decoupling capacitor could also be placed on the underside of the PCB directly underneath the IC, between the V_{DD} and GND pins attached by vias. This method is not recommended on PCBs above a standard 1.6 mm thickness. The best performance will be seen with the decoupling capacitor on the top of the PCB next to the IC.

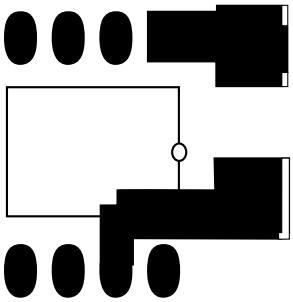


Figure 20. Recommended Supply Decoupling Scheme for the AD7476A/AD7477A/AD7478A MSOP Package

Similarly, for the SC70 package, the decoupling capacitor should be located as close as possible to the V_{DD} and the GND pins. Because of its pinout, i.e., V_{DD} being next to GND, the decoupling capacitor can be placed extremely close to the IC. The decoupling capacitor could be placed on the underside of the PCB directly under the V_{DD} and GND pins, but as before, the best performance will be achieved with the decoupling capacitor on the same side as the IC.

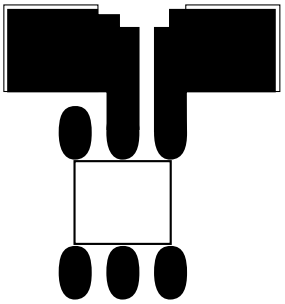


Figure 21. Recommended Supply Decoupling Scheme for the AD7476A/AD7477A/AD7478A SC70 Package

Evaluating the AD7476A/AD7477A Performance

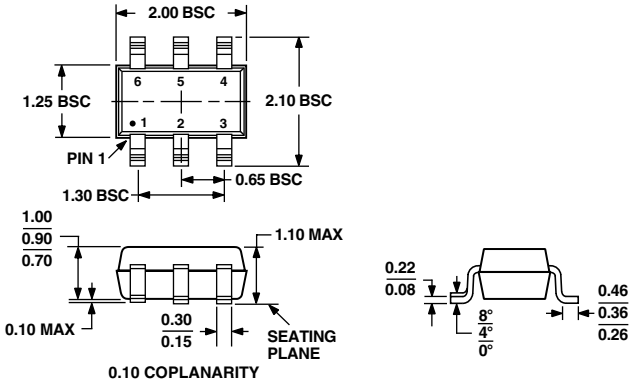
The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from the PC via the EVAL-BOARD CONTROLLER. The EVAL-BOARD CONTROLLER can be used in conjunction with the AD7476ACB/AD7477ACB evaluation board, as well as many other Analog Devices evaluation boards ending in the CB designator, to demonstrate/evaluate the ac and dc performance of the AD7476A/AD7477A.

The software allows the user to perform ac (fast Fourier transform) and dc (histogram of codes) tests on the AD7476A/AD7477A. See the evaluation board application note for more information.

OUTLINE DIMENSIONS

6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)

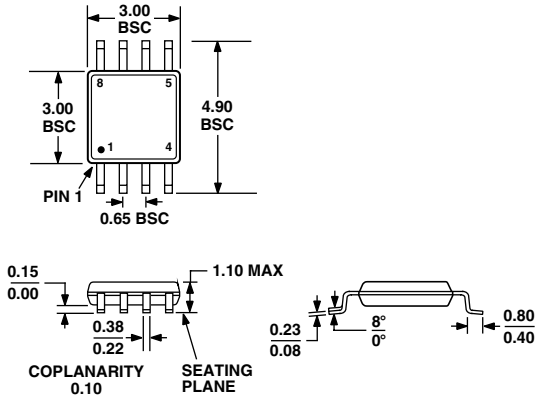
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203AB

8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-187AA

Revision History

Location	Page
3/04—Data Sheet changed from REV. B to REV. C.	
Added U.S. Patent number	1
Changes to AD7476A/AD7477A/AD7478A to ADSP-218x section	20
1/04—Data Sheet changed from REV. A to REV. B.	
Changes to AD7476A SPECIFICATIONS	2
Changes to AD7476A SPECIFICATIONS	2
Changes to AD7477A SPECIFICATIONS	3
Changes to AD7478A SPECIFICATIONS	4
Changes to TIMING SPECIFICATIONS	6
Changes to ABSOLUTE MAXIMUM RATINGS	8
Changes to AD7476A/AD7477A/AD7478A to ADSP-218x section	18
Updated OUTLINE DIMENSIONS	22
2/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to SPECIFICATIONS	2
Changes to TIMING SPECIFICATIONS	6
Changes to ABSOLUTE MAXIMUM RATINGS	7
Change to ORDERING GUIDE	7
Changes to AD7476A/AD7477A/AD7478A to DSP563xx Interface section	18