# ACT-PS512K8 High Speed
# 4 Megabit Plastic Monolithic SRAM

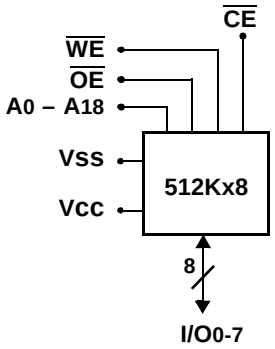
## Plastic Path™ Features

- **Low Power Monolithic CMOS 512K x 8 SRAM**
- **Operating Temperature Range**
  - **Full Military (-55°C to +125°C)**
  - **Industrial (-40°C to +85°C)**
- **Burn-in and Temperature Cycle Available**
- **10, 12, 15, 17, 20 & 25ns Access Times**
- **+5V Power Supply**
- **Industry Standard Pinouts**
  - **Center Power / Ground Pins**
- **TTL Compatible I/O**
- **3.3V Device I/O Interfacing**
- **JEDEC Standard 36 pin Plastic SOJ Package**
  - **36 Lead, .93" x .405" x 0.148 Small Outline J lead (SOJ), Aeroflex code# "L2"**
- **Fully Static Operation**
  - **No Clocks or Refresh Required**

AEROFLEX
CIRCUIT TECHNOLOGY
www.aeroflex.com

AEROFLEX LABS INC. ISO 9001 CERTIFIED

### Block Diagram – SOJ (L2)




**Pin Description**

| | |
|---|---|
| I/O0-7 | Data I/O |
| A0–18 | Address Inputs |
| $\overline{WE}$ | Write Enable |
| $\overline{CE}$ | Chip Enable |
| $\overline{OE}$ | Output Enable |
| Vcc | Power Supply |
| Vss | Ground |
| NC | Not Connected |

## General Description

The ACT-PS512K8 is a Plastic High Speed, 4 Megabit (4,194,304 bits) CMOS Monolithic SRAM organized as 524,288 words by 8 bits. Designed for high-speed, high density, high reliablility, mass memory and fast cache system applications.

The plastic monolithic is input and output TTL compatible. Writing is executed when the write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are low. Reading is accomplished when $\overline{WE}$ is high and $\overline{CE}$ and output enable ($\overline{OE}$) are both low. Access time grades of 10ns 12ns, 15ns, 17ns, 20ns and 25ns are standard.

## Absolute Maximum Ratings

| Symbol | Parameter | MINIMUM | MAXIMUM | Units |
|---|---|---|---|---|
| $T_C$ | Case Operating Temperature | -55 | +125 | °C |
| $T_{STG}$ | Storage Temperature | -65 | +150 | °C |
| $P_D$ | Maximum Package Power Dissipation | | 1.0 | W |
| $V_G$ | Maximum Signal Voltage to Ground | -0.5 | $V_{CC}$ + 0.5 | V |
| $V_{CC}$ | Power Supply Voltage | -0.5 | +7.0 | V |

## Recommended Operating Conditions

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | +4.5 | +5.5 | V |
| $V_{SS}$ | Ground | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | +2.2 | $V_{CC}$ + 0.5 | V |
| $V_{IL}$ | Input Low Voltage | -0.5 | +0.8 | V |
| $T_C$ | Operating Temperature (Military) | -55 | +125 | °C |
| $T_C$ | Operating Temperature (Industrial) | -40 | +85 | °C |

## Truth Table

| Mode | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Data I/O | Supply Current |
|---|---|---|---|---|---|
| Standby | H | X | X | High Z | $I_{SB}$ |
| Output Disable | L | H | H | High Z | $I_{CC}$ |
| Read | L | H | L | Data OUT | $I_{CC}$ |
| Write | L | L | X | Data IN | $I_{CC}$ |

## Capacitance

($V_{IN}$ & $V_{OUT}$ = 0V, f = 1MHz, $T_C$ = 25°C, unless otherwise noted, Guaranteed but not tested)

| Symbol | Parameter | Maximum | Units |
|---|---|---|---|
| $C_{IN}$ | Input Capacitance ($A_{0-18}$, $\overline{WE}$ & $\overline{OE}$) | 6 | pF |
| $C_{OUT}$ | Output Capacitance ($I/O_{0-7}$ & $\overline{CE}$) | 8 | pF |

## DC Characteristics

($V_{CC}$ = 5.0V, $V_{SS}$ = 0V, $T_C$ = -55°C to +125°C or -40°C to +85°C)

| Parameter | Sym | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{CC}$ = Max, $V_{IN}$ = $V_{SS}$ to $V_{CC}$ | -10 | +10 | µA |
| Output Leakage Current | $I_{LO}$ | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$ = $V_{IH}$, $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ | -10 | +10 | µA |
| Operating Supply Current | $I_{CC}$ | $\overline{CE}$ = $V_{IL}$, $\overline{OE}$ = $V_{IH}$,f =5MHz,Vcc=5.5V | | 130 | mA |
| Standby Current | $I_{SB}$ | $\overline{CE}$ = $V_{IH}$, $\overline{OE}$= $V_{IH}$, f =5MHz,Vcc=5.5V | | 20 | mA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 8 mA, Vcc = 4.5V | | 0.4 | V |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -4 mA, Vcc = 4.5V | 2.4 | | V |

Note: DC Test conditions: $V_{IL}$ = 0.3V, $V_{IH}$ = Vcc - 0.3V.

## AC Characteristics

($V_{CC}$ = 5.0V, $V_{SS}$= 0V, $T_C$ = -55°C to +125°C or -40°C to +85°C)

**Read Cycle**

| Parameter | Sym | –010 | | –012 | | –015 | | –017 | | –020 | | –025 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 10 | | 12 | | 15 | | 17 | | 20 | | 25 | | ns |
| Address Access Time | $t_{AA}$ | | 10 | | 12 | | 15 | | 17 | | 20 | | 25 | ns |
| Chip Enable Access Time | $t_{ACE}$ | | 10 | | 12 | | 15 | | 17 | | 20 | | 25 | ns |
| Output Hold from Address Change | $t_{OH}$ | 3 | | 3 | | 3 | | 3 | | 4 | | 5 | | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 5 | | 6 | | 7 | | 8 | | 10 | | 12 | ns |
| Chip Enable to Output in Low Z (1) | $t_{CLZ}$ | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| Output Enable to Output in Low Z (1) | $t_{OLZ}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Chip Deselect to Output in High Z (1) | $t_{CHZ}$ | | 5 | | 6 | | 7 | | 7 | | 8 | | 10 | ns |
| Output Disable to Output in High Z (1) | $t_{OHZ}$ | | 5 | | 6 | | 7 | | 7 | | 8 | | 10 | ns |

Note 1. Guaranteed by design, but not tested

**Write Cycle**

| Parameter | Sym | –010 | | –012 | | –015 | | –017 | | –020 | | –025 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | $t_{WC}$ | 10 | | 12 | | 15 | | 17 | | 20 | | 25 | | ns |
| Chip Enable to End of Write | $t_{CW}$ | 7 | | 8 | | 10 | | 12 | | 13 | | 15 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 7 | | 8 | | 10 | | 12 | | 13 | | 15 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 5 | | 6 | | 8 | | 8 | | 9 | | 10 | | ns |
| Write Pulse Width | $t_{WP}$ | 7 | | 8 | | 10 | | 12 | | 13 | | 15 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Address Hold Time | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write (1) | $t_{OW}$ | 3 | | 3 | | 3 | | 3 | | 4 | | 5 | | ns |
| Write to Output in High Z (1) | $t_{WHZ}$ | | 5 | | 6 | | 7 | | 8 | | 8 | | 10 | ns |
| Data Hold from Write Time | $t_{DH}$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

Note 1. Guaranteed by design, but not tested

## Data Retention Electrical Characteristics (Special Order Only)

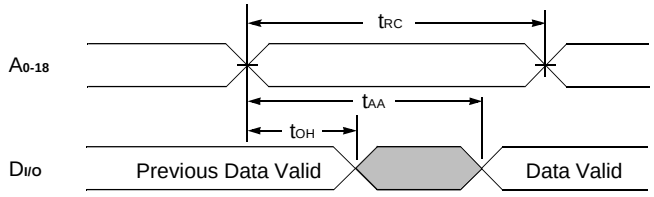
$V_{CC}$ = 5.0V, $V_{SS}$= 0V, $T_C$ = -55°C to +125°C or -40°C to +85°C)

| Parameter | Sym | Test Conditions | All Speeds | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{CC}$ for Data Retention | $V_{DR}$ | $\overline{CE} \geq V_{CC} - 0.2V$ | 2 | | 5.5 | **V** |
| Data Retention Current | $I_{CCDR1}$ | $V_{CC}$ = 3V | | 0.5 | 2.0 | mA |

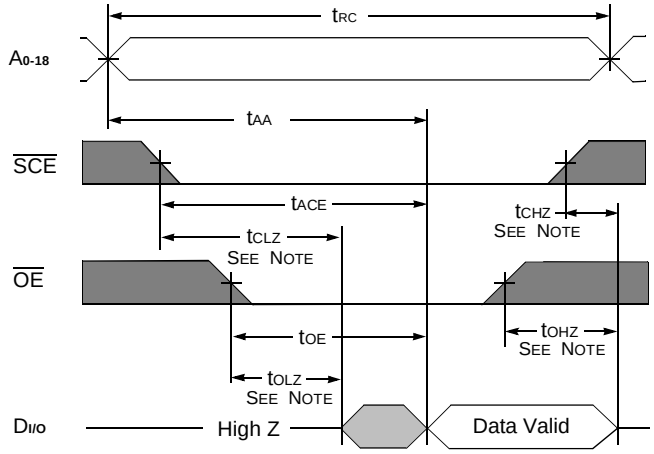
# Timing Diagrams — SRAM

## Read Cycle Timing Diagrams

### Read Cycle 1 ($\overline{SCE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{SWE}$ = $V_{IH}$)



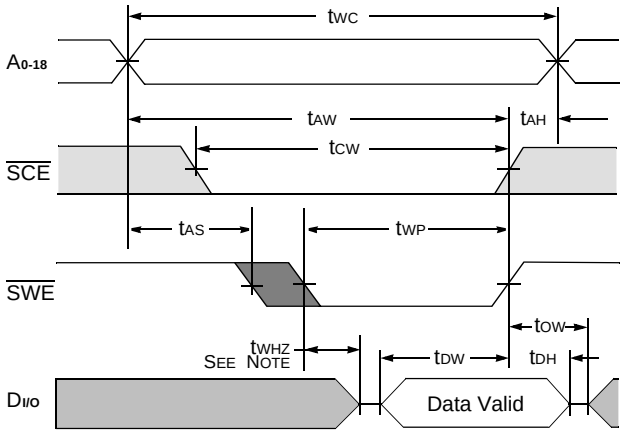

### Read Cycle 2 ($\overline{SWE}$ = $V_{IH}$)



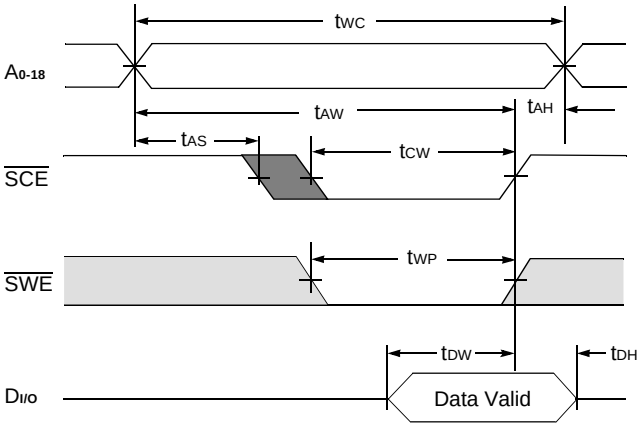


## Write Cycle Timing Diagrams

### Write Cycle ($\overline{SWE}$ Controlled, $\overline{OE}$ = $V_{IH}$)

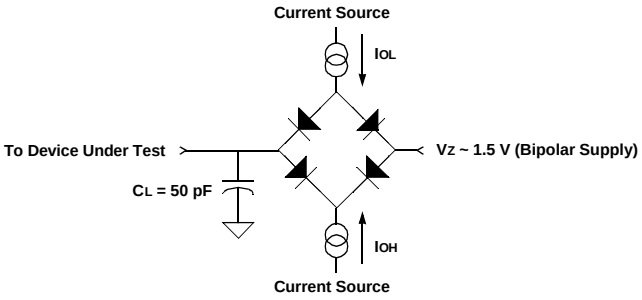



### Write Cycle ($\overline{SCE}$ Controlled, $\overline{OE}$ = $V_{IH}$ )




Note: Guaranteed by design, but not tested.

## AC Test Circuit




### AC Test Conditions

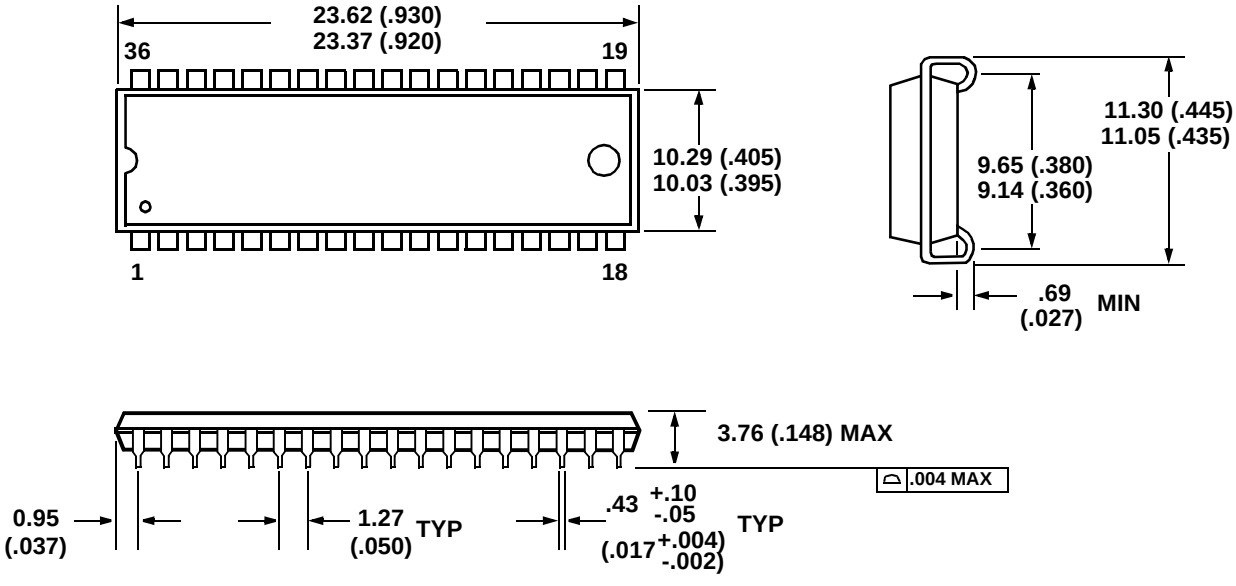
| Parameter | Typical | Units |
|---|---|---|
| Input Pulse Level | 0 – 3.0 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Timing Reference Level | 1.5 | V |

Notes:
1) $V_Z$ is programmable from -2V to +7V. 2) $I_{OL}$ and $I_{OH}$ programmable from 0 to 16 mA. 3) Tester Impedance $Z_O$ = 75Ω. 4) $V_Z$ is typically the midpoint of $V_{OH}$ and $V_{OL}$. 5) $I_{OL}$ and $I_{OH}$ are adjusted to simulate a typical resistance load circuit. 6) ATE Tester includes jig capacitance.

## Pin Numbers & Functions

| 36 Pins — SOJ | | | |
|---|---|---|---|
| Pin # | Function | Pin # | Function |
| 1 | $A_0$ | 19 | NC |
| 2 | $A_1$ | 20 | $A_{10}$ |
| 3 | $A_2$ | 21 | $A_{11}$ |
| 4 | $A_3$ | 22 | $A_{12}$ |
| 5 | $A_4$ | 23 | $A_{13}$ |
| 6 | $\overline{CE}$ | 24 | $A_{14}$ |
| 7 | $I/O_0$ | 25 | $I/O_4$ |
| 8 | $I/O_1$ | 26 | $I/O_5$ |
| 9 | $V_{CC}$ | 27 | $V_{CC}$ |
| 10 | $V_{SS}$ | 28 | $V_{SS}$ |
| 11 | $I/O_2$ | 29 | $I/O_6$ |
| 12 | $I/O_3$ | 30 | $I/O_7$ |
| 13 | $\overline{WE}$ | 31 | $\overline{OE}$ |
| 14 | $A_5$ | 32 | $A_{15}$ |
| 15 | $A_6$ | 33 | $A_{16}$ |
| 16 | $A_7$ | 34 | $A_{17}$ |
| 17 | $A_8$ | 35 | $A_{18}$ |
| 18 | $A_9$ | 36 | NC |

## Package Outline "L2" — SOJ Package, 36 Leads




**All dimensions in inches**

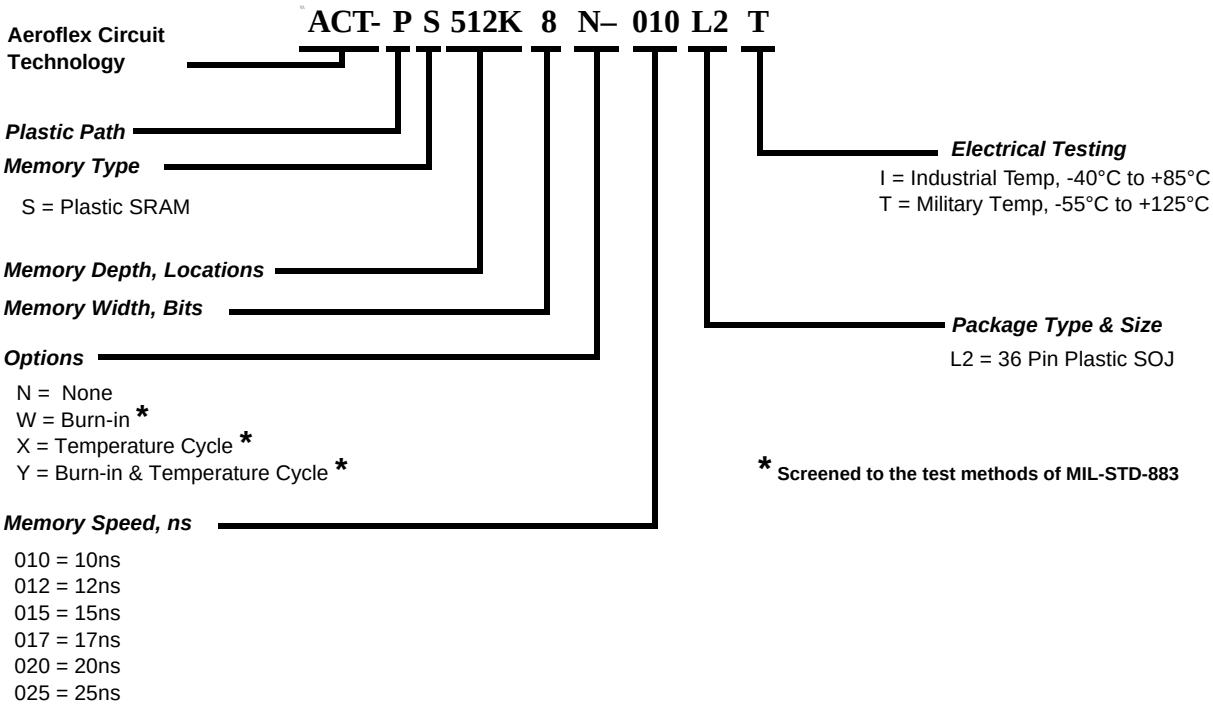
**Dimensions in millmeters mm**
**Dimensions in inches (.xxx)**

AEROFLEX
CIRCUIT TECHNOLOGY

## Ordering Information (Typical)

| Model Number | Options | Speed | Package |
|---|---|---|---|
| ACT-PS512K8N–010L2I | None | 10ns | 36 Lead SOJ |
| ACT-PS512K8W–012L2I | Burn-in | 12ns | 36 Lead SOJ |
| ACT-PS512K8X–015L2T | Temp Cycle | 15ns | 36 Lead SOJ |
| ACT-PS512K8Y–017L2T | Temp Cycle & Burn-in | 17ns | 36 Lead SOJ |
| ACT-PS512K8Y–020L2T | Temp Cycle & Burn-in | 20ns | 36 Lead SOJ |
| ACT-PS512K8Y–025L2T | Temp Cycle & Burn-in | 25ns | 36 Lead SOJ |

## Part Number Breakdown





**Aeroflex Circuit Technology**
**35 South Service Road**
**Plainview New York 11830**

**Telephone: (516) 694-6700**
**FAX: (516) 694-6715**
**Toll Free Inquiries: 1-(800) 843-1553**