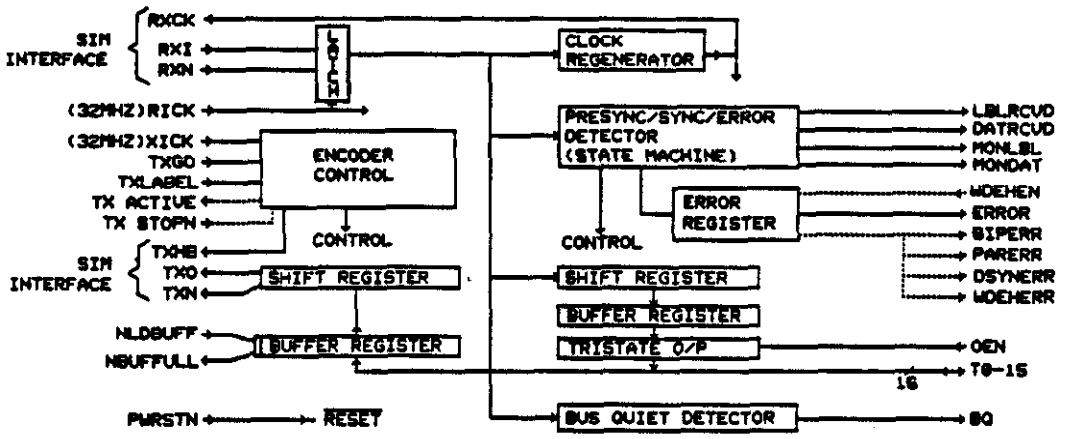
Micro Circuit Engineering

MT62901 ARINC629 ENCODER/DECODER



GENERAL FEATURES

COMPLIANT TO ARINC629.

40/48 PIN DIL OR 44 PIN CHIP CARRIER.

2 MBIT DATA RATE.

LOW POWER CMOS TECHNOLOGY.

ENCODER

STARTS TRANSMISSION ON COMMAND.

TRANSMITS MESSAGES OF ANY LENGTH.

GENERATES PRE-PRESYNC & PRESYNC AT START OF MESSAGE.

GENERATES LABEL/DATA SYNC & PARITY.

GENERATES INTER-STRING GAPS FOR MULTIPLE WORDSTRING MESSAGES.

GENERATES TX ACTIVE OUTPUT DURING TRANSMISSION.

ABORTS TRANSMISSION ON REQUEST.

DECODER

OPERATES WITH EITHER PHASE OF INPUT DATA.

OPERATES WITH OR WITHOUT PRE-PRESYNC & PRESYNC.

DETECTS ERRORS IN SYNC, BIPHASE & PARITY.

OPTIONAL SEPARATE ERROR REGISTER OUTPUTS.

MONITOR OUTPUTS INDICATE WHEN RECEIVING LABEL OR DATA WORD.

BUILT-IN CLOCK REGENERATION CIRCUIT.

BUILT-IN BUS QUIET DETECTION CIRCUIT.

GENERAL DESCRIPTION

The Encoder and Decoder sections of the chip are independent except for sharing a common 16 bit parallel data highway.

The Decoder receives serial data from an ARINC629 SIM and returns the regenerated clock signal. The serial data is decoded and presented on a 16 bit parallel highway with a label or data strobe for each word received. Label words containing errors are rejected. Data words containing errors set an error output. Devices in 48 pin packages have additional separate outputs to flag parity errors, bi-phase errors and data-sync errors. Monitor outputs indicate when a valid label is being received, and when a data word is being received. A Bus Quiet detector detects the end of each word received and sets bus quiet (BQ) active for 2.5 bit times (1.25 micro sec.). After this time, BQ remains set until activity is detected on the bus.

The Encoder generates TXO, TXN and TXHB (TX High impedance on Bus) signals to drive an ARINC629 SIM. Sixteen bit parallel words loaded into a buffer register are converted into ARINC629 label/data format with sync & parity, and transmitted on the serial databus. A pulse on TXGO immediately initiates transmission of a message. Each message begins with pre-presync and presync pulses followed by a label word taken from the buffer register. Transmission continues with data or label words as long as the buffer register is refilled with fresh data. Data words follow with no gap, label words follow after a 4 bit-time gap to indicate the start of a new wordstring. The message transmission ends when no more data is loaded in the buffer register.

SIGNALS

TXO & TXN

Manchester II encoded serial data outputs to the SIM (Serial Interface Module). These signals are both low when the encoder is not transmitting. TXO & TXN are valid from at least 12nS before until 2nS after the falling edge of XICK.

XICK

Arinc terminal transmit clock Xtal oscillator input. 32Mhz for 2MBit data rate. The low and high pulse width must be at least 12.5nS.

TXHB

TX High Impedance on Bus output to control SIM output drivers. TXHB is brought low at the same time as TXO goes high at the start of a wordstring. It remains low until the last transition of TXO or TXN at the end of the wordstring. It will go low again at the start of any subsequent wordstrings in the same message.

NLDBUFF

Active low input asynchronously strobes parallel data into the encoder buffer register and strobes the state of TXLABEL into an internal latch. Data must be valid on T0-15 & TXLABEL from at least 8nS before until 12nS after the rising (trailing) edge of NLDBUFF. Minimum pulse width is 25nS.

NBUFFULL

Active low output asserted (low) on the rising (trailing) edge of NLDBUFF to indicate that the encoder buffer register has been loaded with a word for transmission. The word is transferred to the transmitter shift register during transmission of the sync pattern, and at this point, NBUFFULL is reset (high). If a further word is to be transmitted in the same message, it must be loaded within 8.25uS of NBUFFULL going high. The trailing edge (0->1) of the NLDBUFF strobe must occur at least 250nS after NBUFFULL goes high.

TXLABEL

Input to the encoder, strobed with NLDBUFF (see above).

TXLABEL=1 if the word being loaded is a label.

TXLABEL=0 if the word being loaded is a data word.

TXLABEL is ignored for the first word of a message - the first word is always treated as a label word.

TXGO

Active high input to the encoder. A high level on this input initiates transmission of a message. To guarantee recognition of TXGO in a specific (XICK) clock cycle, it should be asserted from 8nS before until 12nS after the falling clock edge. Transmission of pre-presync will begin asynchronously immediately TXGO is asserted. The end of pre-presync will occur 9 clock cycles ater the falling XICK clock edge on which TXGO is recognised. Note that transmission will begin even if the encoder buffer register is empty. In this case, the buffer must be loaded (with the first label to be transmitted) within 44 clock cycles of asserting TXGO.

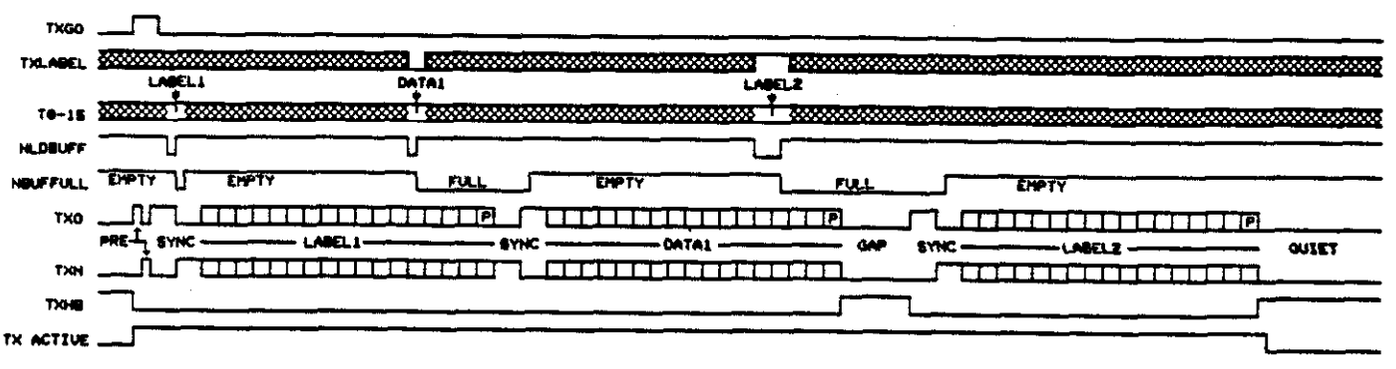
TX ACTIVE (available on 48 pin package only)

This output is brought high immediately TXGO is received and remains high until 250nS after TXHB goes high at the end of the message. Note that TX ACTIVE remains high between wordstrings in the same message.

TXSTOPN (available on 44 & 48 pin packages only)

Active low input with high value internal pullup resistor. When asserted this input, aborts current transmission within 1.5 bit times. Transmission will re-start on the next TXGO.

ENCODER OPERATION



RXI & RXN

Manchester II encoded serial data received from the SIM (Serial Interface Module). Phase of these signals is not important, and may change from one word-string to the next. The only requirement is that each transition or current doublet on the Bus causes one or both signals to change state. The SIM must detect bus quiet and set RXI=RXN on the fourth rising edge of RXCK after the last complementary RXI/RXN transition of a wordstring. RXI & RXN may be asynchronous with RICK. The total combined skew between them plus the time distortion of the databus signal should not exceed 75nS for correct data decoding. To maximise tolerance to signal distortion on the data bus, skew between nominally simultaneous transitions on RXI & RXN should be less than 15nS. If RXI and RXN are synchronous with RICK, then they should be valid from 5nS before until 10nS after the falling edge of RICK to guarantee recognition on that specific clock edge.

RXCK

Regenerated clock output at twice data rate (4MHz) and phase locked to the received data. This signal is principally used to drive the SIM bus quiet timer. The SIM should signal bus quiet (i.e. set RXI=RXN) on the fourth rising edge of RXCK after the last transition on RXI/RXN. The chip will tolerate variations of up to ±62.5nS in the interval between successive changes on RXI/RXN without error or loss of data.

RICK

Arinc terminal receive clock Xtal oscillator input. Set to 32 Mhz for 2 MBit data rate. The low and high pulse width must be at least 12.5nS.

PWRSTN

Active low system/power-up reset input.

MONLBL

Monitor output. This signal is asserted (high) as long as the decoder is receiving a valid label word. Sync, biphase encoding or parity errors detected in the label cause this output to be reset immediately. MONLBL is set high when the centre transition of the label sync (H-L) field is detected. If no errors are detected, MONLBL is reset at the end of the LBLRCVD pulse.

MONDAT

Monitor output. This signal is asserted (high) as long as the decoder is receiving data words. Biphase and parity errors do not affect this output. MONDAT is set high when the centre transition of the dataword sync (L-H) field is detected. It remains high until the end of the next DATRCVD pulse. If an invalid data sync pattern is received, MONDAT goes low for the remainder of the wordstring.

LBLRCVD

Label received output. A 250 nS (nominal) wide active high pulse is generated at the end of each error-free label word received.

DATRCVD

Data received output. A 250 nS (nominal) wide active high pulse is generated at the end of each data word received. Note that the error output must be examined to see if the data word contained a biphase encoding or parity error.

ERROR

Active high error output indicating the decoder has detected an error in a data word. For parity and biphase errors, the error output is set at the same time as DATRCVD is asserted. A datasync error following a valid label or data word will set the error output up to 4 cycles of the RXCK clock (nominally 1uS) after LBLRCVD or DATRCVD is asserted. ERROR remains set until the next DATRCVD or LBLRCVD pulse.

)EN
Output enable. Active low input enables the tristate output buffers on the parallel data bus. Output data is valid 35nS after OEN is asserted (50pF load). The bus is high-Z 10nS after OEN is taken high.

TO -T15
Parallel data bus. T15 is the most significant bit. When the OEN input is held low, decoder output data is valid 30nS after the leading edge of each LBLRCVD and DATRCVD pulse and remains valid until the next LBLRCVD or DATRCVD pulse.

BQ
Bus Quiet - active high output. This output is asserted six cycles of the RICK clock after the end of each label or data word received (see timing diagram) and remains active for at least 2.5 bit times (1.25 micro sec. with 32 MHz RICK). After this time BQ is reset immediately activity is detected on the Bus (i.e. RXI not equal RXN).

WDEHEN (available on 48 pin package only)
This input has an internal high value pullup resistor. Tie this pin high for standard ARINC 629 operation. Pulling WDEHEN low enables a proprietry error detection function which is not compatible with the current issue of ARINC 629.

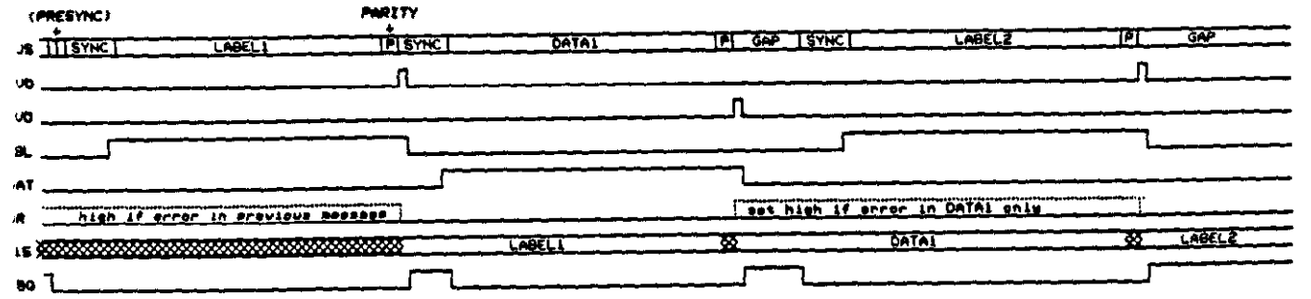
BIPERR (available on 44 & 48 pin packages only)
This output is set high as soon as a bi-phase encoding error is detected whilst receiving a dataword (NOT label). It will remain set for at least 6 cycles of RXCK (nominally 1.5uS) after DATRCVD is asserted at the end of the dataword containing the error.

PARERR (available on 44 & 48 pin packages only)
This output is set high at the same time as DATRCVD is asserted when the dataword contains a parity error. It will remain set for at least 6 cycles of RXCK (nominally 1.5uS).

DSYNERR (available on 44 & 48 pin packages only)
This output is set high if a word is immediately followed by an invalid datasync pattern The device continues to monitor the bus for 2 bit times after the end of the word and reports any illegal states. Note: under some conditions this may indicate the preceeding word contained an error which could not be detected by parity or bi-phase checks. DSYNERR is asserted up to 4 cycles of RXCK (nominally 1uS) after LBLRCVD or DATRCVD is asserted and remains set until at least 6 cycles of RXCK (1.5µS) after the start of DATRCVD or LBLRCVD. Note: BIPERR and DSYNERR together detect all cases of too few or too many bits in a word.

WDEHERR (available on 48 pin package only)
Error output associated with the WDEHEN function. This output is not used for standard ARINC 629 operation.

ER OPERATION



ABSOLUTE MAXIMUM RATINGS (all Voltages Relative to VSS=0V)

	Min.	Max.	Units
Supply Voltage (VDD)	-0.3	7.0	V.
I/P Voltage	VSS-0.3	VDD+0.3	V.
O/P Current Low	---	15	mA.
O/P Current High	---	15	mA.
Storage Temperature	-65	+150	° C.

RECOMMENDED OPERATING CONDITIONS

	Min.	Typ.	Max.	Units
Supply Voltage (VDD)	4.5	5.0	5.5	V.
Case Temp. (Commercial)	0	25	70	° C.
Case Temp. (MIL & BS)	-55	25	+125	° C.

DC CHARACTERISTICS

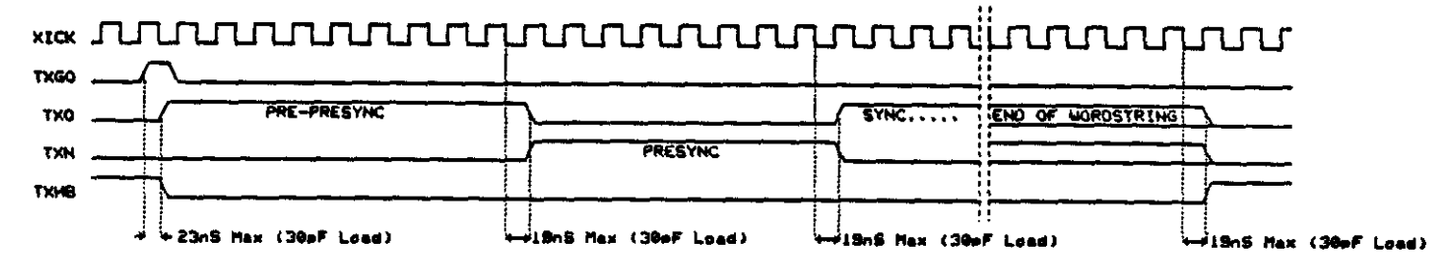
	Min.	Typ.	Max.	Units
VDD supply current		10	20	mA.
Low level I/P voltage	---	0.4	0.8	V.
High level I/P voltage	2.0	2.4	---	V.
I/P current (no pullup)	-5	---	+5	µA.
I/P current (pullup, Vin=0v)	-35	-112	-370	µA.
Low level O/P voltage	---	---	0.4	V.
High level O/P voltage	2.4	---	---	V.
O/P current (Vout=2.4v)	---	-4.0	-2.9	mA.
O/P current (Vout=0.4v)	3.2	4.0	---	mA.
I/P capacitance		5		pF.
I/O capacitance		10		pF.

AC CHARACTERISTICS

Timing parameters are specified for the following conditions unless otherwise stated:

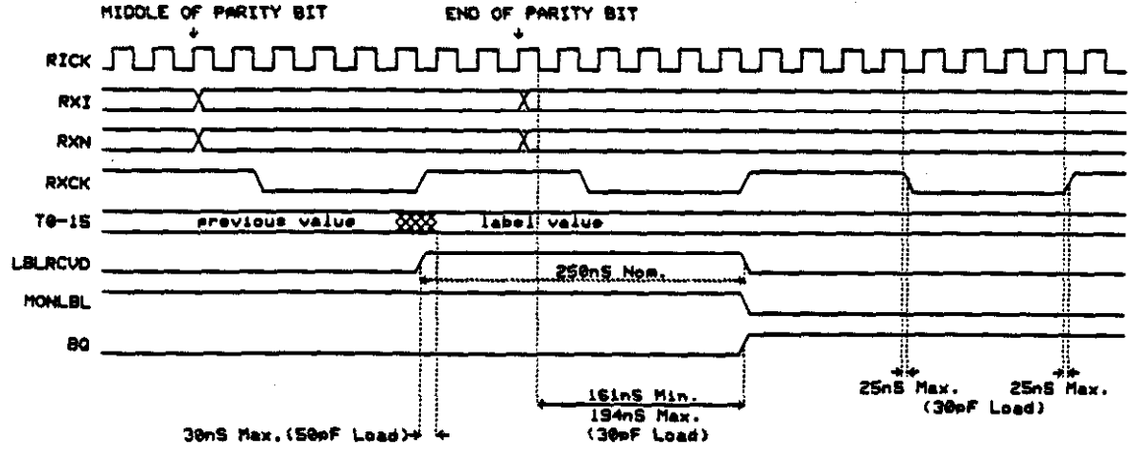
Recommended operating temperature range.
Recommended operating voltage range.
Output load capacitance 50pF.
Rising edge measurements made at Voh = 2.0v.
Falling edge measurements made at Vol = 0.8v.

ENCODER TIMING



N.B. The PRE-PRESYNC pulse starts asynchronously on TXGO and ends 9 clock cycles after the -ve XICK edge on which TXGO is detected. To Guarantee TXGO recognition in a specific clock cycle it should be stable from 0nS before until 12nS after the XICK -ve edge.

DECODER TIMING



N.B. RXI & RXN Are sampled on the -ve RICK edge.
Timing of DATRCVD & MONDAT is identical to LBLRCVD & MONLBL.
BQ will be set Low within 22nS of any activity (i.e. RXI ≠ RXN) on RXI/RXN (30pF Load).

Y ASSIGNMENTS (40 Pin DIL Package)

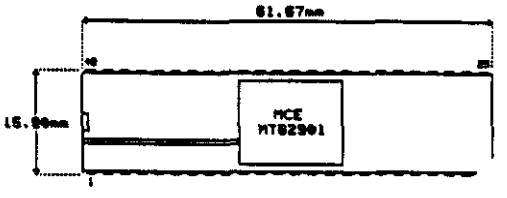
RXI	21	T3
RICK	22	T2
MONLBL	23	T1
MONDAT	24	T0
VDD (+5v)	25	VDD (+5v)
VSS (0v)	26	VSS (0v)
OEN	27	DATRCVD
ERROR	28	LBLRCVD
T15	29	BQ
T14	30	PWRSTN
T13	31	TXO
T12	32	TXN
T11	33	XICK
T10	34	TXHB
T9	35	NBUFFULL
T8	36	NLDBUFF
T7	37	TXGO
T6	38	TXLABEL
T5	39	RXCK
T4	40	RXN

PIN ASSIGNMENTS (48 Pin DIL Package)

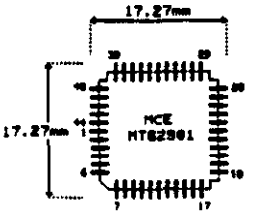
1	RICK	25	T3
2	MONLBL	26	T2
3	PARERR	27	T1
4	BIPERR	28	T0
5	MONDAT	29	TX ACTIVE
6	VDD (+5v)	30	VDD (+5v)
7	TXSTOPN	31	VSS (0v)
8	WDEHEN	32	DATRCVD
9	OEN	33	LBLRCVD
10	WDEHERR	34	BQ
11	ERROR	35	PWRSTN
12	T15	36	DSYNERR
13	T14	37	TXO
14	T13	38	TXN
15	T12	39	XICK
16	T11	40	TXHB
17	T10	41	NBUFFULL
18	T9	42	VSS (0v)
19	VSS (0v)	43	NLDBUFF
20	T8	44	TXGO
21	T7	45	TXLABEL
22	T6	46	RXCK
23	T5	47	RXN
24	T4	48	RXI

N ASSIGNMENTS (44 Pin Quad J-Lead Package)

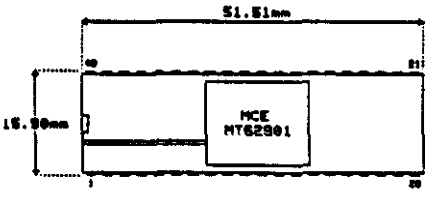
RXI	23	T4
RICK	24	T3
MONLBL	25	T2
PARERR	26	T1
BIPERR	27	T0
MONDAT	28	VDD (+5v)
VDD (+5v)	29	DATRCVD
TXSTOPN	30	LBLRCVD
OEN	31	BQ
ERROR	32	PWRSTN
T15	33	DSYNERR
T14	34	TXO
T13	35	TXN
T12	36	XICK
T11	37	TXHB
T10	38	NBUFFULL
T9	39	VSS (0v)
VSS (0v)	40	NLDBUFF
T8	41	TXGO
T7	42	TXLABEL
T6	43	RXCK
T5	44	RXN



48 PIN DIL CERAMIC PACKAGE
TOP VIEW



44 PIN J-LEAD PACKAGE
TOP VIEW



40 PIN DIL CERAMIC PACKAGE
TOP VIEW

RDERING INFORMATION

he table below gives the MCE part number for each package/screening flow option.

Package	Commercial	BS9400	MIL883B
48 pin Ceramic DIL	MT62901D9	MT62901D2	MT62901D4
44 pin Cerquad J lead	MT62901JZ9	MT62901JZ2	MT62901JZ4
40 pin Ceramic DIL	MT62901D9A	MT62901D2A	MT62901D4A

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