Data Sheet
January 2000

1345-Type Receiver with Clock Recovery and Data Retiming

Operating at 1.3 µm or 1.55 µm wavelengths and at 155 Mbits/s or 622 Mbits/s, the versatile 1345-Type Receiver is manufactured in a 20-pin, plastic DIP with a multimode fiber pigtail.

Features

- Backward compatible with 1330 family
- Space-saving, self-contained, 20-pin plastic DIP
- Silicon based ICs
- Single 5 V power supply operation including photocurrent monitor capability
- Exceeds all SONET (GR-253-CORE) and ITU-T G.958 jitter requirements
- Clocked decision circuit
- Regenerated differential clock signal
- Wide dynamic range
- Qualified to meet the intent of *Telcordia Technologies*™ reliability practices
- Operates at data rates of 155 Mbits/s or 622 Mbits/s
- Positive ECL (PECL) data outputs
- CMOS (TTL) link-status flag output
- Operation at 1.3 µm or 1.55 µm wavelengths
- Operating temperature range of –40 °C to +85 °C

Applications

- Telecommunications:
  - — Inter- and intraoffice SONET/ITU-T SDH
  - — Subscriber loop
  - — Metropolitan area networks
- High-speed data communications

Description

The 1345-Type fiber-optic receiver is designed for use in transmission systems or medium- to high-speed data communication applications. Used in intermediate- and long-reach applications, the receiver operates at the SONET OC-3 or OC-12 data rate as well as the ITU-T synchronous digital hierarchy (SDH) rate of STM-1 or STM-4, depending on the receiver model chosen. The receiver meets all present *Telcordia Technologies* GR-253-CORE requirements, the current ANSI T1X1.5 intraoffice specifications, and the ITU-T G.957 and G.958 recommendations. Compact packaging, a high level of integration, and a wide dynamic range make these receivers ideal for data communications.

Manufactured in a 20-pin DIP, the receiver consists of a planar InGaAs PIN photodetector, a silicon preamplifier, a silicon bipolar limiting amplifier that converts the small signal to ECL levels, a timing recovery unit to recover the clock, and a silicon bipolar decision circuit.

Description (continued)

The receiver converts optical signals in the range of 1.1 μm to 1.6 μm into retimed clock and data signals. The clock and data outputs are raised-ECL (PECL) logic levels. A CMOS-level flag output indicates when there is a loss of optical signal.

The receiver requires a 5 V power supply for the amplifier, logic, and PLL CRC circuits. The operating case temperature range is –40 °C to +85 °C.

Pin 10

Pin 10 on the 1345-Type receiver is not an internally connected (NIC) pin. This definition allows the 1345 to be used in most customer 20-pin receiver module applications. Customer's printed-wiring boards that are designed with ground, +5 V, –5 V, or no connection to this pin are all acceptable options. For those applications that require monitoring the photocurrent of the PIN photodetector for power monitoring purposes, there are versions of the 1345 that require +5 V or –5 V applied to Pin 10. Check Tables 3 and 4 for ordering information.

Flag Output

When the optical input falls below the link status flag switching threshold, the link status flag is deactivated and its output logic level changes from a CMOS logic HIGH to a CMOS logic LOW.

Squelched Data and Clock Outputs

In some versions of the 1345 receiver (see Table 4), when the link status flag is deactivated, the data and clock outputs are squelched (stop outputting a signal). When this occurs, the DATA, $\overline{\text{DATA}}$, CLOCK, and $\overline{\text{CLOCK}}$ outputs switch to a constant dc output voltage level of 1.3 V.

Nonsquelched Data and Clock Outputs

Agere Systems also manufactures nonsquelching versions of the 1345 receiver for those applications that require the data and clock outputs to continue to function after the link status flag is deactivated. In those versions of the receiver, when the link status flag is deactivated, a signal will continue to appear at the DATA, $\overline{\text{DATA}}$, CLOCK, and $\overline{\text{CLOCK}}$ outputs. See Table 4 for nonsquelching codes.

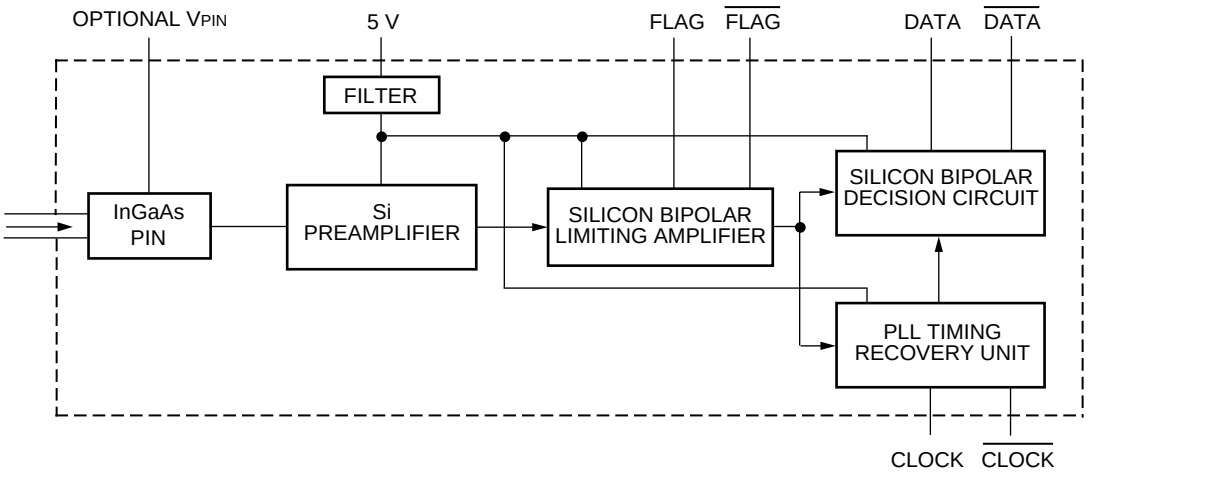


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	0	5.5	V
Operating Case Temperature Range	T_C	–40	85	°C
Storage Case Temperature Range	T_{stg}	–40	85	°C
Lead Soldering Temperature/Time	—	—	250/10	°C/s
Operating Wavelength Range	λ	1.1	1.6	µm
Minimum Fiber Bend Radius	—	1.0 (25.4)	—	in. (mm)

Pin Information

Pin	Name	Pin	Name
1	Ground	20	No User Connection*
2	Ground	19	No User Connection*
3	Ground	18	No User Connection*
4	CLOCK	17	No User Connection*
5	$\overline{\text{CLOCK}}$	16	Ground
6	Ground	15	Ground
7	DATA	14	$\overline{\text{FLAG}}$ †
8	Ground	13	Ground
9	$\overline{\text{DATA}}$	12	FLAG†
10	No Internal Connection or Optional V_{PIN}	11	V_{CC}

* Pins designated as no user connection are not connected internally. However, to allow for future functional upgrades, it is recommended that the user not make any connections to these pins.

† The link status flag is a logic flag that indicates the presence or absence of a minimum acceptable level of optical input. A logic high on the FLAG output indicates the presence of a valid optical signal.

Mounting and Connections

The pigtail consists of a 39 in. ± 4 in. (1 m ± 10 cm), 62.5 µm core/125 µm cladding multimode fiber. The standard fiber has a 0.036 in. (914 µm) diameter tight-buffered outer-jacket. The minimum fiber bending radius during operation is 1.0 in. (25.4 mm).

Electrostatic Discharge

CAUTION: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow guidelines such as *EIA*® Standard *EIA*-625.

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Agere Systems Inc. employs a human-body model (HBM) for ESD susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes. The HBM ESD threshold established for the 1345 receiver is ±1000 V.

Receiver Processing

The 1345-Type receiver devices can withstand normal wave-soldering processes. The complete receiver module is not hermetically sealed; therefore, it should not be immersed in or sprayed with any cleaning solution or solvents. The process cap and fiber pigtail jacket can deform at temperatures greater than 85 °C. The receiver pins can be wave-soldered at maximum temperature of 250 °C for 10 seconds.

Application Information

The 1345 receiver is a highly sensitive fiber-optic receiver. Although the data outputs are digital logic levels (PECL), the device should be thought of as an analog component. When laying out the printed-wiring board (PWB), the 1345 receiver should be given the same type of consideration one would give to a sensitive analog component.

At a minimum, a double-sided printed-wiring board with a large component-side ground plane beneath the receiver must be used. In applications that include many other high-speed devices, a multilayer PWB is highly recommended. This permits the placement of power and ground connections on separate layers, which helps minimize the coupling of unwanted signal noise into the power supplies of the receiver.

Layout Considerations

A fiber-optic receiver employs a very high-gain, wide-bandwidth transimpedance amplifier. The amplifier detects and amplifies signals that are only tens of nA in amplitude. Any unwanted signal currents that couple into the receiver circuitry cause a decrease in the receiver's sensitivity and can also degrade the performance of the receiver's loss of signal (FLAG) circuit. To minimize the coupling of unwanted noise into the receiver, route high-level, high-speed signals such as transmitter inputs and clock lines as far away as possible from the receiver pins. If this is not possible, then the PWB layout engineer should consider interleaving the receiver signal and flag traces with ground traces in order to provide the required isolation.

Noise that couples into the receiver through the power supply pins can also degrade device performance. The application schematics, Figures 2—3, show recommended power supply filtering that helps minimize noise coupling into the receiver. The bypass capacitors should be high-quality ceramic devices rated for RF applications. They should be surface-mount components placed as close as possible to the receiver power supply pins. The ferrite bead should have as high an impedance as possible in the frequency range that is most likely to cause problems. This will vary for each application and is dependent on the signaling frequencies present on the application circuit card. Surface-mount, high-impedance beads are available from several manufacturers.

Data and Flag Outputs

The data and clock outputs of the 1345 receiver are driven by open-emitter NPN transistors which have an output impedance of approximately 7 Ω. Each output can provide approximately 50 mA maximum output current. Due to the high switching speeds of ECL outputs, transmission line design must be used to interconnect components. To ensure optimum signal fidelity, both data outputs (DATA and $\overline{\text{DATA}}$) and clock outputs (CLOCK and $\overline{\text{CLOCK}}$) should be terminated identically. The signal lines connecting the data and clock outputs to the next device should be equal in length and should have matched impedances.

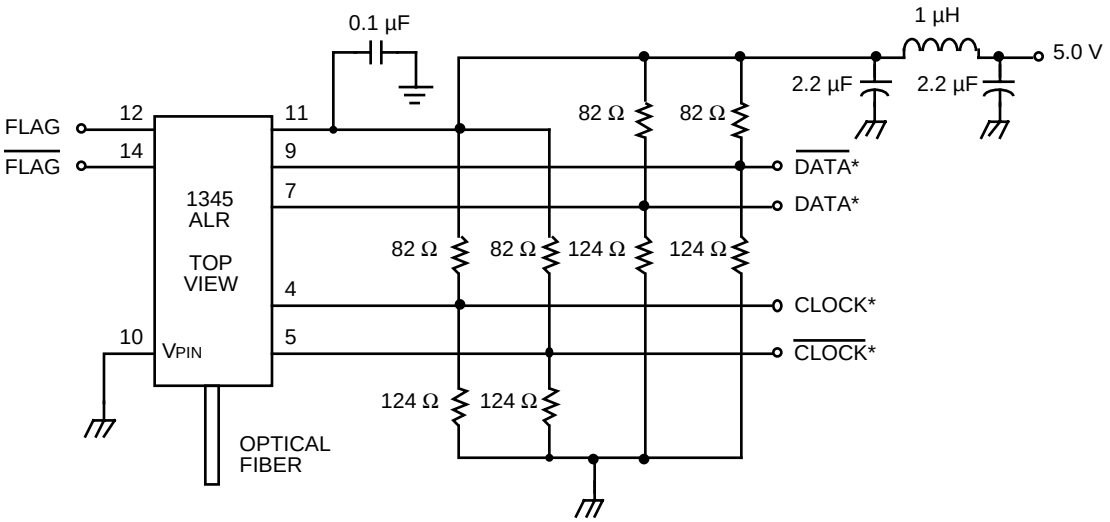
Controlled impedance stripline or microstrip construction must be used in order not to degrade the quality of the signal into the next component and to minimize reflections back into the receiver. Excessive ringing due to reflections caused by improperly terminated signal lines makes it difficult for the component receiving these signals to decipher the proper logic levels and may cause transitions to occur where none were intended. Also, by minimizing high frequency ringing due to reflections caused by improperly designed and terminated signal lines, possible EMI problems can be avoided. The applications sections in the Signetics™ *ECL 10K/100K Data Manual* or the National Semiconductor® *ECL Logic Databook and Design Guide* provide excellent design information on ECL interfacing.

The FLAG and $\overline{\text{FLAG}}$ outputs of the OC-3/STM-1 155 Mbits/s receiver and the OC-12/STM-4 622 Mbits/s receiver are 5 V TTL logic-level compatible. The FLAG output is provided directly by the comparator IC. However, the FLAG output is derived from the $\overline{\text{FLAG}}$ output through an inverter. Excessive loading of the $\overline{\text{FLAG}}$ output can cause the FLAG output to malfunction.

Recommended User Interface

The 1345 receiver is designed to be operated from a 5 V power supply and provides raised or pseudo-ECL (PECL) data outputs. Figures 2 and 3 show two possible application circuits for the 1345 receiver. Figure 2 represents an application for a PECL compatible interface while Figure 3 shows a possible application for an ac-coupled, ECL-compatible interface. In both instances, the DATA outputs are terminated with a Thévenin equivalent circuit, which provides the equivalent of a 50 Ω load terminated to (V_{CC} – 2 V). A single 50 Ω resistor terminated to (V_{CC} – 2 V) could also be used, but this requires a second power supply. Other methods of terminating ECL-type outputs are discussed in the references previously mentioned.

Recommended User Interface (continued)



* DATA, $\overline{\text{DATA}}$, CLOCK, and $\overline{\text{CLOCK}}$ are 50 Ω transmission lines that can be ac- or dc-coupled.

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Figure 2. PECL-Compatible (5 V) Interface

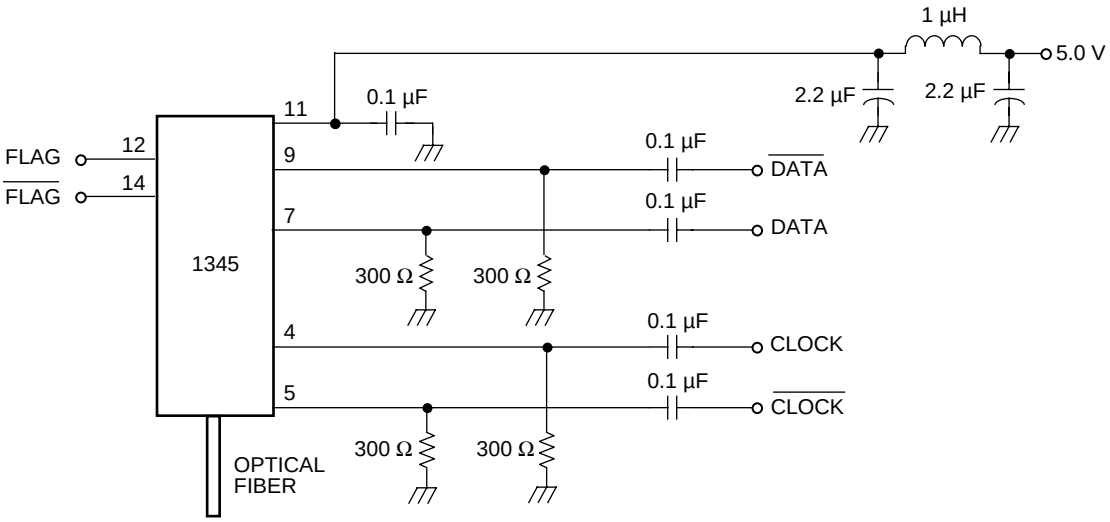

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Figure 3. ac-Coupled ECL-Compatible Interface

Installation Considerations

Although the receiver has been designed with ruggedness in mind, care should be used during handling. The optical connector should be kept free from dust, and the process cap should be kept in place as a dust cover when the device is not connected to a cable. If contamination is present on the optical connector, the use of canned air with an extension tube should remove any debris. Other cleaning procedures are identified in the *Cleaning Fiber-Optic Assemblies* Technical Note (TN95-010LWP).

Characteristics

Minimum and maximum values specified over operating case temperature range and end-of-life (EOL). Typical values are measured at beginning-of-life (BOL) room temperature unless otherwise noted.

Table 1. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
dc Power Supply Voltages	V_{CC}	4.75	5.0	5.25	V
PIN Photodetector Supply Voltage (Pin 10)[1]	V_{PIN} V_{PIN}	4.75 –5.25	5.0 –5.0	5.25 –4.75	V V
dc Power Supply Currents:[2] OC-3/STM-1 Version OC-12/STM-4 Version	 I_{CC} I_{CC}	 — —	 110 150	 150 200	 mA mA
Output Data/Clock Voltage:[3, 4] Low High	 V_{OL} V_{OH}	 V_{CC} – 1.95 V_{CC} – 1.03	 — 	 V_{CC} – 1.63 V_{CC} – 0.88	 V V
Output Data/Clock Rise and Fall Time: OC-3/STM-1 Version OC-12/STM-4 Version	 t_R/t_F t_R/t_F	 1100 320	 1300 360	 1700 500	 ps ps
Output Flag Voltage: Low High	 VF_L VF_H	 0 V_{CC} – 0.5	 — —	 0.6 V_{CC}	 V V
Clock/Data Alignment:[5] OC-3/STM-1 Version OC-12/STM-4 Version	 T_{CDA} T_{CDA}	 –800 –300	 — —	 800 300	 ps ps
Clock Duty Cycle	dc	45	—	55	%
Output Clock Random Jitter:[6] OC-3/STM-1 Version OC-12/STM-4 Version	 J_C J_C	 — —	 0.003 0.005	 0.008 0.01	 UI UI
Output Clock Jitter Peaking	J_P	0.04	0.05	0.1	dB
Jitter Tolerance	*Telcordia Technologies* GR-253-CORE and ITU-T G.958 Compliant				
Jitter Transfer	*Telcordia Technologies* GR-253-CORE and ITU-T G.958 Compliant				

1. Customers have the option for either a +5 V or –5 V supply.
2. Includes approximately 50 mA of DATA and CLOCK output termination current.
3. Measured with 50 Ω load terminated to (V_{CC} – 2.00) V.
4. DATA and CLOCK outputs are 10K ECL compatible.
5. Measured as shown in Figure 4.
6. Measured with an input data pseudorandom word $2^{23} – 1$.

Characteristics (continued)

Table 2. Optical Characteristics

Parameter	Symbol	Data Rates Mbits/s	Min	Typ	Max*	Unit
Measured Average Sensitivity:*, †						
OC-3	P_{RL}	OC-3/STM-1	—	38	–36	dBm
OC-12	P_{RL}	OC-12/STM-4	—	–32.5	–30	dBm
Maximum Input Power‡	P_{MAX}	OC-3/STM-1	0	2	—	dBm
		OC-12/STM-4	–6	–4	—	dBm
Link Status Flag Threshold:‡						
Decreasing Light Input	LST_D	OC-3/STM-1	–50	–41	–37.5	dBm
		OC-12/STM-4	–50	–38.8	–32.5	dBm
Decreasing Light Input	LST_I	OC-3/STM-1	–50	–38	–37.0	dBm
		OC-12/STM-4	–50	–35	–32.0	dBm
Flag Hysteresis	HYS	155/622	0.5	3	6	dB
Flag Response Time	t_{FLAG}	155/622	3	—	100	µs
Detector Responsivity	R	155/622	0.7	0.8	1.2	A/W

* For a 1 x 10^{-10} BER. Measured with a $2^{23} – 1$ pseudorandom word optical input having a 50% average duty cycle.

† Whenever the flag output is deasserted (logic low), the DATA and CLOCK outputs are silenced. See the Flag Output section on page 2 for the DATA and CLOCK output signal levels.

‡ Power supply noise in excess of 50 mVp-p may degrade the performance of the receiver. See User Interface section for recommended power supply filtering.

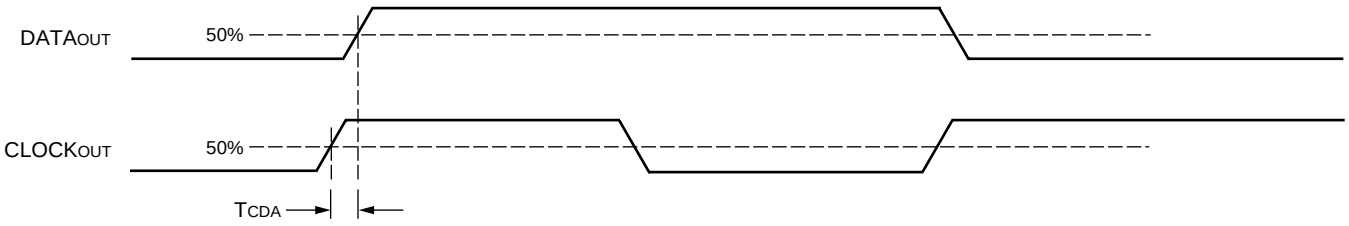

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Figure 4. Clock/Data Alignment

PWB Layout Guidelines

- Follow high-speed ECL design rules.
- All high-speed output lines must be controlled-impedance lines, and the termination impedance must match the line impedance. Controlled-impedance interruptions should be avoided (i.e., 90° bends, etc.) and paired lines (i.e., DATA and $\overline{\text{DATA}}$) should be of equal length.
- Each output line should be terminated at the end of the line and must have a bypass capacitor on the voltage side of the resistor for each termination.
- Data and clock output lines should be as short and as straight as possible and isolated from noise sources (and each other) to prevent noise from feeding back into the receiver.
- Noise that couples into the receiver through the power supply pins can degrade device performance. See Figure 2 for an example of power supply filtering for the receiver 5 V power supply pins.
- Use a multilayer board so that the ground plane surrounds the areas occupied by the receiver and directly underneath it. Directly attach all pins listed as ground pins to the ground plane with no additional lead length.

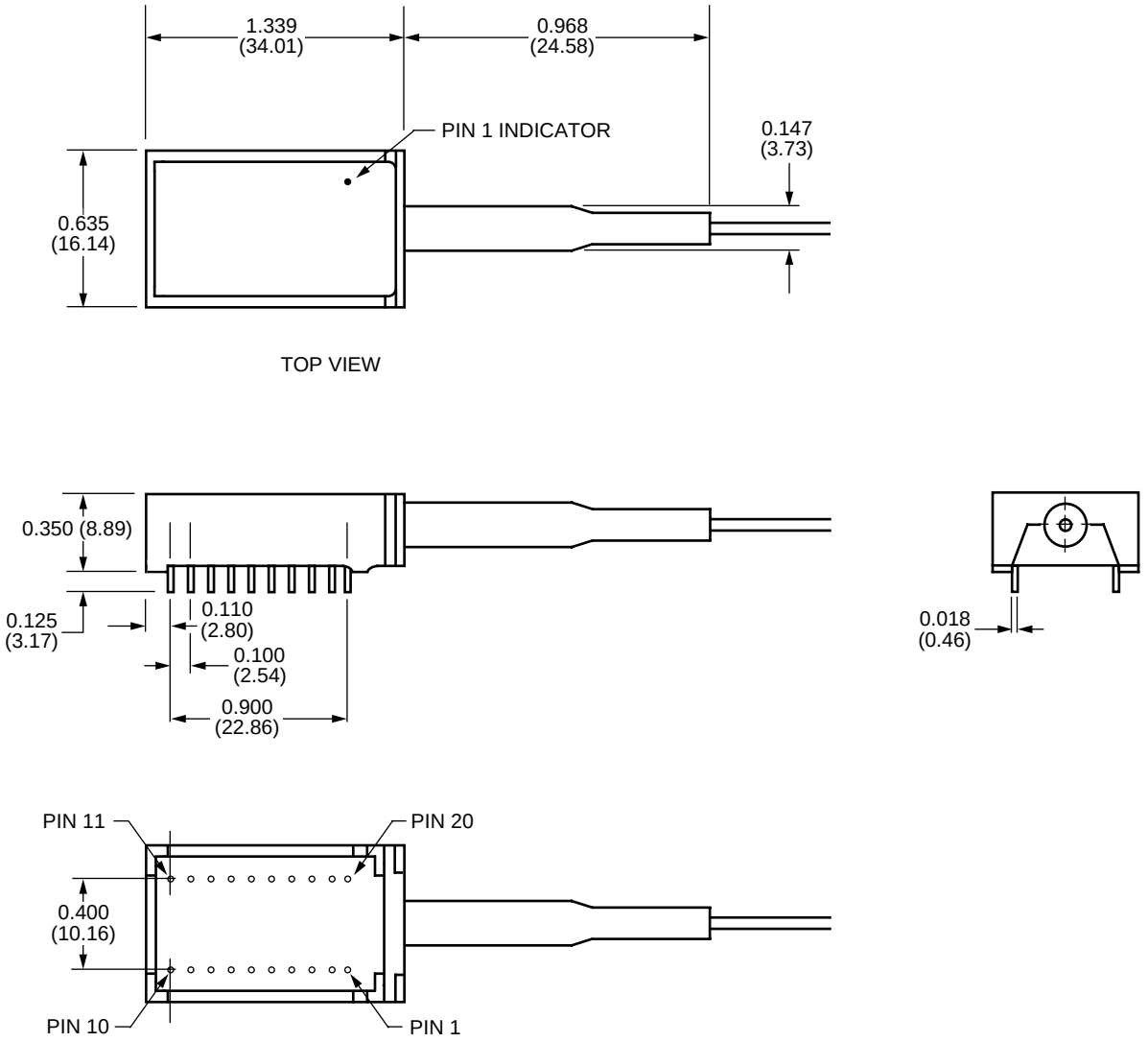
All unused outputs must be terminated as shown. All resistors are 1/8 W, thin-film, ceramic chips. All capacitors are 25 Vdc, ceramic X7R or equivalent.

Qualification and Reliability

To help ensure high product reliability and customer satisfaction, Agere Systems is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing process. Optoelectronics modules are qualified to Agere Systems internal standards using MIL-STD-883 test methods and procedures and using sampling techniques consistent with *Telcordia Technologies* requirements. The 1345 series of receivers have undergone an extensive and rigorous set of qualification tests. This qualification program fully meets the intent of *Telcordia Technologies* reliability practices TR-NWT-000468 and TA-NWT-000983. In addition, the design, development, and manufacturing facility of the Optoelectronics unit at Agere Systems is certified to be in full compliance with the latest *ISO*®-9001 Quality System Standards.

Outline Drawings

Dimensions are in inches and (millimeters). Unless noted otherwise, tolerances are ±0.005 in. (±0.127 mm).



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Ordering Information

Table 3. OC-3/STM-1 Receiver Versions

Device Code	Pin 10 Requirements	Connector	Comcode
1345FMPC	No Internal Connections	FC-PC	108339979
1345CMPC		SC	108354473
1345TMPC		*ST* ®	108572421
1345FMPD*		FC-PC	108354515
1345CMPD*		SC	108354481
1345TMPD*		*ST*	108572439
1345FAPC	Requires +5 V or –5 V	FC-PC	108468687
1345CAPC		SC	108359175
1345TAPC		*ST*	108572249
1345FAPD*		FC-PC	108572322
1345CAPD*		SC	108572280
1345TAPD*		*ST*	108572389

* These versions have nonsquelching data and clock outputs. See Nonsquelched Data and Clock Outputs section on page 2.

Table 4. OC-12/STM-4 Receiver Versions

Device Code	Pin 10 Requirements	Connector	Comcode
1345FNPC	No Internal Connections	FC-PC	108155722
1345CNPC		SC	107354499
1345TNPC		*ST*	108572447
1345FNPD*		FC-PC	108354523
1345CNPD*		SC	108354507
1345TNPD*		*ST*	108572454
1345FBPC	Requires +5 V or –5 V	FC-PC	108572355
1345CBPC		SC	108572298
1345TBPC		*ST*	108572397
1345FBPD*		FC-PC	108573965
1345CBPD*		SC	108572306
1345TBPD*		*ST*	108572413

* These versions have nonsquelching data and clock outputs. See Nonsquelched Data and Clock Outputs section on page 2.

Table 5. Related Products

Description	Document Number
1241/1243/1245-Type Receivers for SONET/SDH Applications	DS99-073LWP
1340-Type Receiver with Clock Recovery and Data Retiming	DS00-098LWP

Notes

Telcordia Technologies is a trademark of Telcordia Technologies Inc.
EIA is a registered trademark of Electronic Industries Association.
Signetics is a registered trademark of Signetics Corp.
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ISO is a registered trademark of The International Organization for Standardization.

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