

Dual Differential Transceivers BTK1A and BTM1A

Features

Driver Features

- Two line drivers per package
- Logic to convert TTL input logic levels to differential, pseudo-emitter coupled logic (ECL) output logic levels
- No line loading when $V_{cc} = 0\text{ V}$
- High output driver for $50\ \Omega$ loads
- 200 mA short-circuit current (typical)
- 2.0 ns maximum propagation delay
- $<0.2\text{ ns}$ output skew (typical)

Receiver Features

- Two line receivers per package
- High input impedance $\cong 8\text{ k}\Omega$
- Logic that converts differential input logic levels to transistor-transistor logic (TTL) output logic levels
- 4.0 ns maximum propagation delay
- $<0.20\text{ V}$ input sensitivity (typical)
- -1.2 V to $+7.2\text{ V}$ common-mode range

Common Device Features

- Common enable for each driver/receiver pair
- Operating temperature range: $-40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ (wider than the 41 Series)
- Single $5.0\text{ V} \pm 10\%$ supply
- 400 Mb/s maximum data rate
- Meets enhanced small device interface (ESDI) standards
- Electrostatic discharge (ESD) performance better than the 41 Series
- Lower power requirement than the 41 Series

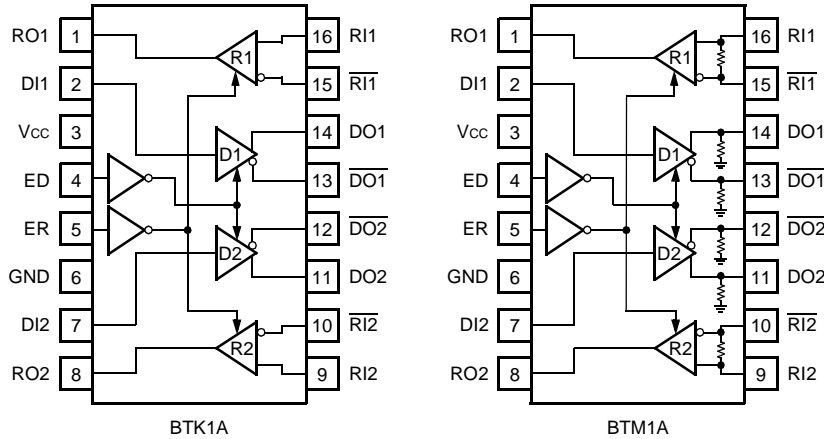
Description

The BTK1A and BTM1A devices are dual differential transceiver circuits that transmit and receive digital data over balanced transmission lines and are compatible with Agere Systems Inc. quad differential drivers and receivers. The dual drivers translate input TTL logic levels to differential pseudo-ECL output levels. The dual receivers convert differential input logic levels to TTL output levels. Each driver/receiver pair has its own common enable control allowing serial data and a control clock to be transmitted and received on a single integrated circuit. The BTK1A transceiver requires the customer to supply termination resistors on the circuit board. The BTM1A transceiver has an internal resistor termination for both the driver outputs ($220\ \Omega$) and receiver inputs ($110\ \Omega$), eliminating the need for external resistors on the circuit board when used with $100\ \Omega$ impedance, twisted-pair (or flat) cable. These transceivers replace the Agere 41 Series transceivers.

The powerdown loading characteristics of the receiver input circuit are approximately $8\text{ k}\Omega$ relative to the power supplies; hence, they will not load the transmission line when the circuit is powered down. For those circuits with termination resistors, the line will remain impedance matched when the circuit is powered down. The driver does not load the line when it is powered down.

The packaging options that are available for the dual differential transceivers include a 16-pin DIP; a 16-pin, J-lead SOJ; a 16-pin, gull-wing SOIC; and a 16-pin, narrow-body, gull-wing SOIC.

Pin Information



12-2747.b(F)

Figure 1. Differential Transceiver Logic Diagrams

Table 1. Enable Truth Table

ED	ER	D1	D2	R1	R2
0	0	Active	Active	Active	Active
1	0	Disabled	Disabled	Active	Active
0	1	Active	Active	Disabled	Disabled
1	1	Disabled	Disabled	Disabled	Disabled

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	Vcc	—	6.5	V
Ambient Operating Temperature	T _A	-40	125	°C
Storage Temperature	T _{stg}	-55	150	°C

Electrical Characteristics

For variations in electrical characteristics over the temperature range, see Figure 10 on page 10 through Figure 12 on page 11.

Table 3. Power Supply Current Characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current ($V_{CC} = 5.5\text{ V}$): All Outputs Disabled:					
BTK1A	I_{CC}	—	40	65	mA
BTM1A	I_{CC}	—	80	115	mA
All Outputs Enabled:					
BTK1A	I_{CC}	—	20	35	mA
BTM1A	I_{CC}	—	80	115	mA

Third State

These drivers produce pseudo-ECL levels, and the third-state mode is different than the conventional TTL devices. When a driver is placed in the third state, the bases of the output transistors are pulled low, bringing the outputs below the active-high and active-low levels. This voltage is typically 2 V for most drivers. In the bidirectional bus application, the driver of one device, which is in its third state, may be back driven by another driver on the bus whose voltage in the low state is lower than the third-stated device. This could come about due to differences in the drivers' independent power supplies. In this case, the device in the third state will control the line, thus clamping the line and reducing the signal swing. If the difference voltage between the independent power supplies and the drivers is small, then this consideration can be ignored. In the typical case, the difference voltage can be as much as 1 V without significantly affecting the amplitude of the driving signal.

Electrical Characteristics (continued)

Table 4. Driver Voltage and Current Characteristics

For variations in output voltage over the temperature range, see Figure 10 and Figure 11. $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages:					
Low*	V_{OL}	$V_{OH} - 1.4$	$V_{OH} - 1.1$	$V_{OH} - 0.65$	V
High*:	V_{OH}	$V_{CC} - 1.8$	$V_{CC} - 1$	$V_{CC} - 0.8$	V
Differential Voltage ($V_{OH} - V_{OL}$)	V_{DIFF}	0.65	1.1	1.4	V
Third State, $I_{OH} = -1.0\text{ mA}$, $V_{CC} = 4.5\text{ V}$	V_{OZ}	—	$V_{OL} - 0.5$	$V_{OL} - 0.2$	V
Output Voltages ($T_A = 0\text{ }^\circ\text{C}$ to $85\text{ }^\circ\text{C}$):					
Low*	V_{OL}	$V_{OH} - 1.4$	$V_{OH} - 1.1$	$V_{OH} - 0.8$	V
High*:	V_{OH}	$V_{CC} - 1.5$	$V_{CC} - 1$	$V_{CC} - 0.8$	V
Differential Voltage ($V_{OH} - V_{OL}$)	V_{DIFF}	0.8	1.1	1.4	V
Input Voltages:					
Low, $V_{CC} = 5.5\text{ V}$:					
Data Input	V_{IL}^\dagger	—	—	0.8	V
Enable Input	V_{IL}^\ddagger	—	—	0.8	V
High, $V_{CC} = 4.5\text{ V}$	V_{IH}^\dagger	2.0	—	—	V
Clamp, $V_{CC} = 4.5\text{ V}$, $I_I = -5.0\text{ mA}$	V_{IK}	—	—	-1.0	V
Short-circuit Output Current, $V_{CC} = 5.5\text{ V}$	I_{OS}^\S	-100	—	—	mA
Input Currents, $V_{CC} = 5.5\text{ V}$:					
Low, $V_I = 0.4\text{ V}$	I_{IL}	—	—	-400	μA
High, $V_I = 2.7\text{ V}$	I_{IH}	—	—	20	μA
Reverse, $V_I = 5.5\text{ V}$	I_{IH}	—	—	100	μA
Output Resistors:					
BTM1A [†]	R_O	—	220	—	Ω

* Values are with terminations as per Figure 7.

† The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

‡ Test must be performed one lead at a time to prevent damage to the device.

Electrical Characteristics (continued)

Table 5. Receiver Voltage and Current Characteristics

For variation in minimum V_{OH} and maximum V_{OL} over the temperature range, see Figure 10.

$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages $V_{CC} = 4.5\text{ V}$:					
Low, $I_{OL} = 8.0\text{ mA}^*$	V_{OL}	—	—	0.5	V
High, $I_{OH} = -400\text{ }\mu\text{A}$	V_{OH}	2.4	—	—	V
Enable Input Voltages:					
Low, $V_{CC} = 5.5\text{ V}$	V_{IL}^*	—	—	0.7	V
High, $V_{CC} = 4.5\text{ V}$	V_{IH}^*	2.0	—	—	V
Clamp, $V_{CC} = 4.5\text{ V}$, $I_I = -5.0\text{ mA}$	V_{IK}	—	—	-1.0	V
Minimum Differential Input Voltages, $V_{IH} - V_{IL}^\dagger$ $-0.80\text{ V} < V_{IH} < 7.2\text{ V}$, $-1.2\text{ V} < V_{IL} < 6.8\text{ V}$	V_{TH}^*	—	0.1	0.20	V
Input Offset Voltage	V_{OFF}	—	0.03	0.05	V
Output Currents, $V_{CC} = 5.5\text{ V}$:					
Off-state (high Z), $V_O = 0.4\text{ V}$	I_{OZL}	—	—	-20	μA
Off-state (high Z), $V_O = 2.4\text{ V}$	I_{OZH}	—	—	20	μA
Short Circuit	I_{OS}^\ddagger	-25	—	-100	mA
Enable Input Currents, $V_{CC} = 5.5\text{ V}$:					
Low, $V_{IN} = 0.4\text{ V}$	I_{IL}	—	—	-400	μA
High, $V_{IN} = 2.7\text{ V}$	I_{IH}	—	—	20	μA
Reverse, $V_{IN} = 5.5\text{ V}$	I_{IH}	—	—	100	μA
Differential Input Currents, (BTK1A):					
Low, $V_{IN} = -1.2\text{ V}$	I_{IL}	—	—	-1.0	mA
High, $V_{IN} = 7.2\text{ V}$	I_{IH}	—	—	1.0	mA
Differential Input Impedance (BTM1A): Connected Between R_I and $\overline{R_I}$	R_I	—	110	—	Ω

* The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.

† Outputs of unused receivers assume a logic 1 level when the inputs are left open. (It is recommended that all unused positive inputs be tied to the positive power supply. No external series resistor is required.)

‡ Test must be performed one lead at a time to prevent damage to the device.

Timing Characteristics

Table 6. Driver Timing Characteristics (See Figure 3 and Figure 4.)

For t_{P1} and t_{P2} propagation delays over the temperature range, see Figure 13. Propagation delay test circuit connected to output is shown in Figure 7. $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay:					
Input High to Output†	t_{P1}^*	0.8	1.2	2.0	ns
Input Low to Output†	t_{P2}^*	0.8	1.2	2.0	ns
Capacitive Delay	Δt_p	—	0.02	0.03	ns/pF
Disable Time (either E1 or E2):					
High-to-High Impedance	t_{PHZ}	4	8	12	ns
Low-to-High Impedance	t_{PLZ}	4	8	12	ns
Enable Time (either E1 or E2):					
High Impedance to High	t_{PZH}	4	8	12	ns
High Impedance to Low	t_{PZL}	4	8	12	ns
Output Skew:					
$ t_{P1} - t_{P2} $	t_{skew1}	—	0.1	0.3	ns
$ t_{PHH} - t_{PHL} , t_{PLH} - t_{PLL} $	t_{skew2}	—	0.2	0.5	ns
Difference Between Drivers	Δt_{skew}	—	—	0.3	ns
Rise Time (20%—80%)	t_{rLH}	—	0.7	2	ns
Fall Time (80%—20%)	t_{fHL}	—	0.7	2	ns

* t_{P1} and t_{P2} are measured from the 1.5 V point of the input to the crossover point of the outputs (see Figure 3).

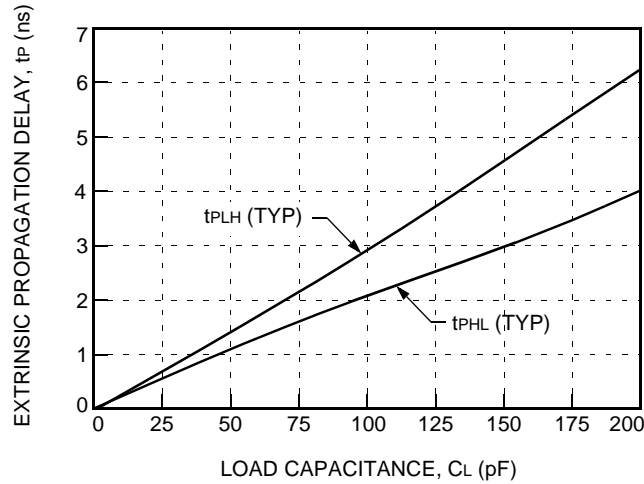
† $C_L = 5\text{ pF}$. Capacitor is connected from each output to ground.

Table 7. Receiver Timing Characteristics (See Figure 5 and Figure 6.)

For propagation delays (t_{PLH} and t_{PHL}) over the temperature range, see Figure 14 and Figure 15. Propagation delay test circuit connected to output is shown in Figure 8. $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay:					
Input to Output High	t_{PLH}	1.5	2.5	4.0	ns
Input to Output Low	t_{PHL}	1.5	2.5	4.0	ns
Pulse Width Distortion, $t_{pHL} - t_{pLH}$:					
Load Capacitance (C_L) = 15 pF	t_{skew1}	—	—	0.7	ns
Load Capacitance (C_L) = 150 pF	t_{skew1}	—	—	4.0	ns
Output Waveform Skews:					
Part-to-Part Skew, $T_A = 75\text{ }^\circ\text{C}$	$\Delta t_{skew1p-p}$	—	0.8	1.4	ns
Part-to-Part Skew, $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$	$\Delta t_{skew1p-p}$	—	—	1.5	ns
Same Part Skew	Δt_{skew}	—	—	0.3	ns
Disable Time, $C_L = 5\text{ pF}$:					
High-to-high Impedance	t_{PHZ}	—	5	12	ns
Low-to-high Impedance	t_{PLZ}	—	5	12	ns
Enable Time:					
High Impedance to High	t_{PZH}	—	8	12	ns
High Impedance to Low	t_{PZL}	—	8	12	ns
Rise Time (20%—80%)	t_{rLH}	—	—	3.0	ns
Fall Time (80%—20%)	t_{fHL}	—	—	3.0	ns

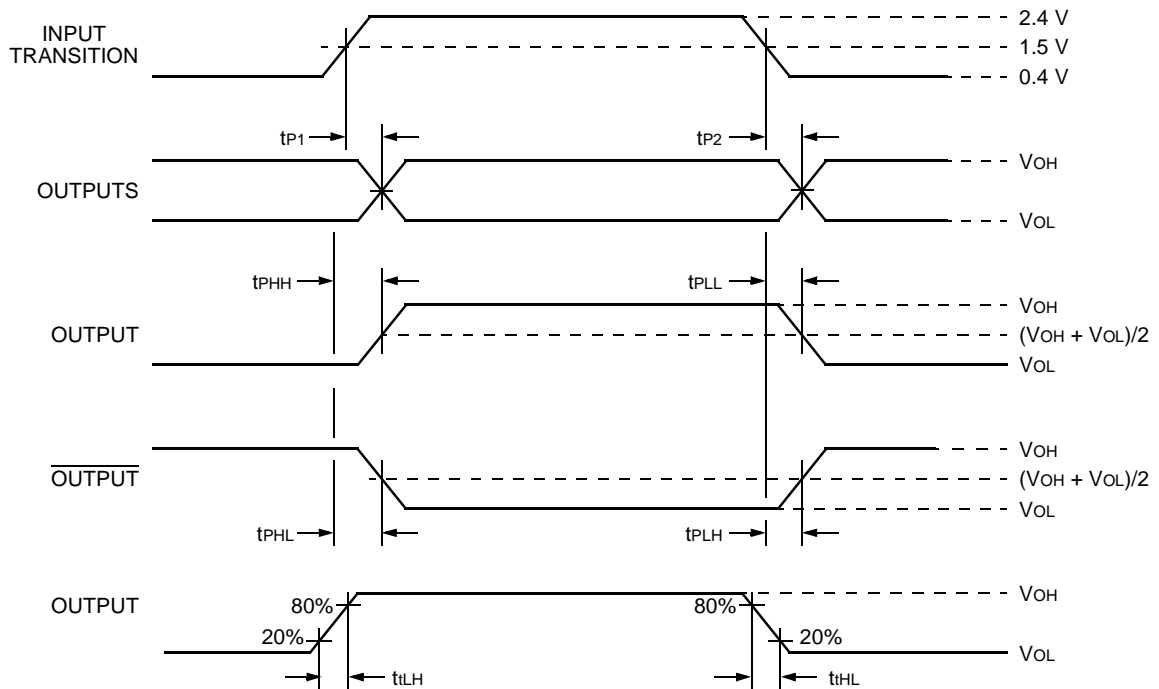
Timing Characteristics (continued)



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Note: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to the external capacitance and the intrinsic delay of the device.

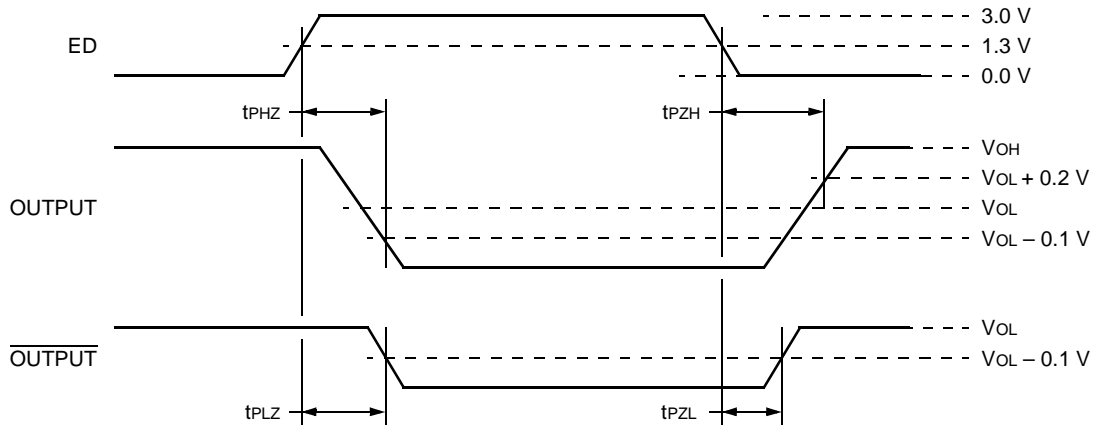
Figure 2. Typical Extrinsic Propagation Delay Versus Load Capacitance at 25 °C



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Figure 3. Driver Propagation Delay Timing

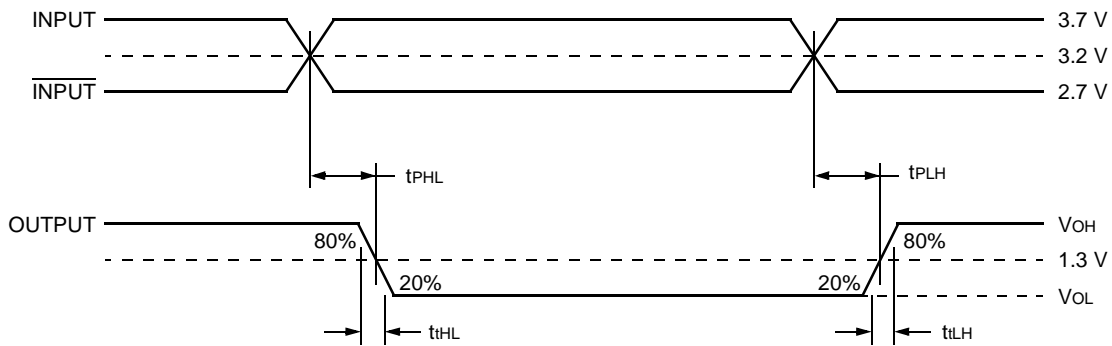
Timing Characteristics (continued)



12-2268.c(F)

Note: In the third state, both outputs (i.e., OUTPUT and $\overline{\text{OUTPUT}}$) are 0.1 V below the low state.

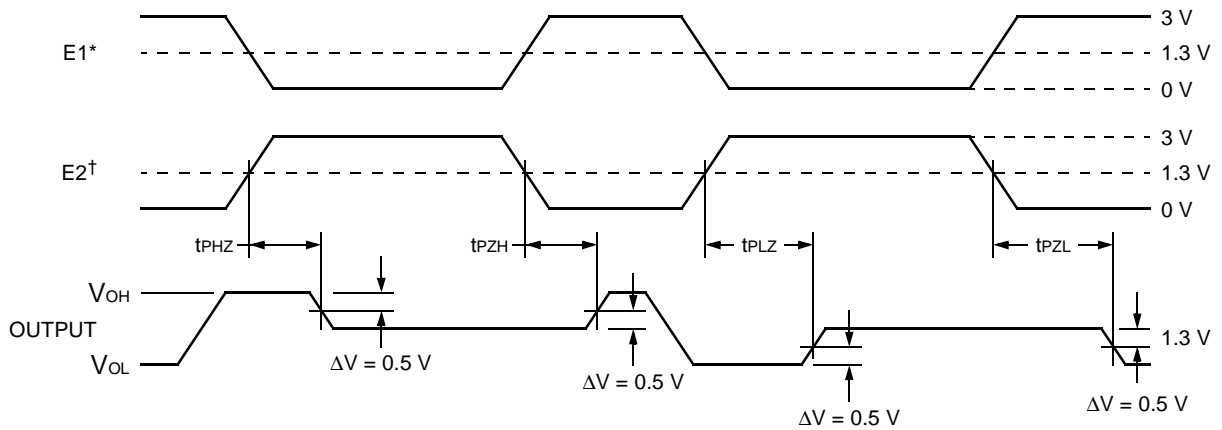
Figure 4. Driver Enable and Disable Timing



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Figure 5. Receiver Propagation Delay Timing

Timing Characteristics (continued)



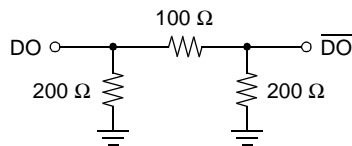
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* E2 = 1 while E1 changes state.
† E1 = 0 while E2 changes state.

Figure 6. Receiver Enable and Disable Timing

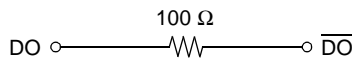
Test Conditions

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.



12-2271.a(F)

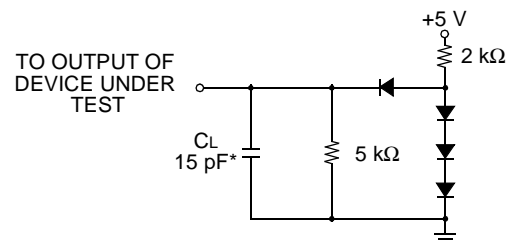
BTK1A



12-2271.b(F)

BTM1A

Figure 7. Driver Propagation Delay Test Circuit



12-2249(F)

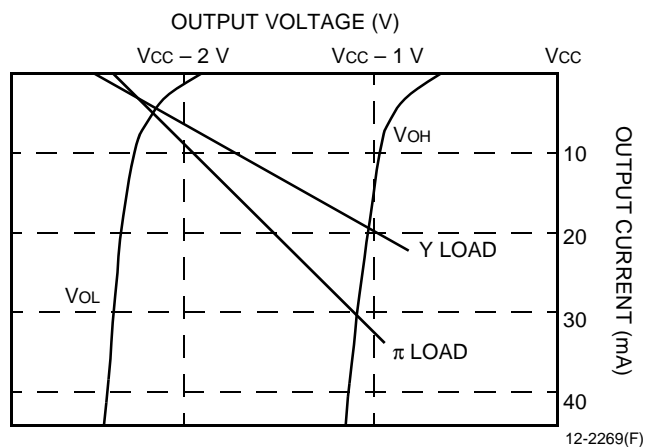
* Includes probe and jig capacitances.

Note: All 458E, IN4148, or equivalent diodes.

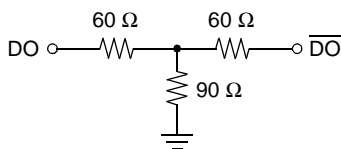
Figure 8. Receiver Propagation Delay Test Circuit

Output Characteristics

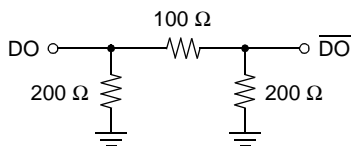
Figure 9 illustrates typical driver output characteristics. Included are load lines for two typical termination configurations.



A. Output Current vs. Output Voltage for Loads Shown in B and C



B. Y Load



C. π Load

Figure 9. Driver Output Current Versus Voltage Characteristics

Temperature Characteristics

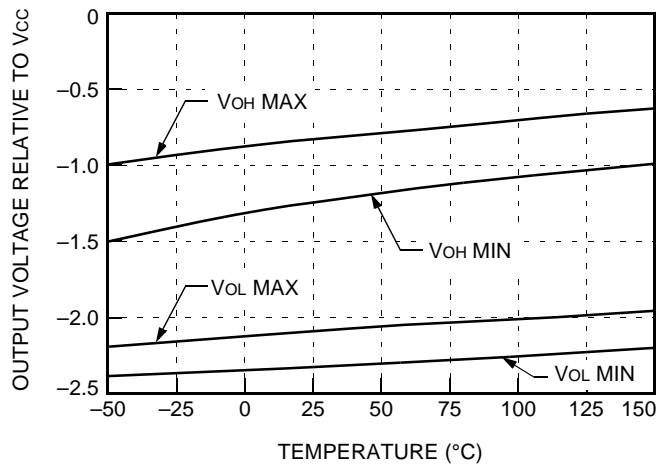


Figure 10. V_{OL} and V_{OH} Extremes for Drivers Versus Temperature for 100 Ω Load

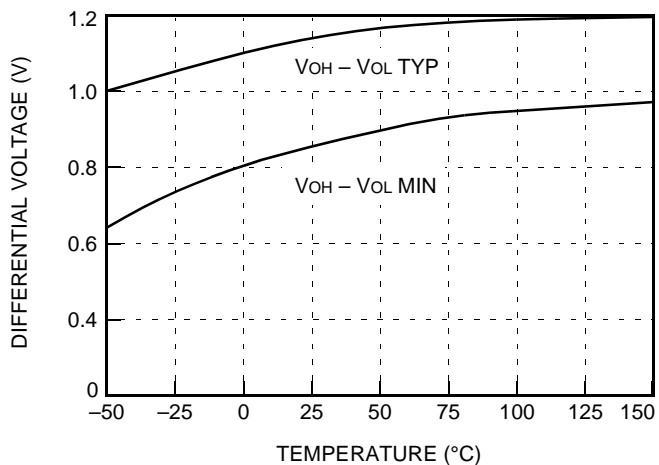
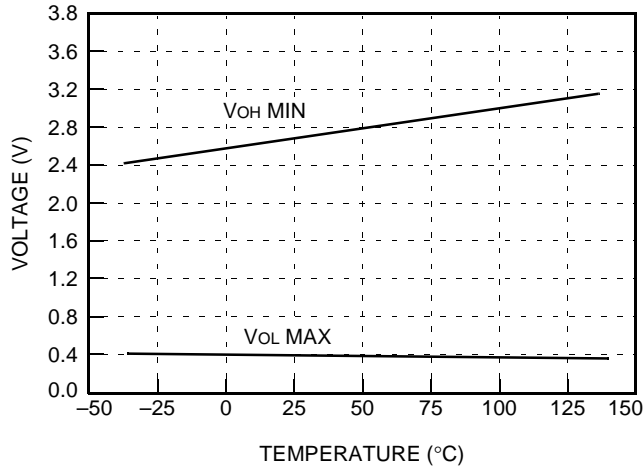


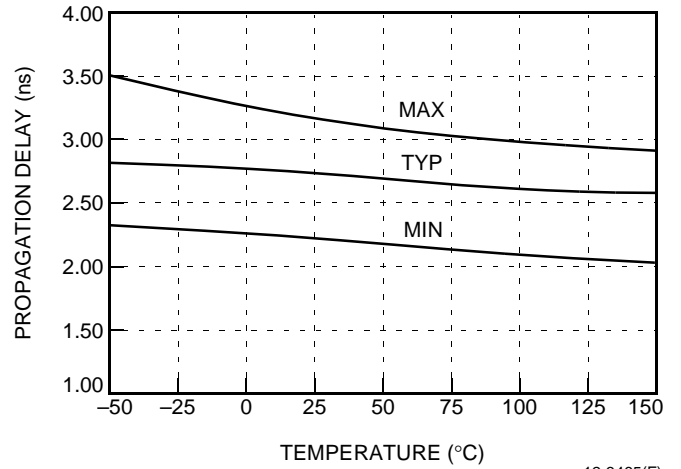
Figure 11. Differential Voltage (V_{OH} - V_{OL}) for Drivers Versus Temperature

Temperature Characteristics (continued)



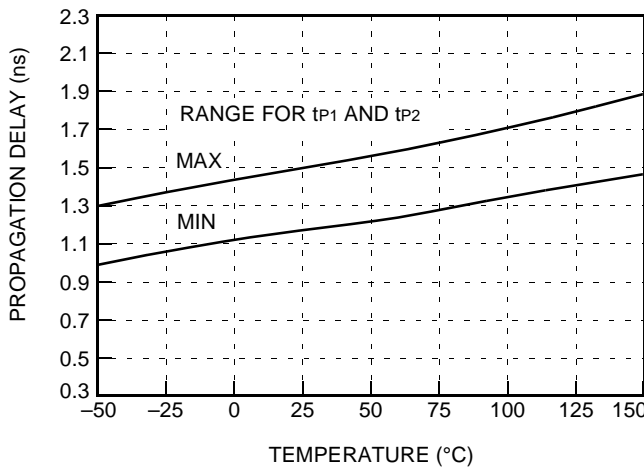
12-3464.b(F)

Figure 12. Minimum V_{OH} and Maximum V_{OL} Versus Temperature at $V_{CC} = 4.5$ V for the Receiver



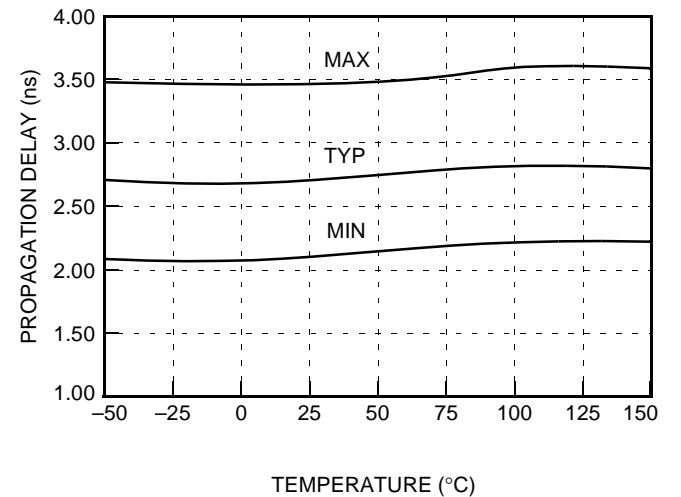
12-3465(F)

Figure 14. Propagation Delay for a High Output (t_{PLH}) Versus Temperature at $V_{CC} = 5.0$ V for the Receivers



12-3469.a(F)

Figure 13. Min and Max for t_{P1} and t_{P2} Propagation Delays Versus Temperature for the Driver



12-3466(F)

Figure 15. Propagation Delay for a Low Output (t_{PHL}) Versus Temperature at $V_{CC} = 5.0$ V for the Receivers

Handling Precautions

CAUTION: This device is susceptible to damage as a result of electrostatic discharge. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

When handling and mounting line driver products, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD). The user should adhere to the following basic rules for ESD control:

1. Assume that all electronic components are sensitive to ESD damage.
2. Never touch a sensitive component unless properly grounded.
3. Never transport, store, or handle sensitive components except in a static-safe environment.

ESD Failure Models

Agere employs two models for ESD events that can cause device damage or failure:

1. A human-body model (HBM) that is used by most of the industry for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1500 Ω , capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.
2. A charged-device model (CDM), which many believe is the better simulator of electronics manufacturing exposure.

Table 8 and Table 9 illustrate the role these two models play in the overall prevention of ESD damage. HBM ESD testing is intended to simulate an ESD event from a charged person. The CDM ESD testing simulates charging and discharging events that occur in production equipment and processes, e.g., an integrated circuit sliding down a shipping tube.

The HBM ESD threshold voltage presented here was obtained by using these circuit parameters.

Table 8. Typical ESD Thresholds for Data Transmission Transceivers

Device	HBM Threshold	CDM Threshold
BTK1A BTM1A	>800	>1000
All other pins	>2000	>1000

Table 9. ESD Damage Protection

	ESD Threat Controls	
	Personnel	Processes
Control	Wrist straps ESD shoes Antistatic flooring	Static-dissipative materials Air ionization
Model	Human-body model (HBM)	Charged-device model (CDM)

Latch-Up

Latch-up evaluation has been performed on the data transmission receivers. Latch-up testing determines if the power-supply current exceeds the specified maximum due to the application of a stress to the device under test. A device is considered susceptible to latch-up if the power supply current exceeds the maximum level and remains at that level after the stress is removed.

Agere performs latch-up testing per an internal test method which is consistent with JEDEC Standard No. 17 (previously JC-40.2) *CMOS Latch-Up Standardized Test Procedure*.

Latch-up evaluation involves the following three separate stresses to evaluate latch-up susceptibility levels:

1. dc current stressing of input and output pins.
2. Power supply slew rate.
3. Power supply overvoltage.

Table 10. Latch-Up Test Criteria and Test Results

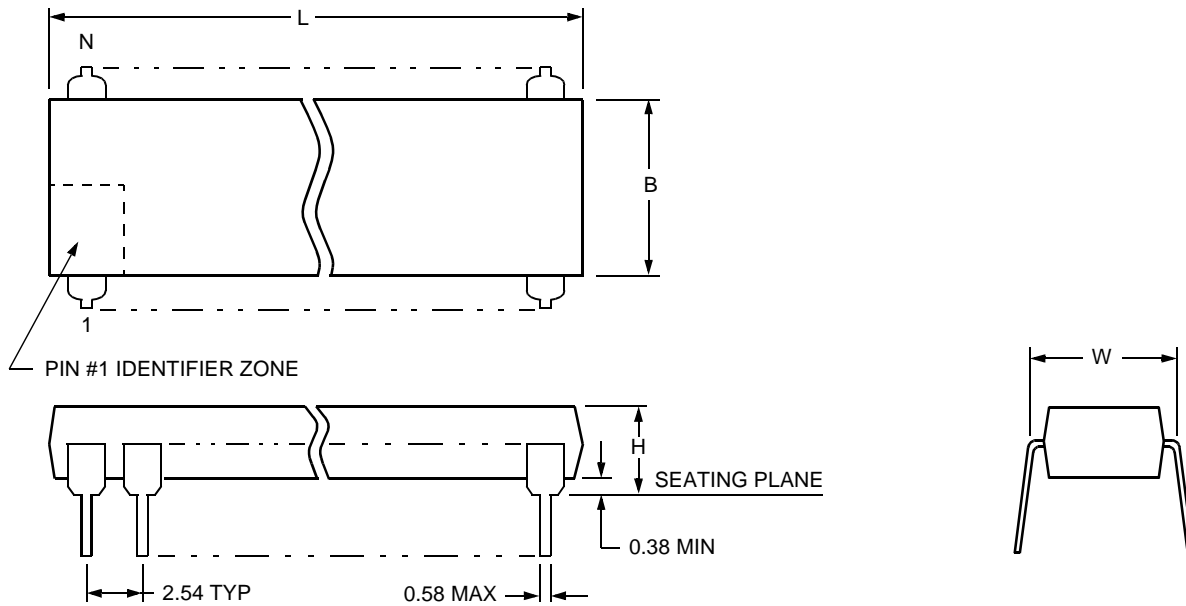
		dc Current Stress of I/O Pins	Power Supply Slew Rate	Power Supply Overvoltage
Data Transmission Receiver ICs	Minimum Criteria	≥150 mA	≤1 μs	≥1.75 x Vmax
	Test Results	≥250 mA	≤100 ns	≥2.25 x Vmax

Based on the results in Table 10, the data transmission receivers pass the Agere latch-up testing requirements and are considered not susceptible to latch-up.

Outline Diagrams

16-Pin DIP

Dimensions are in millimeters.



5-4410(F)

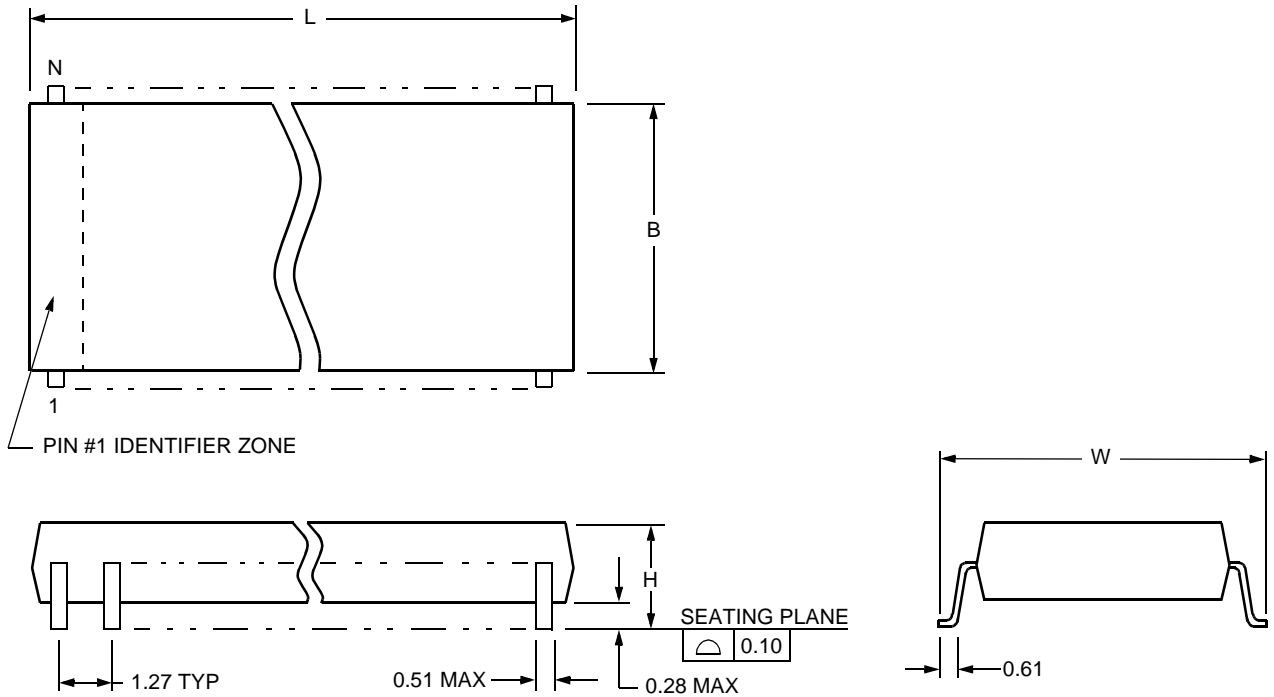
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
PDIP3 (Plastic Dual-In-Line Package)	16	20.57	6.48	7.87	5.08

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

Outline Diagrams (continued)

16-Pin SOIC (SONB/SOG)

Dimensions are in millimeters.



5-4414(F)

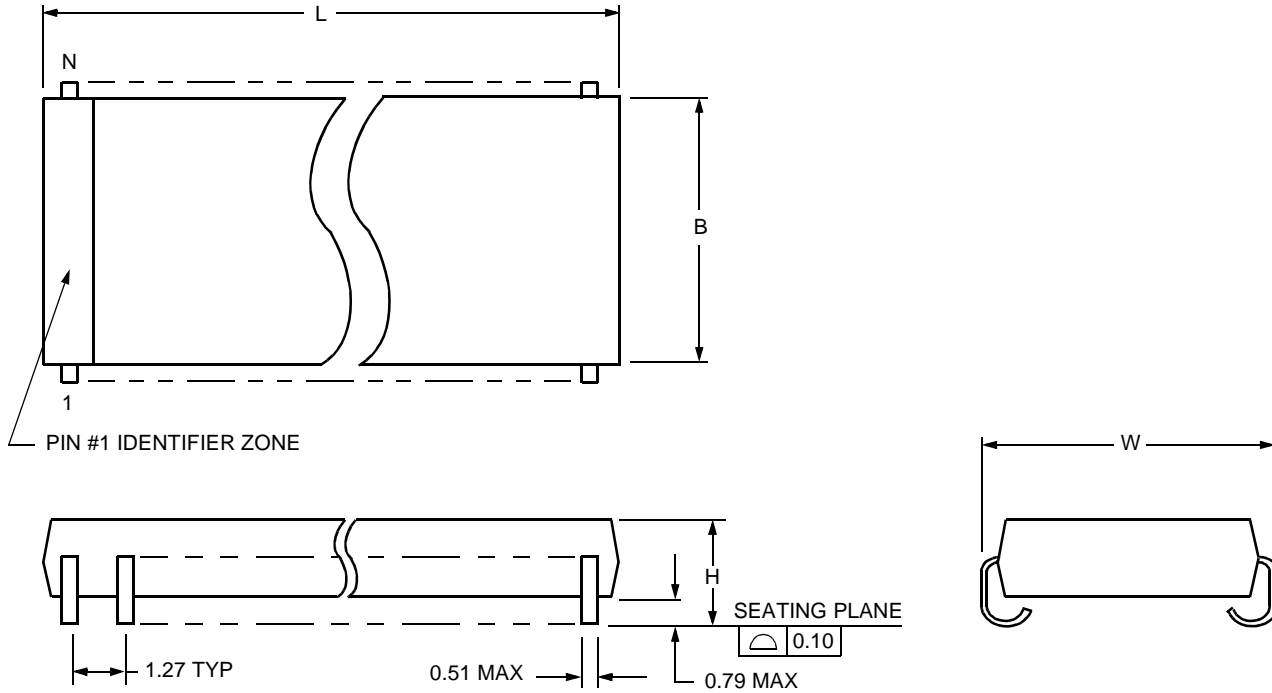
Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
SONB (Small-Outline, Narrow Body)	16	10.11	4.01	6.17	1.73
SOG (Small-Outline, Gull-Wing)	16	10.49	7.62	10.64	2.67

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

Outline Diagrams (continued)

16-Pin SOIC (SOJ)

Dimensions are in millimeters.



5-4413(F)r.3

Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
SOJ (Small-Outline, J-Lead)	16	10.41	7.62	8.81	3.18

Note: The dimensions in this outline diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Agere Sales Representative.

Power Dissipation

System designers incorporating Agere data transmission drivers in their applications should be aware of package and thermal information associated with these components.

Proper thermal management is essential to the long-term reliability of any plastic encapsulated integrated circuit. Thermal management is especially important for surface-mount devices, given the increasing circuit pack density and resulting higher thermal density. A key aspect of thermal management involves the junction temperature (silicon temperature) of the integrated circuit.

Several factors contribute to the resulting junction temperature of an integrated circuit:

- Ambient use temperature
- Device power dissipation
- Component placement on the board
- Thermal properties of the board
- Thermal impedance of the package

Thermal impedance of the package is referred to as Θ_{ja} and is measured in °C rise in junction temperature per watt of power dissipation. Thermal impedance is also a function of airflow present in system application.

The following equation can be used to estimate the junction temperature of any device:

$$T_j = T_A + P_D \Theta_{ja}$$

where:

T_j is device junction temperature (°C).

T_A is ambient temperature (°C).

P_D is power dissipation (W).

Θ_{ja} is package thermal impedance (junction to ambient—°C/W).

The power dissipation estimate is derived from two factors:

- Internal device power
- Power associated with output terminations

Multiplying I_{cc} times V_{cc} provides an estimate of internal power dissipation.

The power dissipated in the output is a function of the:

- Termination scheme on the outputs
- Termination resistors
- Duty cycle of the output

Package thermal impedance depends on:

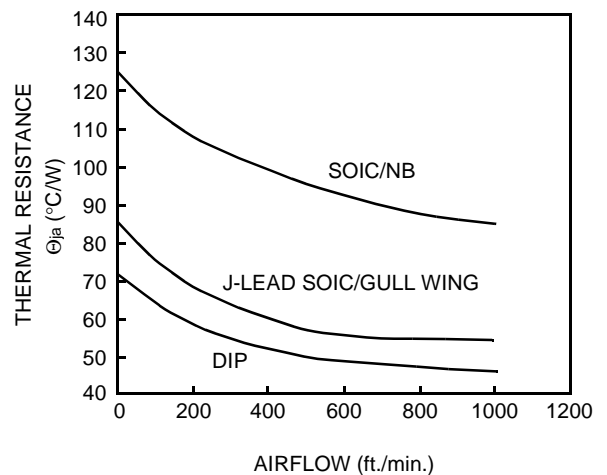
- Airflow
- Package type (e.g., DIP, SOIC, SOIC/NB)

The junction temperature can be calculated using the previous equation, after power dissipation levels and package thermal impedances are known.

Figure 16 illustrates the thermal impedance estimates for the various package types as a function of airflow. This figure shows that package thermal impedance is higher for the narrow-body SOIC package. Particular attention should, therefore, be paid to the thermal management issues when using this package type.

In general, system designers should attempt to maintain junction temperature below 125 °C. The following factors should be used to determine if specific data transmission drivers in particular package types meet the system reliability objectives:

- System ambient temperature
- Power dissipation
- Package type
- Airflow



12-2753F

Figure 16. Power Dissipation

Ordering Information

Part Number	Driver Termination*	Receiver Termination†	Package Type	Comcode	Former Pkg. Type	Former Part Number
BTK1A16E	None	None	16-pin, Plastic SOJ	107950347	1041	LK, MK
BTK1A16E-TR	None	None	Tape & Reel SOJ	107950354	1041	LK, MK, -TR
BTK1A16G	None	None	16-pin, Plastic SOIC	107950362	1141	LK, MK
BTK1A16G-TR	None	None	Tape & Reel SOIC	107950370	1141	LK, MK, -TR
BTK1A16NB	None	None	Plastic SOIC/NB	107950388	1241	LK, MK
BTK1A16NB-TR	None	None	Tape & Reel SOIC/NB	107950396	1241	LK, MK, -TR
BTK1A16P	None	None	16-pin, Plastic DIP	107950404	41	LK, MK
BTM1A16E	220 Ω	110 Ω	16-pin, Plastic SOJ	107950537	1041	LM, MM
BTM1A16E-TR	220 Ω	110 Ω	Tape & Reel SOJ	107950545	1041	LM, MM, -TR
BTM1A16G	220 Ω	110 Ω	16-pin, Plastic SOIC	107950552	1141	LM, MM
BTM1A16G-TR	220 Ω	110 Ω	Tape & Reel SOIC	107950560	1141	LM, MM, -TR
BTM1A16NB	220 Ω	110 Ω	Plastic SOIC/NB	107950578	1241	LM, MM
BTM1A16NB-TR	220 Ω	110 Ω	Tape & Reel SOIC/NB	107950586	1241	LM, MM, -TR
BTM1A16P	220 Ω	110 Ω	16-pin, Plastic DIP	107950594	41	LM, MM

* Indicates on-chip output terminating resistors from each driver output to ground.

† Indicates on-chip input terminations across receiver inputs.

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