Data Sheet
June 1999

microelectronics group

Lucent Technologies
Bell Labs Innovations

CDRM622
622 Mbits/s Multichannel Digital Timing Recovery

Features

- Receives scrambled serial data at STS-12/STM-4 (622.08 Mbits/s) rate.
- Demultiplexes serial data to 77.76 Mbytes/s parallel byte wide data with aligned 77.76 MHz clock.
- Synthesizes 622.06 MHz clock with on-chip PLL, requiring only 77.76 MHz input reference clock and one external resistor.
- Multiplexes parallel 77.76 Mbytes/s data to 622 Mbits/s serial data for transmission.
- Incorporates n = 1 to 16 channels with modular design. Implemented in Lucent Technologies Microelectronics Group HL250C technology.
- Meets type B jitter tolerance specification of ITU-T Recommendation G.958.
- Sources stable clock in absence of data transitions once the clock synthesizer has acquired lock.
- Uses single, low-voltage (3.3 V ± 5%) supply.
- Includes built-in test circuitry such as high-speed loopback of transmit data into receiver.
- IDDQ compatible.
- Powers down the receiver on per-channel basis.
- Allows JTAG access to high-speed data paths.

Description

The CDRM622 provides a physical medium for high-speed asynchronous serial data transfer between ASIC devices. Devices can be on the same PC-board, or on separate boards connected across a backplane, or connected by cables. The macrocell is intended for, but not limited to, terminal equipment in SONET/SDH and ATM systems.

The macrocell consists of three functional blocks.

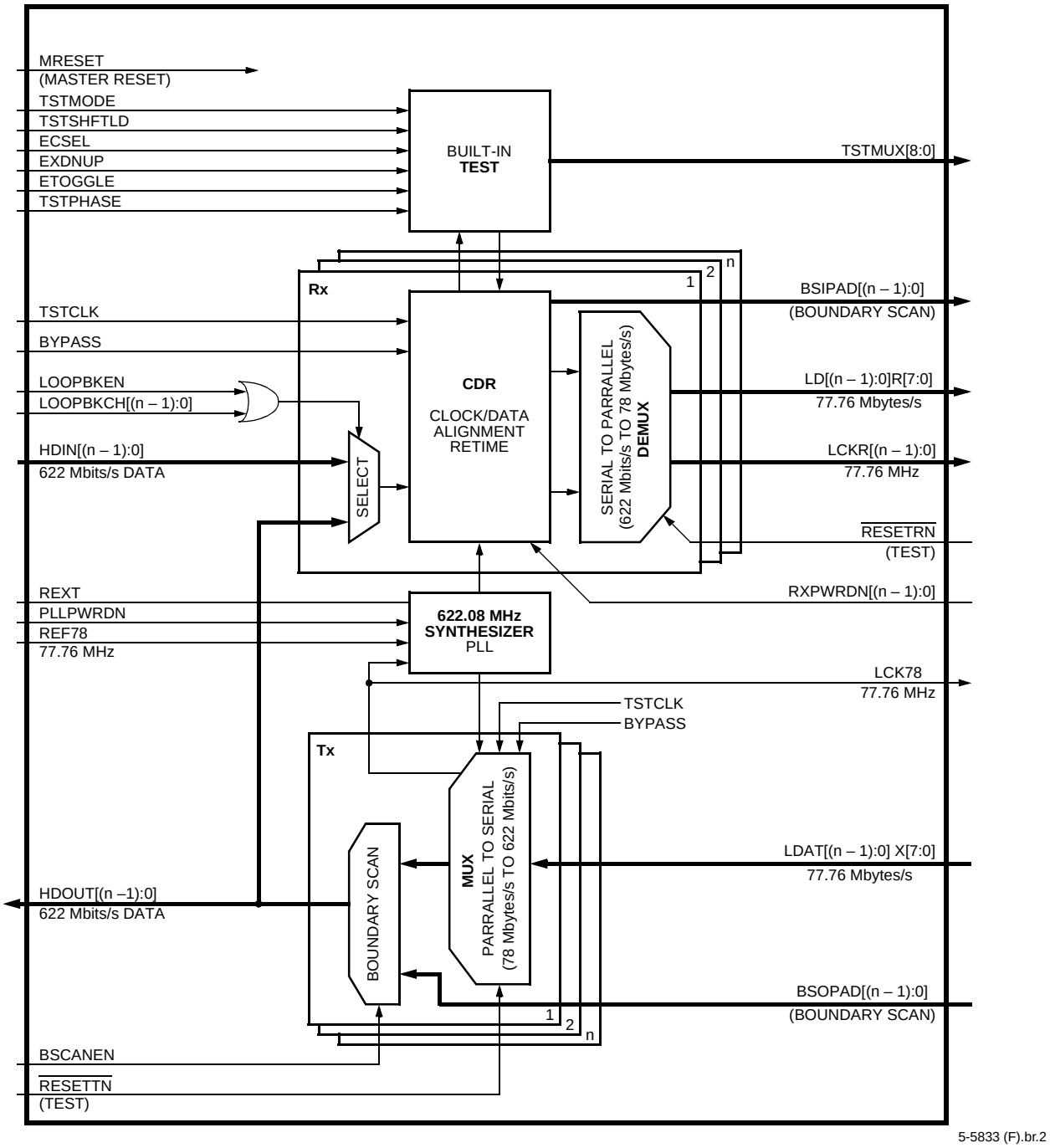
The receiver accepts 622.08 Mbits/s serial data. Based on data transitions, the receiver selects an appropriate 622 MHz clock phase for each channel to retime the data, then demultiplexes down to 77.76 Mbytes/s parallel bytes and a 77.76 MHz clock.

The transmitter operates in the reverse direction. 77.76 Mbytes/s parallel bytes are multiplexed up to 662.08 Mbits/s serial data for off-chip communication.

The clock synthesizer generates the necessary 622.08 MHz clock for operation from a 77.76 MHz reference. Figure 1 illustrates the function of the macrocell.

The hard macrocell can be supplied for up to 16 data channels. Multiple macrocells can be used on a single device. The macrocell is intended to be used with high-speed differential I/O buffers for the 622 Mbits/s serial data streams and the 77.76 MHz reference clock. Common selections are low-voltage differential swing (LVDS) or PECL. The I/O buffers are part of our standard-cell ASIC library and are not included in the macrocell to allow for flexibility.

Description (continued)



5-5833 (F).br.2

Figure 1. CDRM622 Block Diagram

Description (continued)

Physical Size

The macrocell is able to support up to 16 channels of serial data; however, the physical design will be limited to two sizes (8 and 16). Unused receivers will be powered down for specific applications as the physical size of the macrocell does not vary directly with channels. The physical dimensions of a 16-channel macrocell are approximately square at 2.2 mm per side.

Power Dissipation

At 3.3 V, power is estimated by 300 mW + 50 mW per Rx channel + 10 mW per Tx channel.

Device IO Buffers

Device IO buffers are not part of the hard macrocell. This allows customers to choose the most appropriate interface levels without disturbing the macrocell. Common choices of device interface levels are LVDS (low-voltage differential swing) and PECL. Device pinout is also flexible. Appropriate buffering will be added to the device by Lucent Technologies Microelectronics Group to ensure data integrity between the IO buffers and the macrocell.

Hardware Interface

Table 1. Functional Signals

Signal Name	Type	Description
HDIN[(n – 1):0]	I	622.08 Mbits/s serial data inputs. One input for each independent data channel.
LD[(n – 1):0]R[7:0]	O	Low-speed demultiplexed data bytes retimed to recovered 77.76 MHz clocks.
LCKR[(n – 1):0]	O	Low-speed 77.76 MHz recovered clocks.
LCK78	O	Low-speed (77.76 MHz) PLL divide-down clock. Can be used as a PLL activity monitor point. This buffered version of internal transmit 77.76 MHz clock can be used to time data transfer into the transmitter.
LDAT[(n – 1):0]X[7:0]	I	77.76 MHz data byte inputs to transmitter.
HDOUT[(n – 1):0]	O	622.08 Mbits/s serial data outputs.
REF78	I	77.76 MHz reference clock input to clock synthesizer.
REXT	I	Connects to external 10 kΩ ± 1% resistor that is tied to ground potential (V_{SSA}) on the circuit pack. Provides reference current to on-chip PLL.
MRESET	I	**(Active-High).** Asynchronous master reset for macrocell initialization. Also used in test mode to reset test circuitry.
PLLPWRDN	I	**(Active-High).** PLL powerdown for I_{DDQ} testing.
RXPWRDN[(n – 1):0]	I	**(Active-High).** Per-channel powerdown of receiver.

Low-Speed 77.76 Mbytes/s Interface

The internal timing performance of the macrocell is independent of the remaining device logic with the exception of the low-speed interface. The macrocell sources clock and data bytes for each channel to be captured and processed by the device logic. In the other direction, the device logic sources data bytes to be captured and processed by the macrocell. These interfaces are generally designed and verified using static timing analysis. Figure 2 illustrates these interfaces and their associated timing.

Input Capacitance

For all digital inputs, the input capacitance at the boundary of the macrocell is 0.02 pF.

Output Signal Drive Strength

For all low-speed outputs, the output driver strength is equivalent to that of a Lucent-type SBNS standard cell. (See *HL250C 3.3 Volt 0.25 µm CMOS Standard-Cell Library*, System ASIC Data Book March 1998 (MN97-066ASIC)).

Hardware Interface (continued)

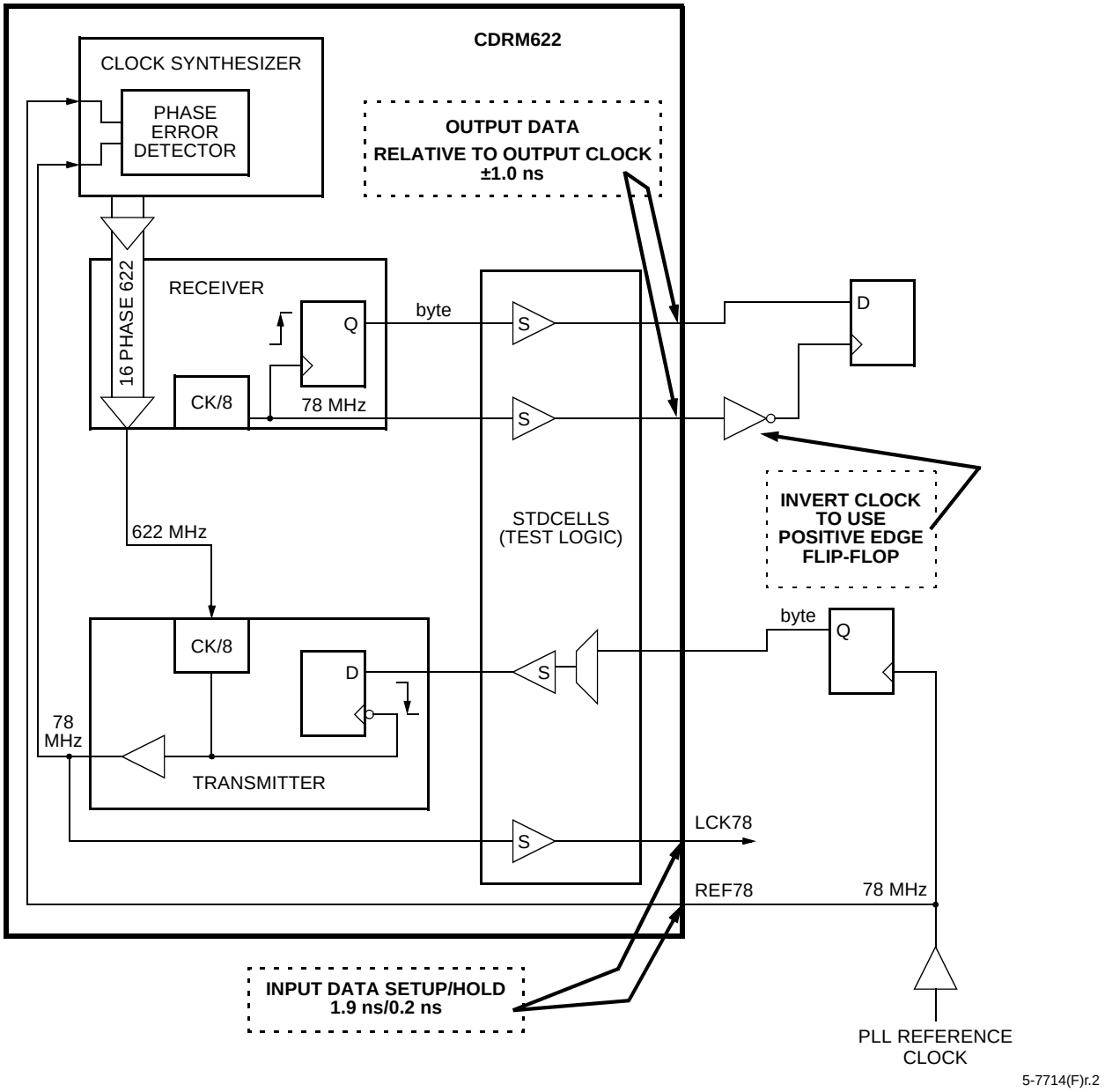


Figure 2. 78 MHz Interfaces

Simulation Interface

Table 2. Simulation Signals

Signal Name	Type	Description
BYPASS	I	**(Active-High).** Enables functional bypassing of the 622 MHz clock synthesis with TSTCLK. Receiver and transmitter pass data in a logically correct manner based on the test clock timing.
TSTCLK	I	Test clock for emulation of 622.08 MHz clock during PLL bypass. This input can run up to 155 MHz for factory testing. Also used for low-speed fault coverage testing.
$\overline{\text{RESETTN}}$	I	**(Active-Low).** Resets transmitter clock division counter to enable synchronizing the internal 77.76 MHz clock to the reference clock during PLL bypass.
$\overline{\text{RESETRN}}$	I	**(Active-Low).** Resets receiver clock division counter to enable synchronizing the recovered 77.76 MHz clocks to the reference clock during PLL bypass.

PLL Bypass

Device simulating, debugging, and testing with a working PLL is not recommended. Therefore, a test mode that bypasses the PLL is provided. Functional simulation and factory testing can make use of this mode. The logic of the data paths remain functional. Only the 622.08 MHz clock source is changed to the test clock. For factory testing, the PLL is separately exercised and monitored through the test port. Figure 3 illustrates this mode.

Logical Timing

Figure 4 and Figure 5 illustrate the functional timing relationships during PLL bypass mode operation.

Internal Clock Synchronization

When the PLL is bypassed, the internal clock dividers are not automatically aligned with the phase of the input reference clock. Resets are provided as an aid to force a relationship. During PLL bypass, the clock dividers are clocked by the test clock. The first falling edge of the test clock after the resets become inactive will generate a rising edge of the internal 77.76 MHz clocks. PLL bypass simulation test benches should be designed so that the device input signals driving TSTCLK, REF78, $\overline{\text{RESETRN}}$, and $\overline{\text{RESETTN}}$ are sequenced to closely align the internal clocks with the reference clock. Figure 6 illustrates this sequence.

Simulation Interface (continued)

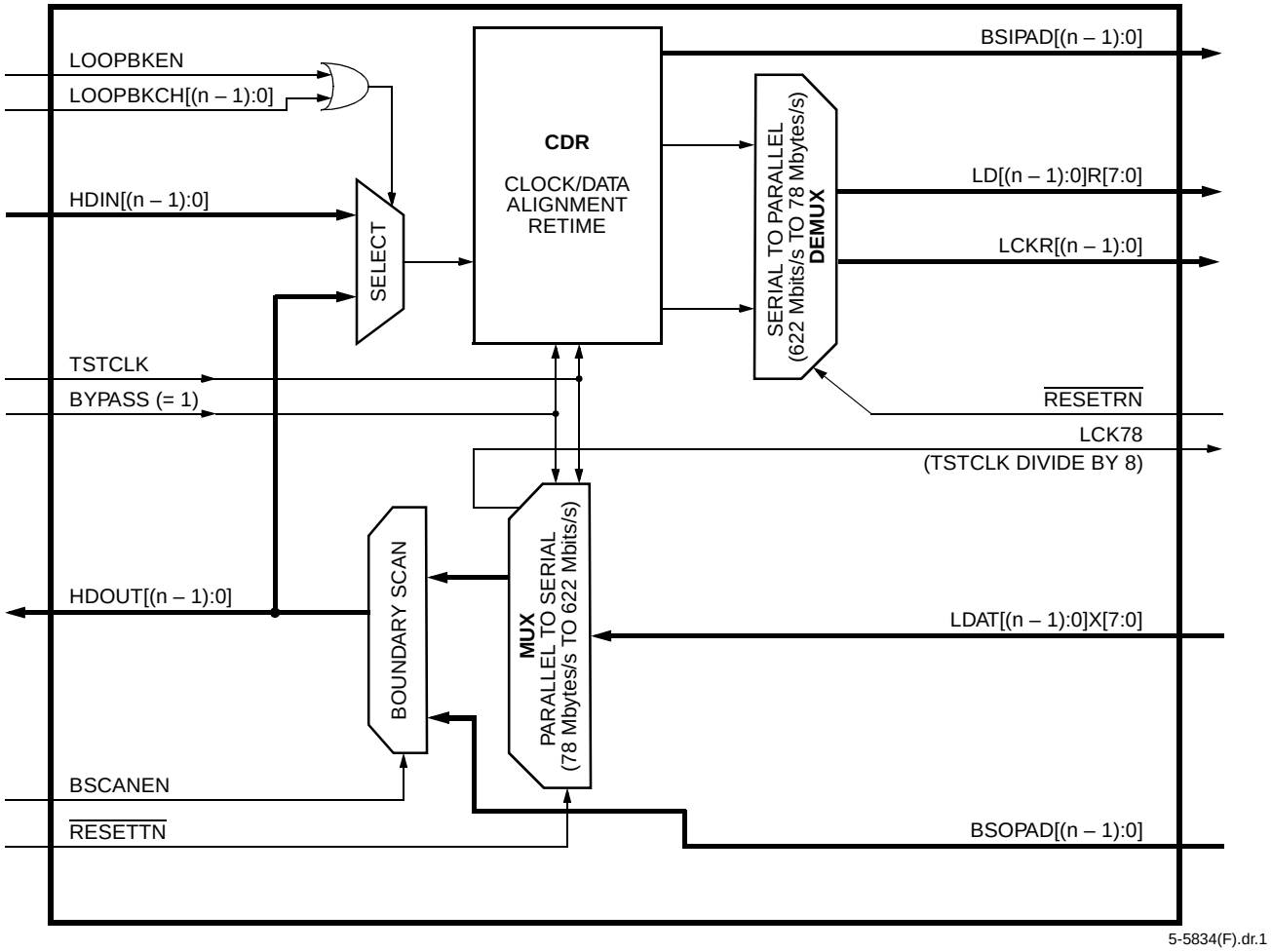


Figure 3. PLL Bypass Mode Block Diagram

Simulation Interface (continued)

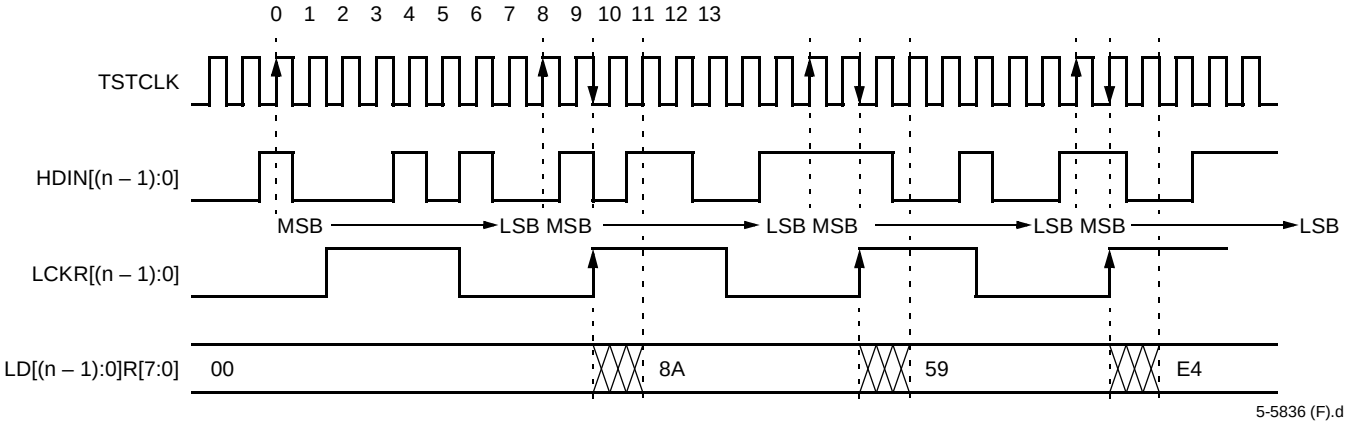


Figure 4. 622.08 Mbits/s Receive (PLL Bypass Mode) Timing

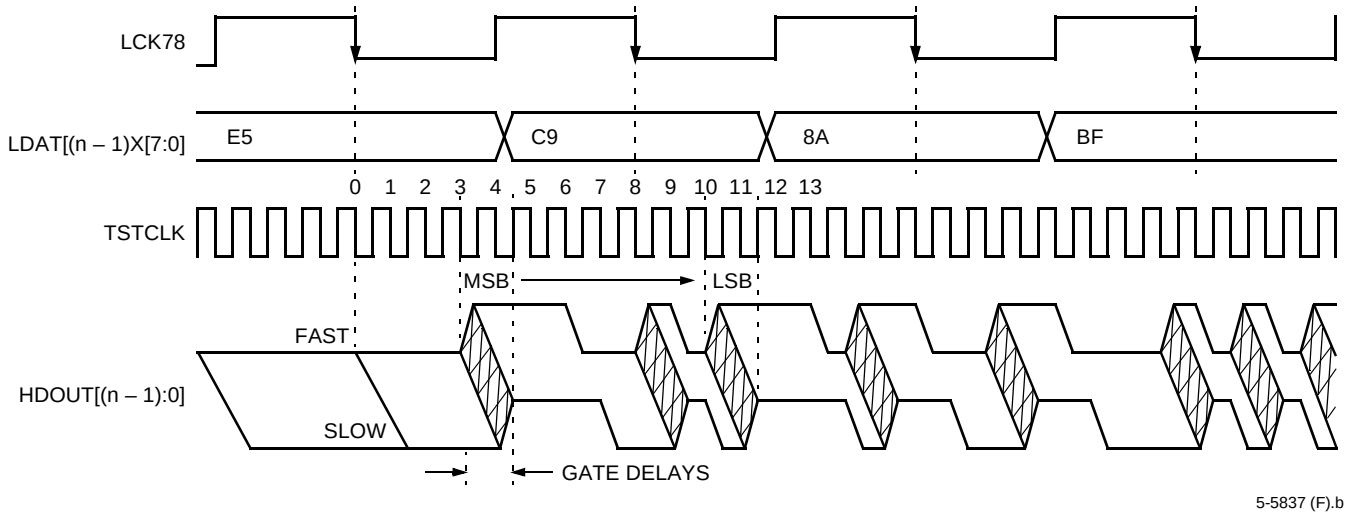
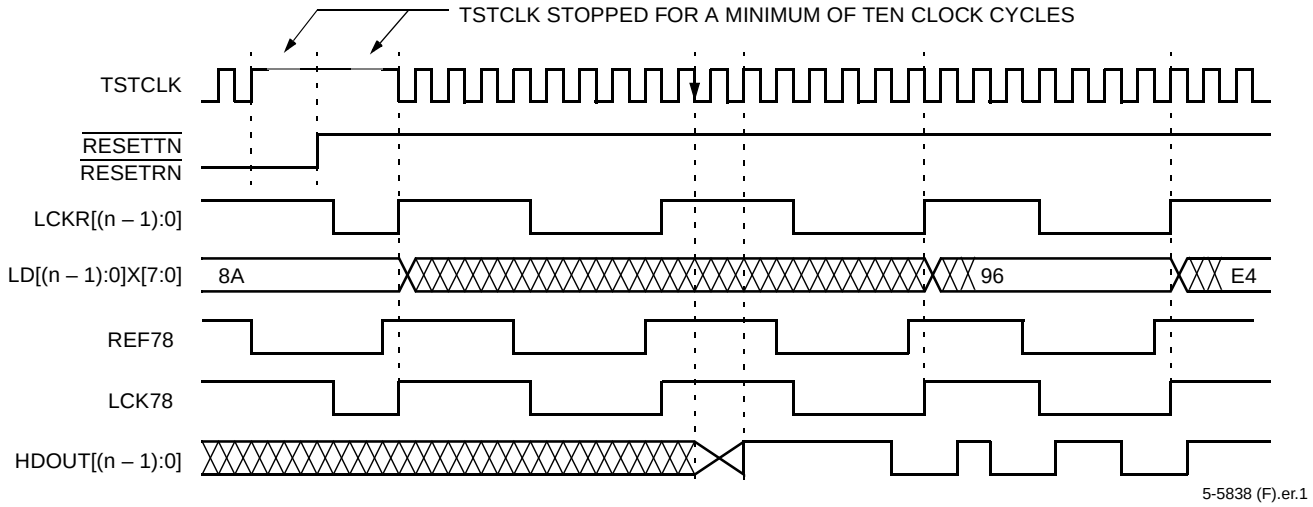


Figure 5. 622.08 Mbits/s Transmit (PLL Bypass Mode) Timing

Simulation Interface (continued)



Notes:
During PLL BYPASS mode, TSTCLK is asynchronous to the REF78 input of the CDRM622; therefore, test resets ($\overline{\text{RESETTN}}$ and $\overline{\text{RESETRN}}$) were added to allow establishing a relationship between the internally generated 77.76 MHz clocks and the reference clocks.

$\overline{\text{RESETRN}}$ allows synchronization of the 77.76 MHz recovered clocks in the receiver.

$\overline{\text{RESETTN}}$ allows synchronization of the 77.76 MHz clock internal to the transmitter.

TSTCLK should be stopped high while the resets change but needs to toggle at least four clock cycles while resets are active.

Figure 6. Synchronization of CDRM622 Generated Clocks During Bypass Mode

Test Interface

Table 3. System Test Signals

Signal Name	Type	Description
BSIPAD[(n – 1):0]	O	Provides buffered monitor points reflecting state of the 622.08 Mbits/s device input pads for use in boundary scan.
BSOPAD[(n – 1):0]	I	Provides access to 622.08 Mbits/s output pads for boundary scan. Output boundary-scan multiplexers are built into the macrocell.
BSCANEN	I	**(Active-High).** Enables boundary-scan values to control 622.08 MHz output device pins.
LOOPBKEN	I	**(Active-High).** Enables 622.08 Mbits/s loopback mode. All transmit outputs are directed into the receivers. Overrides individual channel loopback controls.
LOOPBKCH[(n – 1):0]	I	**(Active-High).** Enables 622.08 Mbits/s loopback mode on a per-channel basis.

Boundary Scan

In order to avoid loading the high-speed data signals unnecessarily, access has been provided through the macrocell. The state of the input pads can be monitored at buffered test outputs. The state of the output pads can be controlled through a multiplexer built into the macrocell data path.

Test Interface (continued)

High-Speed Loopback

The output of the transmitter can be looped back into the receiver. This feature enables factory testing 622 Mbits/s circuitry on a test set only capable of 200 MHz clocking. System product diagnostics may also find a use for this mode. The loopback function can be selected on a per-channel basis or by a global override.

Table 4. CDR Test Signals

Signal Name	Type	Description
TSTMODE	I	**(Active-High).** Enables CDR test mode.
TSTSHFTLD	I	**(Active-High).** Enables the test mode control register for shifting in selected tests by a serial port (EXDNUP). Serial stream setup is 18 bits long.
ECSEL	I	**(Active-High).** Enables external manual test control of 622.08 MHz clock phase selection through ETOGGLE and EXDNUP inputs.
ETOGGLE	I	**(Active +pulse).** Moves 622.08 MHz clock selection one phase per positive pulse >50 ns.
EXDNUP	I	Direction of phase change: 0 = down; 1 = up.
TSTPHASE	I	**(Active-High).** Controls bypass of 16 PLL-generated phases with 16 low-speed phases, generated by test logic.
TSTMUX[8:0]	O	Test mode output port. Can monitor recovered channel 77.76 Mbytes/s data byte and clock. Selection under control of test mode register.

CDR Testing

Built-in test cirtuitry is included as part of the macrocell in order to ensure quality of manufacture. Test access and control has been added to facilitate characterization and evaluation of the macrocell function. Macrocell testing is added by Lucent to verify PLL, high-speed data paths, and fault coverage within the macrocell.

One such test configures the macrocell in high-speed loopback with transmit pattern generation and receive byte alignment in order to observe 77.76 Mbytes/s data after passing through both transmitter and receiver at 622.08 Mbits/s. This test requires only the PLL reference clock to be sourced from the factory test set.

Also, each of the recovered channels (clock and data byte) can be brought out through the test port one channel at a time, and the synthesized clock, divided by eight, is brought out for frequency measurement and evaluation.

Macrocell testing is set up by an internal control register that is written through a 3-pin serial test interface.

Built-in testing cannot verify the 78 MHz interface connections to the device logic. Therefore, at least one test exercising the functional data path through the macrocell using PLL bypass is required from the device logic designers.

Test Access

In order to accomplish these tests, access is required to approximately 20 test signals through the device pins. Test pins can be multiplexed with other pins and TSTMODE = 1 can be used as an indication when CDR test access is needed. In addition, to standard manufacture testing, access to built-in test features has been useful during functional board-level prototype prove-in.

CDR testing requires access to the following signals **from the device pins**: TSTMODE, BYPASS, TSTCLK, RESETRN, RESETTN, TSTSHFTLD, ECSEL, EXDNUP, ETOGGLE, LOOPBKEN, TSTPHASE, TSTMUX[8:0].

REF78, MRESET, and HDIN[(n – 1):0] are also used during testing but are expected to be controllable through functional device pins. REF78 should be controllable through the reference clock input to the device. A 155 MHz reference clock pin which is divided on-chip to 78 MHz is acceptable. MRESET should be controllable through the device powerup reset pin.

Electrical and Timing Characteristics

Table 5. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Unit
Power Dissipation	16 channels at 3.3 V	—	—	1.25[1]	W

1. At 3.3 V, power is estimated by 300 mW + 50 mW per Rx channel + 10 mW per Tx channel.

Table 6. Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	—	3.135	—	3.465	V

Table 7. Receiver Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Input Data[1]					
Stream of Nontransitional 622 Mbits/s[2]	—	—	—	60	bits
Phase Change, Input Signal	Over a 200 ns time interval[3]	—	—	100	ps
Eye Opening[4]	—	0.4	—	—	UIp-p
Jitter Tolerance					
Jitter Tolerance:	—				
250 kHz		—	—	0.6	UIp-p
25 kHz		—	—	6	UIp-p
2 kHz		—	—	60	UIp-p

1. 622 Mbits/s scrambled data stream conforming to SONET STS-12 and SDH STM-4 data format using either a PN7 or PN9 sequence.
   - PN7 charateristic is $1 + x^6 + x^7$.
   - PN9 charateristic is $1 + x^4 + x^9$.
2. This sequence should not occur more than once per minute.
3. Translates to a frequency change of 500 ppm.
4. A unit interval for 622 Mbits/s data is 1.6075 ns.

Table 8. Transmitter Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Output Jitter, Generated	250 kHz to 5 MHz (measured with a spectrum analyzer)	—	—	0.2	UIp-p

Table 9. Synthesizer Specifications

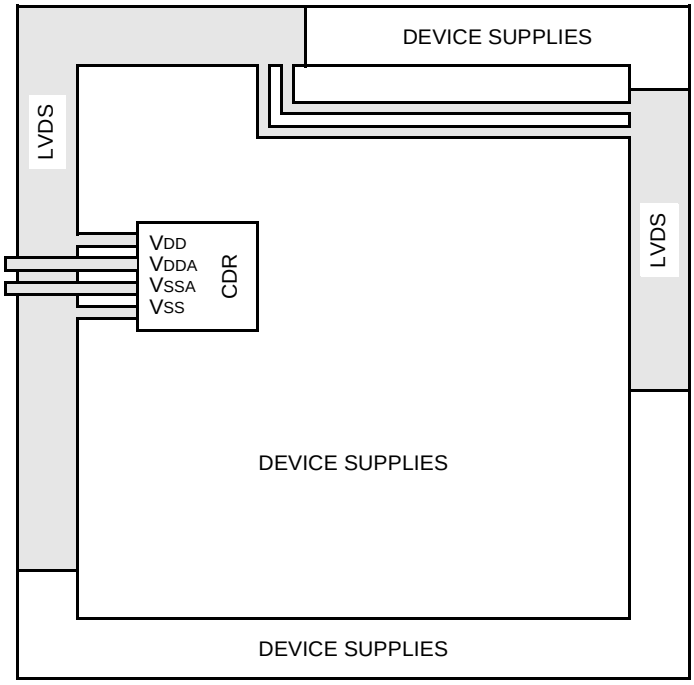
Parameter	Conditions	Min	Typ	Max	Unit
PLL[1]					
Loop Bandwidth	—	—	—	6	MHz
Jitter Peaking	—	—	—	2	dB
Powerup Reset Time	—	10	—	—	µs
Lock Aquisition Time	—	—	—	1	ms
Input Reference Clock					
Frequency	—	77.76	—	—	MHz
Frequency Deviation	—	—	—	±20	ppm
Phase Change	Over a 200 ns time interval[2]	—	—	100	ps

1. External 10 kΩ resistor to analog ground required.
2. Translates to a frequency change of 500 ppm.

Silicon Layout Considerations

MACROCELL ANALOG SUPPLIES:
ISOLATED TO THE CIRCUIT BOARD
<3 Ω

MACROCELL DIGITAL SUPPLIES:
TIED TO HIGH-SPEED I/O BUFFER SUPPLIES
ISOLATED FROM DEVICE SUPPLIES
<0.5 Ω

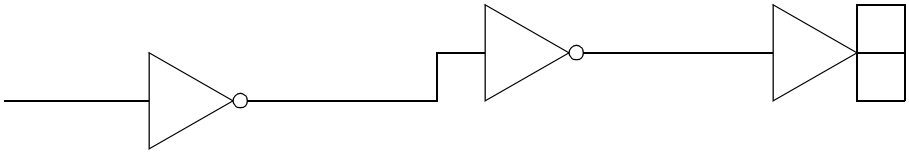


5-7715(F)r.1

Figure 7. Power Supply Connections

Integrity of Signal Transfer from the I/O Buffer

Figure 8 shows a repeater configuration recomended to ensure the integrity of the signal transfer from the I/O buffer to the macrocell.



5-7716(F)

Notes:
Use standard-cell SBIX16s as repeater buffers for 622 Mbits/s data (in pairs).

Power supplies should be tied to the high-speed I/O buffer and the digital macrocell source.

Routing: 1 µm wide and 4 µm spacing.

Remain in one metal level as much as is reasonable. Use double contact windows when changing levels.

Repeaters can drive up to 2000 µm.

Evenly distribute load on repeaters (approximately).

Transmitter can drive up to 2000 µm.

LVDS receivers can drive up to 2000 µm.

Figure 8. 622 Mbits/s Repeater Recomendations

Notes

For additional information, contact your Microelectronics Group Account Manager or the following:

INTERNET: **http://www.lucent.com/micro**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18103
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road, Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468**, **ext. 316**, FAX (86) 21 6440 0652
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 7000 582 368** , FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 4354 2800** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

June 1999
DS99-153NTBB

microelectronics group

Lucent Technologies
Bell Labs Innovations