HEWLETT PACKARD

High Speed Optocouplers

Technical Data

CNW135
CNW136
CNW4502
New **CNW4503**

Features

- **5000 Vrms/1 Minute Insulation Withstand Capability**
- **Worldwide Safety Approval**
  - UL1577 (File No. E55361)
  - VDE 0884 Certification (V_{IORM} = 1 kV_{RMS})
  - VDE 860/805/806/804/750-1/IEC950
  - BSI according to BS 415/7002/6301
  - SETI-SEMKO-NEMKO DEMKO according to IEC 65/380/950/335
- **High Speed: 1 Mbit/s**
- **TTL Compatible**
- **Performance Guaranteed over Temperature 0°C to 70°C**
- **Pin Compatible with 6N135/6 and HCPL-4502/3**
- **Very High Common Mode Rejection for CNW4503**
- **Line Receivers (15 K V/μs Common Mode Transient Immunity and Low Input-Output Capacitance of 0.6 pF)**
- **Analog Signal Ground Isolation (Integrated Photon Detector Provides Improved Linearity over Phototransistor Type)**
- **Feedback Element in Switched Mode Power Supplies**
- **High Speed Logic Ground Isolation – TTL/TTL, TTL/CMOS, TTL/LSTTL**
- **Power Transistors Isolation in Motor Drives**
- **Replaces Pulse Transformers**
- **Replaces Slow Photo-Transistor Isolators (Pins 2-7 of the CNW135/6 Conforms to Pins 1-6 of 6 Pin Phototransistor Couplers. Pin 8 can be Tied to any Available BiasVoltage of 1.5 V to 30 V for High Speed Operation)**

Applications

- **High Voltage Insulation**
- **Video Signal Isolation**

Description

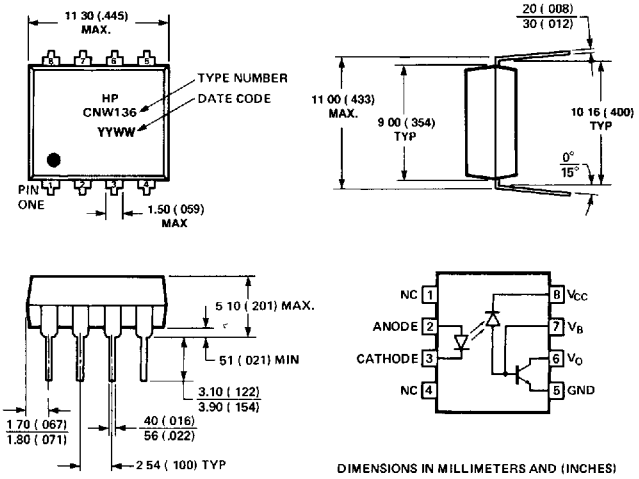
These devices are high voltage and fast switching optocouplers consisting of an AlGaAs LED and a silicon photodetector. A wide body encapsulation is used to provide creepage and clearance dimensions suitable for safety approval by regulatory agencies worldwide.

The CNW135 is for use in TTL/CMOS, TTL/LSTTL or wide bandwidth analog applications.

Current transfer ratio (CTR) for the CNW135 is 7% minimum at I_F = 16 mA.

OPTO COUPLERS

Package Outline



DIMENSIONS IN MILLIMETERS AND (INCHES)

The CNW136 is designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6K pullup resistor. CTR of the CNW136 is 19% minimum at I_F = 16 mA. Selection for higher CTR is available.

The CNW4502/3 provides the electrical and switching performance of the CNW136, increased ESD protection and increased transient immunity.

Regulatory Information

These products feature a wide body 8 PIN DIP. This package was specifically designed to meet regulatory requirements worldwide. The CNW135/6 and CNW4502/3* have been approved by the following organizations:

UL – Covered under UL component recognition FILE E55361

VDE – Approved according to VDE 0884 (marks License No. 70975)
Complies for reinforced insulation at 250 V AC with:
DIN IEC 380/VDE 0806
DIN IEC 435/VDE 0805 "ENTWURF"
DIN 57804/VDE 0804 (isolation group C)
DIN VDE 0860 (HD 195 S6)
DIN IEC 601 Teil 1/VDE 0750-1
DIN VDE 0160
EN 60950/IEC950

NORDIC – Tested for applications (reinforced insulation) – Class II applications for plugable apparatus in normal tight execution.
-SETI-SEMKO-NEMKO-DEMKO-According to IEC 65-IEC380-IEC950-IEC335

BSI – Certification according to BS415:1990, BS7002:1989 and BS6301: 1982 for class II applications.

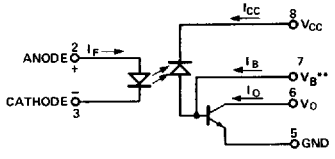
*Pending SETI and SEMKO approval

Absolute Maximum Ratings

Storage Temperature	-55°C to +125°C
Operating Temperature	-55°C to 85°C
Lead Solder Temperature	260°C for 10s (up to seating plane)
Average Input Current – I_F	100 mA
Peak Transient Input Current – I_F	1.0 A (≤1 µs pulse width, 300 Hz)
Reverse Input Voltage – V_R (Pin 3-2)	5 V
Input Power Dissipation (up to 70°C)	250 mW*
Average Output Current – I_O (Pin 6)	10 mA
Emitter-Base Reverse Voltage (Pin 5-7)	5 V
Output Voltage – V_O (Pin 6-5)	-0.5 V to 20 V
Supply Voltage – V_{CC} (Pin 8-5)	-0.5 V to 30 V
Base Current – I_B (Pin 7, except HCPL-4502/3)	5 mA
Output Power Dissipation	100 mW

*Derate at 5.0 mW/°C for operating temperatures above 70°C.

Schematic



**Note: For CNW4502/3, Pin 7 is not connected.

CAUTION: The small junction sizes inherent to the design of this bipolar component increases the component's susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assemby of this component to prevent damage and/or degradation which may be induced by ESD.

VDE 0884 Insulation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0109/12.83, Table 1 for rated mains voltage ≤ 600 V_{RMS} for rated mains voltage ≤ 1000 V_{RMS}		 I-IV I-III	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0109/12.83)		2	
Maximum Working Insulation Voltage	V_{IORM}	1414	V_{PEAK}
		1000	V_{RMS}
Input to Output Test Voltage, Method b* V_{PR} = 1.6 x V_{IORM}, 100% Production Test with tp = 1 sec, Partial Discharge < 5 pC	V_{PR}	2263	V_{PEAK}
		1600	V_{RMS}
Input to Output Test Voltage, Method a* V_{PR} = 1.2 x V_{IORM}, Type and sample test, tp = 60 sec, Partial Discharge < 5 pC	V_{PR}	1697	V_{PEAK}
		1200	V_{RMS}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}	8000	V_{PEAK}
Safety-Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9) Case Temperature Current (Input Current I_F, P_{SI} = 0) Output Power (obtained by setting pin 8 = 5.5 V, pins 7, 6, 5 = ground)	 T_{SI} I_{SI} $P_{SI, OUTPUT}$	 150 400 700	 °C mA mW
Insulation Resistance at T_{SI}, V_{IO} = 500 V V_{IO} = 500 V	R_{IS}	≥ 10^9	Ω

*Refer to the front of the optocoupler section of the HP Optoelectronics Designer's Catalog, under Product Safety Regulations Section, (VDE 0884) for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in the application.

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Clearance (External Air Gap)	L(IO1)	9.6	mm	Measured from input terminals to output terminals
Min. External Creepage (External Tracking Path)	L(IO2)	10.0	mm	Measured from input terminals to output terminals
Min. Internal Clearance (Internal Plastic Gap)		1.0	mm	Through insulation distance conductor to conductor
Min. Internal Creepage (Internal Tracking Path)		4.0	mm	Measured from input terminals to output terminals
Comparative Tracking Index	CTI	200	volts	DIN IEC 112/VDE 0303 PART 1
Isolation Group (per DIN VDE 0109)		IIIa		Material group (DIN VDE 0109)

Electrical Specifications

Over Recommended Temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 8.)

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	CNW135	7	18	150	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	1
			5				V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
		CNW136 CNW4502 CNW4503	19	50	150	%	T_A = 25°C, V_O = 0.4 V, I_F = 16 mA, V_{CC} = 4.5 V		
			15				V_O = 0.5 V, I_F = 16 mA, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	CNW135		0.1	0.4	V	T_A = 25°C, I_O = 1.1 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 0.8 mA, I_F = 16 mA, V_{CC} = 4.5 V		
		CNW136 CNW4502 CNW4503		0.1	0.4	V	T_A = 25°C, I_O = 3.0 mA, I_F = 16 mA, V_{CC} = 4.5 V		
					0.5		I_O = 2.4 mA, I_F = 16 mA, V_{CC} = 4.5 V		
Logic High Output Current	I_{OH}			0.002	0.5	µA	T_A = 25°C, V_O = V_{CC} = 5.5 V, I_F = 0 mA	6	
					1		T_A = 25°C, V_O = V_{CC} = 15 V, I_F = 0 mA		
					50				
Logic Low Supply Current	I_{CCL}			70	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V		
Logic High Supply Current	I_{CCH}				1	µA	T_A = 25°C, I_F = 0 mA, V_O = Open, V_{CC} = 15 V		
					2				
Input Forward Voltage	V_F		1.45	1.68	1.85	V	T_A = 25°C, I_F = 16 mA	3	
			1.35		1.95				
Input Reverse Breakdown Voltage	BV_R		5			V	I_R = 10 µA, T_A = 25°C		
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$			1.9		mV/°C	I_F = 16 mA		
Input Capacitance	C_{IN}			90		pF	f = 1 MHz, V_F = 0 V		
Input-Output Insulation Voltage	V_{ISO}		5000			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C		2, 7
Resistance (Input-Output)	R_{I-O}		10^{12}	10^{13}		Ω	T_A = 25°C, V_{I-O} = 500 VDC		2
			10^{11}				T_A = 100°C, V_{I-O} = 500 VDC		
Capacitance (Input-Output)	C_{I-O}			0.5	0.6	pF	f = 1 MHz		2
Transistor DC Current Gain	h_{FE}			180			V_O = 5 V, I_O = 3 mA		
				160			V_O = 0.4 V, I_B = 40 µA		

*All typicals at T_A = 25°C.

Switching Specifications

Over Recommended Temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, I_F = 16 mA, unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	CNW135		0.2	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 8, 11	4, 5
					2.0					
		CNW136 CNW4502		0.2	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Propagation Delay Time to Logic High at Output	t_{PLH}	CNW135		0.6	1.5	µs	T_A = 25°C	R_L = 4.1 kΩ	5, 8, 11	4, 5
					2.0					
		CNW136 CNW4502		0.35	0.8		T_A = 25°C	R_L = 1.9 kΩ		
					1.0					
Common Mode Transient Immunity at Logic High Level Output	$\|CM_H\|$	CNW135	1,000			V/µs	R_L = 4.1 kΩ	I_F = 0 mA, T_A = 25°C, V_{CM} = 10 V	12	3, 4, 5
		CNW136	1,000				R_L = 1.9 kΩ			
		CNW4502	1,000	≥10,000			V_{CM} = 10 V	I_F = 0 mA, T_A = 25°C, R_L = 1.9 kΩ	12	3, 4
		CNW4503	15,000	30,000			V_{CM} = 1500 V			
Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$	CNW135	1,000			V/µs	R_L = 4.1 kΩ	I_F = 16 mA, T_A = 25°C, V_{CM} = 10 V	12	3, 4, 5
		CNW136	1,000				R_L = 1.9 kΩ			
		CNW4502	1,000	10,000			V_{CM} = 10 V	I_F = 16 mA, T_A = 25°C, R_L = 1.9 kΩ	12	3, 4
		CNW4503	15,000	30,000			V_{CM} = 1500 V			
Bandwidth	BW	CNW135 CNW136		11		MHz	See Test Circuit		7, 10	6

*All typicals are at T_A = 25°C.

Notes:

1. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
3. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse V_{CM}, to assure that the output will remain in a Logic High state (i.e. V_O > 2.0 V) Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM} dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e. V_O > 0.8 V).
4. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
5. The 4.1 kΩ load represents 1 LSTTL unit load of 0.36 mA and 6.1 kΩ pull-up resistor.
6. The frequency at which the ac output voltage is 3 dB below the low frequency asymptote.
7. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage of ≥ 6000 Vrms for one second (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% Production test shown in the VDE 0884 Insulation Characteristics Table.
8. Use of a 0.1 µf bypass capacitor connected between pins 5 and 8 is recommended for operation.

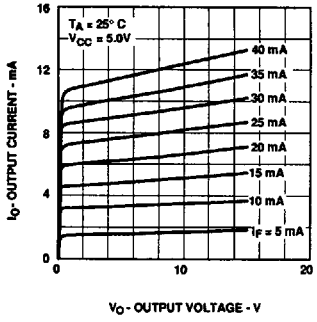


Figure 1. DC and Pulsed Transfer Characteristics.

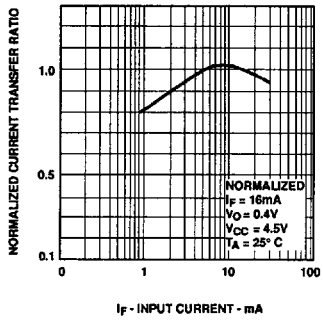


Figure 2. Current Transfer Ratio vs. Input Current

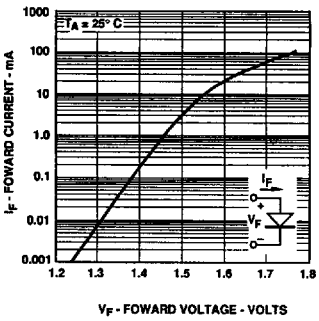


Figure 3. Input Current vs. Forward Voltage.

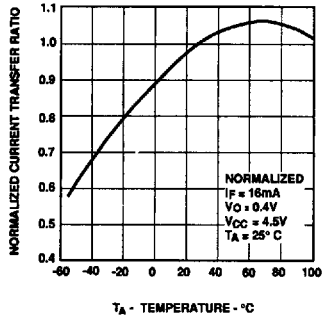


Figure 4. Current Transfer Ratio vs. Temperature.

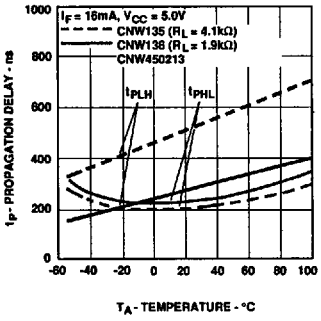


Figure 5. Propagation Delay vs. Temperature.

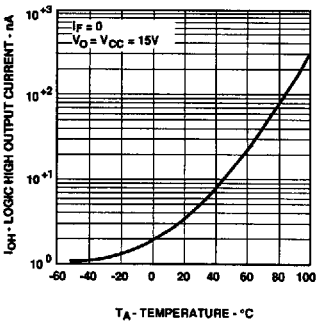


Figure 6. Logic High Output Current vs. Temperature.

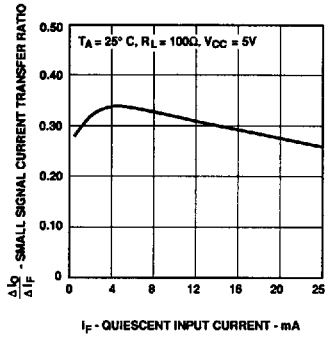


Figure 7. Small-Signal Current Transfer Ratio vs. Quiescent Input Current.

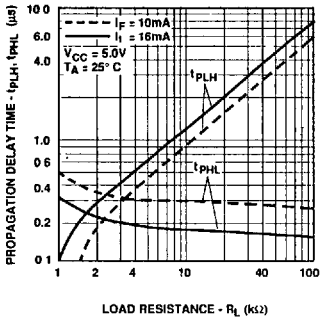


Figure 8. Propagation Delay Time vs. Load Resistance.

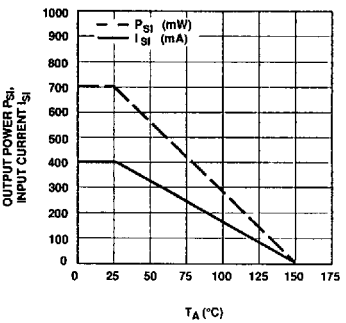


Figure 9. Dependence of Safety Maximum Ratings with Ambient Temperature.

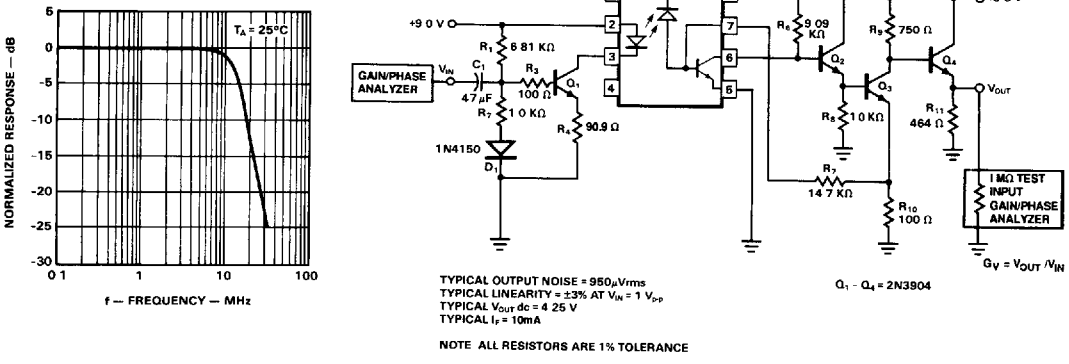


Figure 10. Frequency Response. (CNW135/6)

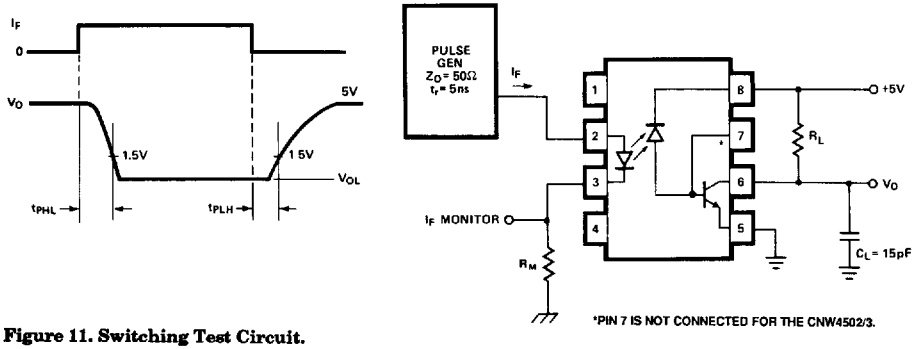


Figure 11. Switching Test Circuit.

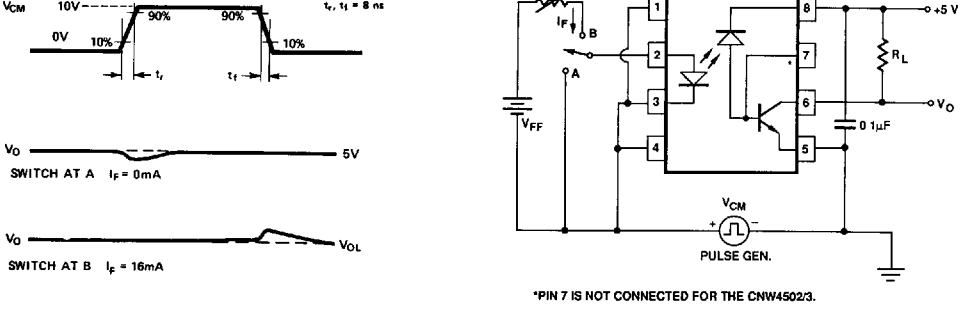


Figure 12. Test Circuit for Transient Immunity and Typical Waveforms.

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