
Low Cost, Industry Standard FDDI MIC Transceivers

Technical Data

**HFBR-5111 (2x11)
HFBR-5112 (Narrow 1x13)
HFBR-5113 (Standard 1x13)**

Features

- Full Compliance with the FDDI PMD Standard
- Full Compliance with the Optical Performance Requirements of the ATM 100 Mbps Physical Layer
- Full Compliance with the Optical Performance Requirements of the Fast Ethernet Physical Layer
- Multisourced Package Style with:
 - 2x11 or 1x13 Pin Configuration
 - MIC Receptacle
 - Field Changeable Keying
- Wave Solder and Aqueous Wash Process Compatible Package
- Internal Shielding for Low EMI Emissions and High EMI Immunity
- Single +5V Power Supply
- Shifted ECL Logic Interface Directly Compatible with FDDI PHY Circuits
- Manufactured in an ISO 9001 Certified Facility

Applications

- FDDI Concentrators, Bridges, Routers, and Network Interface Cards
- 100 Mbps ATM Interfaces
- Fast Ethernet Interfaces

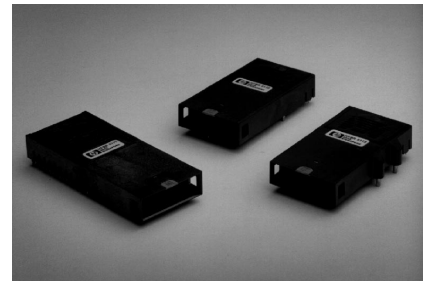
- Point-to-Point Data Communications
- Replaces DLX2012-FD and DLX2020-FD Model Transceivers

Description

The HFBR-511X family of transceivers from Hewlett-Packard consists of high performance, cost effective modules for optical data communication applications at the 100 Mbps/125 MBd rate.

The transceivers feature full compliance with the Fiber Distributed Data Interface (FDDI) Physical Media Dependent (PMD) standard. This standard has been approved as an International Standard, ISO/IEC 9314-3, and an American National Standard, ANSI X3.166 - 1990. The HFBR-5111 represents the 2x11 package style. The "2x11" denotes two rows of eleven pins. The HFBR-5112 and HFBR-5113 represent the Narrow and Standard 1x13 package styles, respectively. The "1x13" denotes one row of thirteen pins.

The modules are designed for 50 or 62.5 μm core multimode optical fiber and operate at a nominal wavelength of 1300 nm. Each transceiver incorporates



our high-performance, reliable, long-wavelength optical devices and proven circuit technology to give long life and consistent performance.

The transceivers are optimized for 125 MBd operation but can be used over a wide range of signal rates. The transceivers are guaranteed to meet FDDI PMD specifications when used within the operating conditions specified in this document.

These HFBR-511X Series transceivers are also useful for both ATM 100 Mbps interfaces and Fast Ethernet 100 Base-FX interfaces. The ATM Forum User-Network Interface (UNI) Standard, Version 3.0, defines the Physical Layer for 100 Mbps Multimode Fiber Interface for ATM in Section 2.3 to be the

FDDI PMD standard. Likewise, the Fast Ethernet Alliance defines the Physical Layer for the 100 Base-FX Version of IEEE 802.3u to be the FDDI PMD standard.

Hewlett-Packard also provides several other FDDI products compliant with the FDDI Low Cost Fiber (LCF) -PMD and Single Mode (SM) -PMD standards. These products are available with ST, SC, and FC connector styles. They are available in the 1x9 transceiver and 14- and 16-pin transmitter/receiver package styles for those designs that require these alternate configurations. Contact your Hewlett-Packard sales representative for information on these alternative FDDI products.

Transmitter Section

The transmitter section of the HFBR-511X Series utilizes a 1300 nm surface emitting InGaAsP LED. The LED is packaged in the optical subassembly portion of the transmitter section. It is decoupled to a custom IC which converts differential-input, PECL logic signals, ECL referenced (shifted) to a +5 V power supply, into an analog LED drive current.

Receiver Section

The receiver section of the HFBR-511X Series utilizes an InGaAs PIN photodiode coupled to a custom silicon transimpedance preamplifier IC. They are packaged in the optical subassembly portion of the receiver.

The PIN/preamplifier combination is ac-coupled to a custom quantizer IC which provides the final pulse shaping for the logic output and the Signal Detect function. Both the Data and Signal Detect outputs are

differential. Also, both Data and Signal Detect outputs are PECL compatible, ECL referenced (shifted) to a +5 V power supply.

Package

The overall package concept for the HP transceiver consists of the following basic elements: two optical subassemblies, an electrical subassembly, and the housing with full compliance to the FDDI PMD standard. A block diagram is illustrated in Figure 1.

The package outline drawings and pin-outs are shown in Figures 2 and 3. These are compliant with the industry standard 2x11 and 1x13 pin configurations.

The optical subassemblies utilize a high-volume assembly process together with low-cost lens elements which result in a cost-effective building block.

The electrical subassemblies consist of a high-volume, multi-layer printed circuit board on which the IC chips and various surface-mounted passive circuit elements are attached.

Each transceiver package includes internal shields for the electrical and optical subassemblies to ensure low EMI emissions and high immunity to external EMI fields.

The outer housings including the MIC receptacles are molded of filled non-conductive plastic to provide mechanical strength and electrical isolation. The solder posts of each package design are isolated from the circuit design of the transceiver and do not require connection to a ground plane on the circuit board.

Each transceiver is attached to its printed circuit boards with the 2x11 or 1x13 signal pins and the solder posts which exit the bottom of the housing. The solder posts provide the primary mechanical strength to withstand the loads imposed on the transceiver when mating with MIC-connected fiber cables.

Application Information

The Applications Engineering group of the Optical Communication Division is available to assist you with the technical under

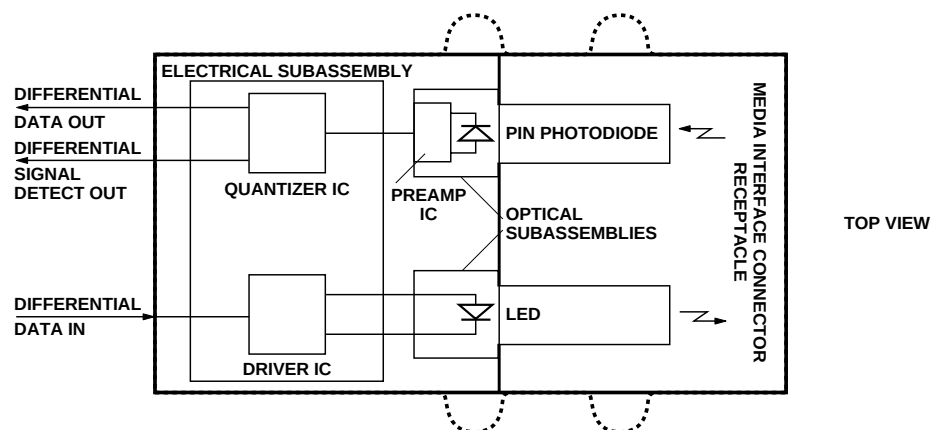


Figure 1. HFBR-5111/-5112/-5113 Block Diagram.

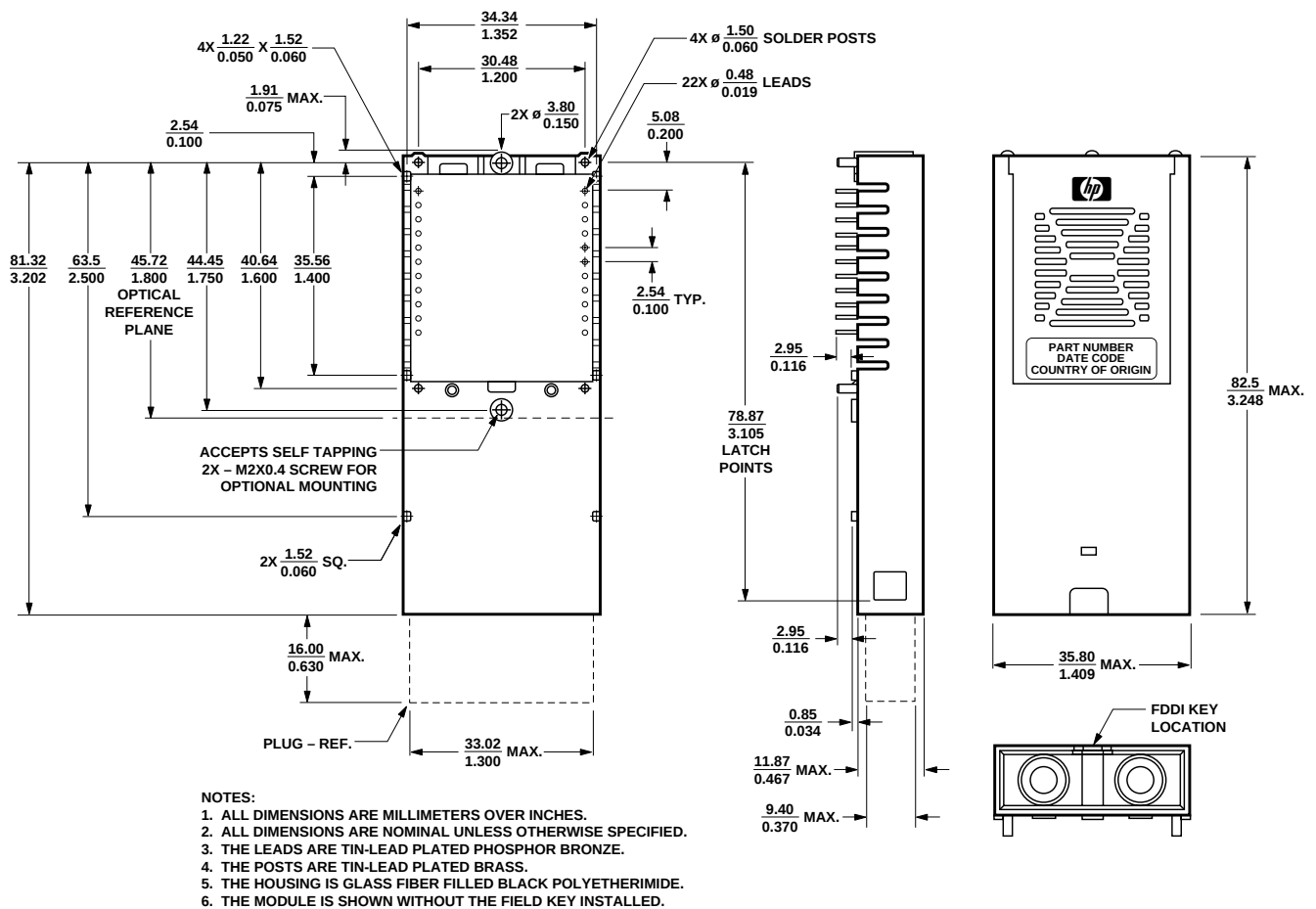


Figure 2(a). HFBR-5111 Outline Drawing.

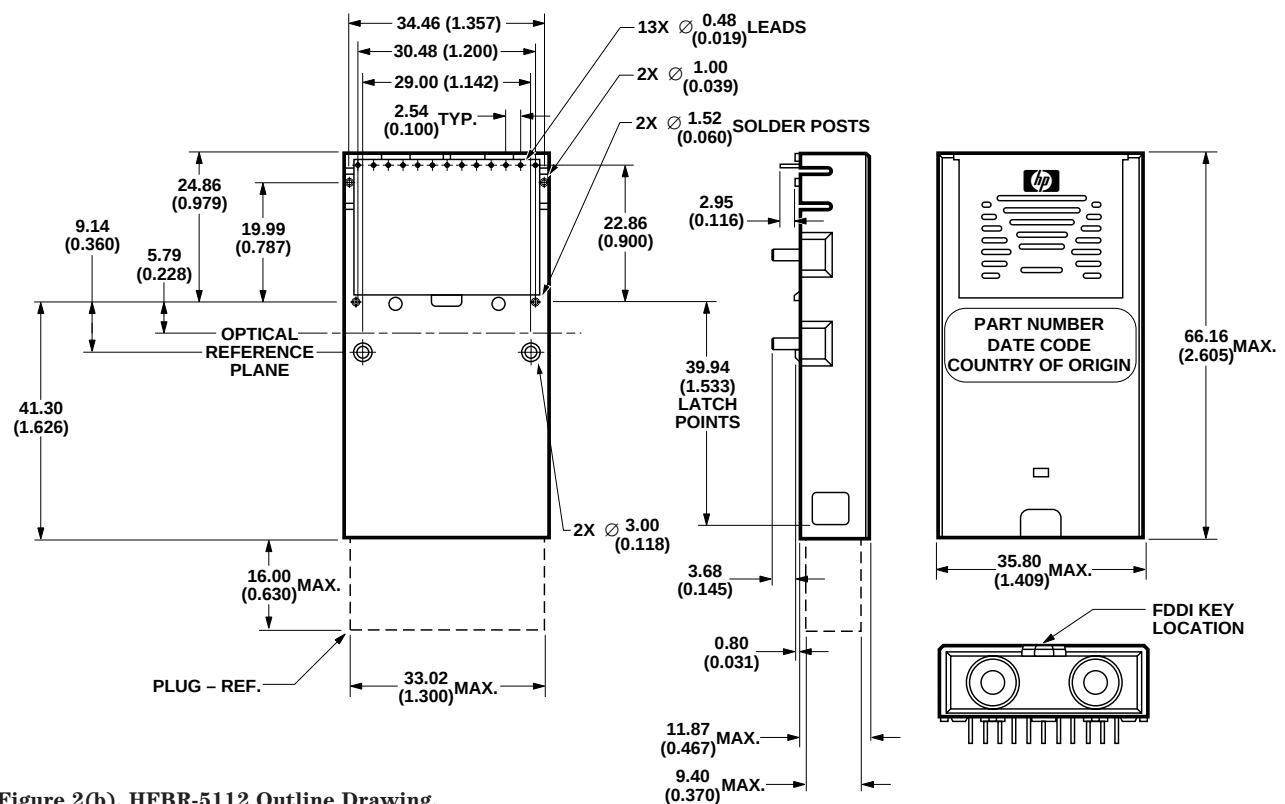


Figure 2(b). HFBR-5112 Outline Drawing.

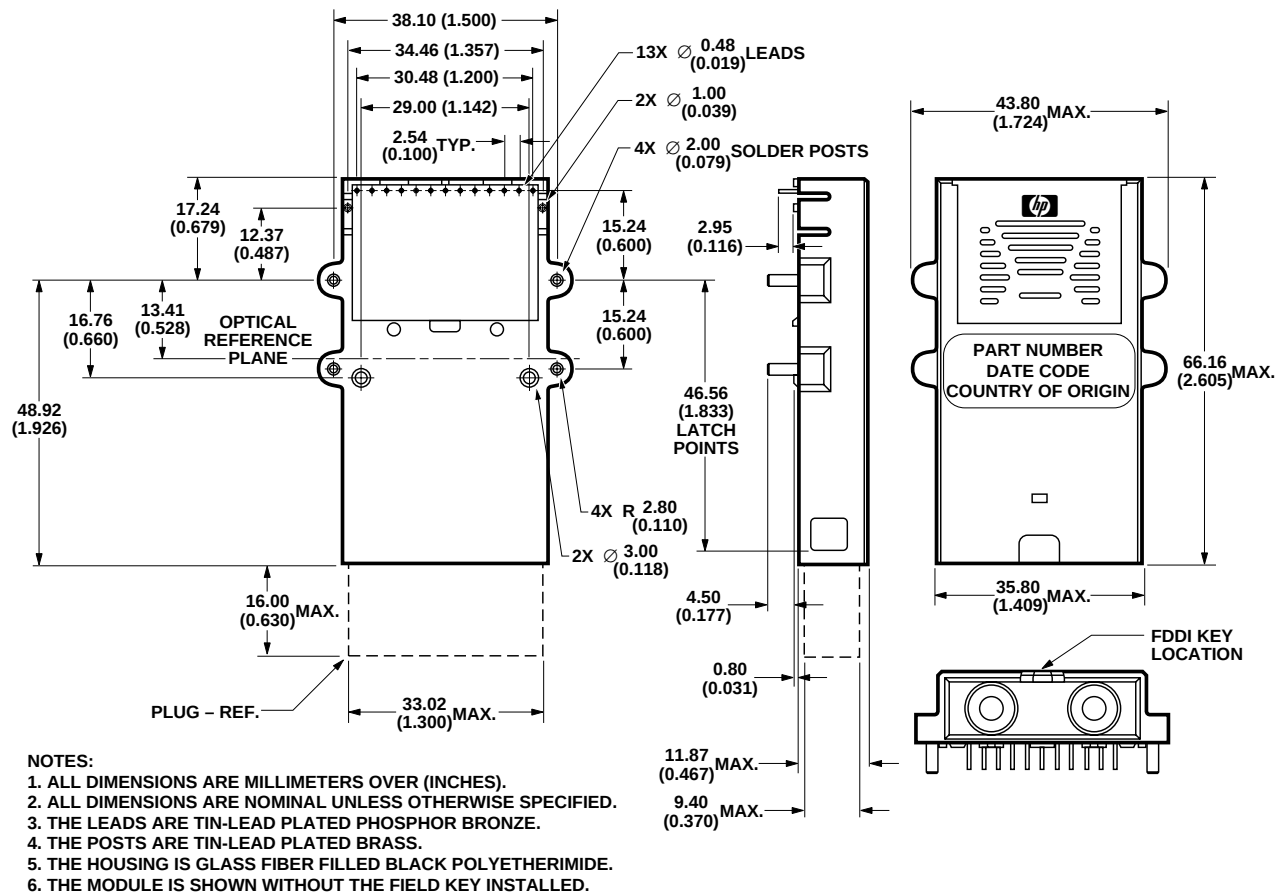


Figure 2(c). HFBR-5113 Outline Drawing.

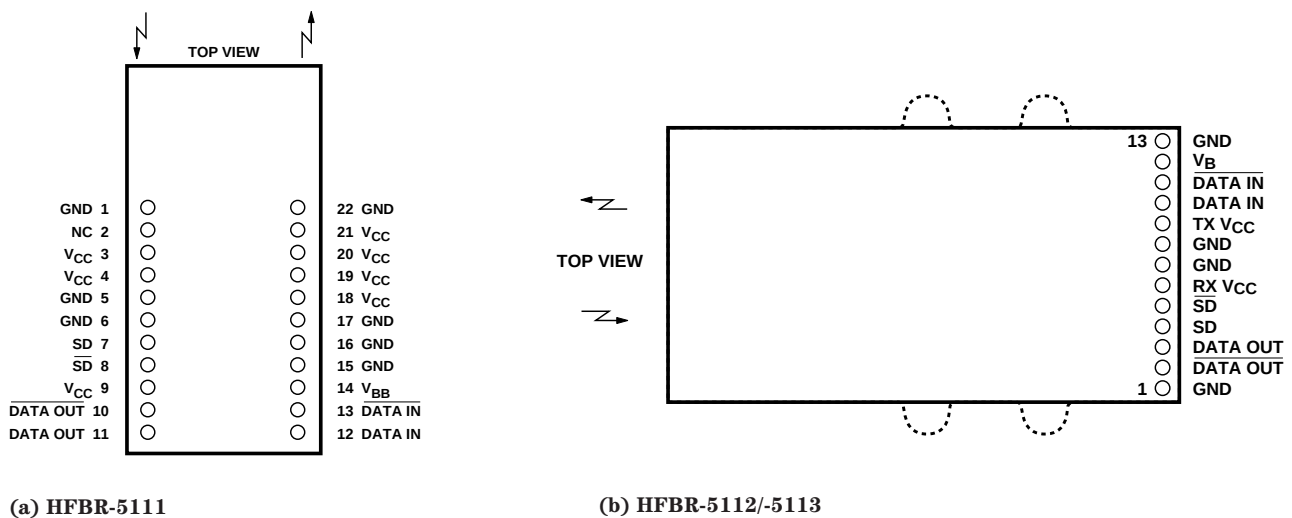


Figure 3. Pin Assignments.

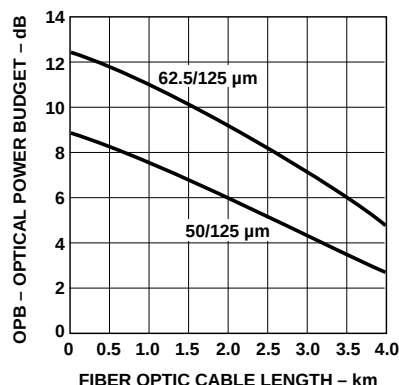


Figure 4. Optical Power Budget at BOL vs. Fiber Optic Cable Length.

standing and design trade-offs associated with this transceiver. You can contact them through your Hewlett-Packard sales representative.

The following information is provided to answer some of the most common questions about the use of these parts.

Transceiver Optical Power Budget versus Link Length

The Optical Power Budget (OPB) is the available optical power for a fiber-optic link to accommodate fiber cable losses plus losses due to in-line connectors, splices, optical switches, and to provide margin for link aging and unplanned losses due to cable plant reconfiguration or repair.

Figure 4 illustrates the predicted OPB associated with the transceivers specified in this data sheet at the Beginning of Life (BOL). This curve represents the attenuation and chromatic plus modal dispersion losses associated with the 62.5/125 μm and 50/125 μm fiber cables only. The area under the curve represents the remaining OPB at any link length, which is available for overcoming non-fiber cable related losses.

Hewlett-Packard LED technology has produced 1300 nm LED devices with lower aging characteristics than normally associated with these technologies in the industry. The industry convention is 1.5 dB aging for 1300 nm LEDs, however HP 1300 nm LEDs will experience less than 1 dB of aging over normal commercial equipment mission life periods. Contact your Hewlett-Packard sales representative for additional details.

Figure 4 was generated with a Hewlett-Packard fiber-optic link model containing the current industry conventions for fiber cable specifications and the FDDI PMD optical parameters. These parameters are reflected in the guaranteed performance of the transceiver specifications in this data sheet. This same model has been used extensively in the ANSI and IEEE committees, including the ANSI X3T9.5 committee, to establish the optical performance requirements for various fiber-optic interface standards. The cable parameters used come from the ISO/IEC JTC1/SC 25/WG3 Generic Cabling for Customer Premises per DIS 11801 document and the EIA/TIA-568-A Commercial Building Telecommunications Cabling Standard per SP-2840.

Transceiver Signaling Operating Rate Range and BER Performance

For purposes of definition, the symbol rate (Baud), also called signaling rate, is the reciprocal of the symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).

When used in FDDI 100 Mbps applications, the performance of the 1300 nm transceivers is guaranteed over the signaling rate of 10 MBd to 125 MBd to the full conditions listed in the individual product specification tables.

The transceivers may be used for other applications at signaling rates outside of the 10 MBd to 125 MBd range with some penalty in the link optical power budget primarily caused by a reduction of receiver sensitivity. Figure 5 gives an indication of the typical performance of these 1300 nm products at different rates.

These transceivers can also be used for applications which require different bit error rate (BER) performance. Figure 6 illustrates the typical trade-off between link BER and the receiver's input optical power level.

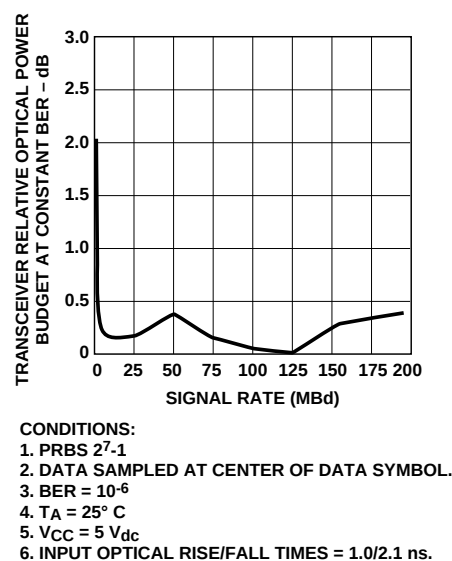


Figure 5. Transceiver Relative Optical Power Budget at Constant BER vs. Signaling Rate.

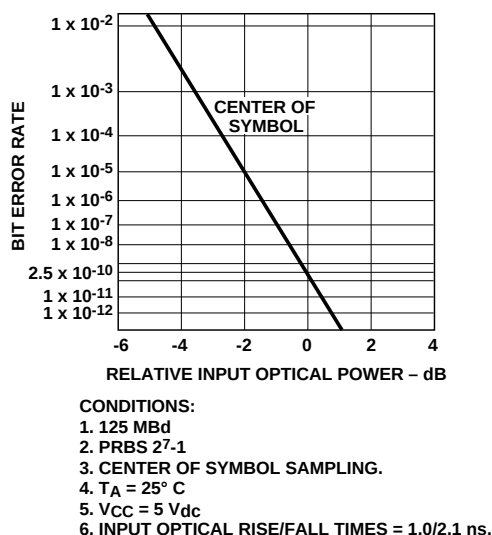


Figure 6. Bit Error Rate vs. Relative Receiver Input Optical Power.

Transceiver Jitter Performance

The Hewlett-Packard 1300 nm transceivers are designed to operate per the system jitter allocations stated in Table E1 of Annex E of the FDDI PMD standard.

The HP 1300 nm transmitters will tolerate the worst-case input electrical jitter allowed in the table without violating the worst-case output optical jitter requirement of Sections 8.1 Active Output Interface of the FDDI PMD standard.

The HP 1300 nm receivers will tolerate the worst-case input optical jitter allowed in Section 8.2 Active Input Interface of the FDDI PMD standard without violating the worst-case output electrical jitter allowed in the Table E1 of the Annex E.

The jitter specifications stated in the following 1300 nm transceiver specification table are derived from the values in Table

E1 of Annex E. They represent the worst-case jitter contribution that the transceivers are allowed to make to the overall system jitter without violating the Annex E allocation example. In practice, the typical contribution of the HP transceiver is well below the maximum amount.

Recommended Handling Precautions

It is advised that normal static precautions be taken in the handling and assembly of these transceivers to prevent damage which may be induced by electrostatic discharge (ESD). The HFBR-511X Series meets MIL-STD-883C Method 3015.4 Class 2.

Care should be taken to avoid shorting the receiver Data or Signal Detect outputs directly to ground without proper current-limiting impedance.

Solder and Wash Process Compatibility

Each transceiver is delivered with a protective port plug inserted into the MIC receptacle. This port process plug protects the optical subassembly during wave solder and aqueous wash processing and acts as a dust cover during shipping. The port process plugs have been tested up to and found to withstand 110 psi and 190°F.

These transceivers are compatible with either industry standard wave- or hand-solder processes.

Shipping Container

Each transceiver is packaged in a shipping container designed to protect it from mechanical and ESD damage during shipment or storage.

Board Layout—Decoupling Circuit and Ground Planes

It is important to take care in the layout of your circuit board to achieve optimum performance from these transceivers. Figure 7 provides a good example of schematics for decoupling circuits that work well with this product. It is further recommended that a contiguous ground plane be provided in the circuit board directly under the transceiver to provide a low inductance ground for signal return current. This recommendation is in keeping with good high frequency board layout practices.

Board Layout—Hole Pattern

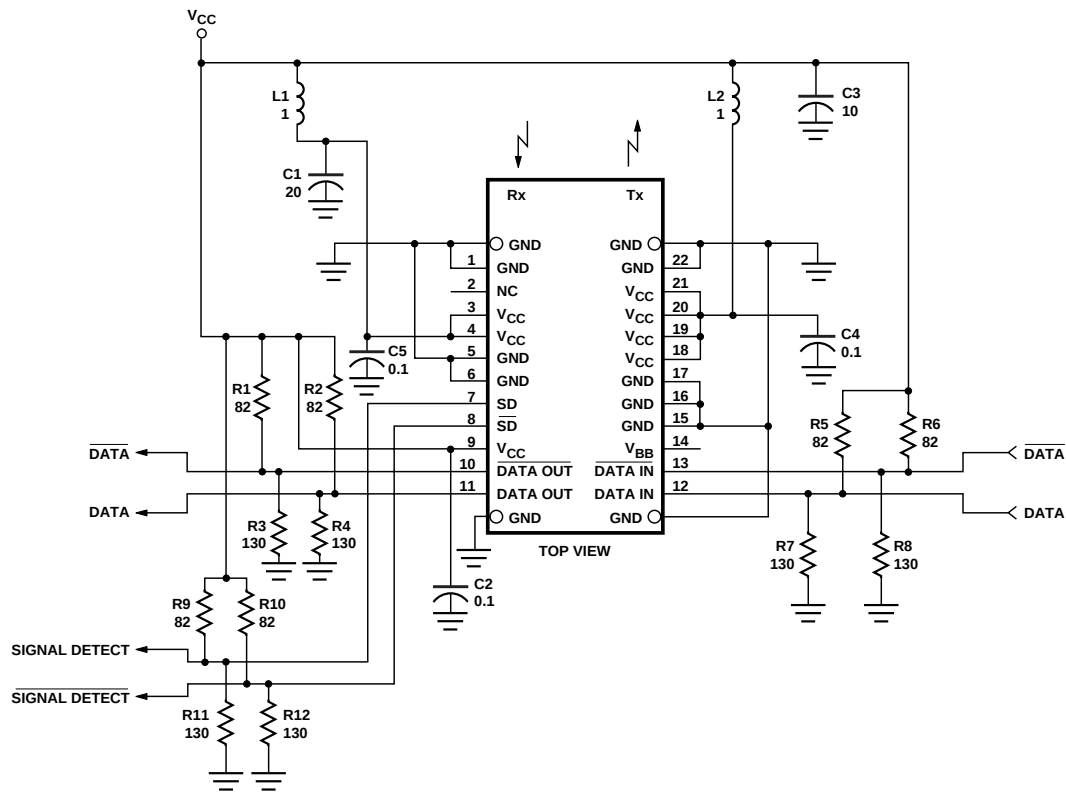
The hole pattern shown in Figure 8 for the 2x11 package style complies with the pin sizes specified by the multisource agreement. Hole patterns are also provided for the Standard and Narrow 1x13 package styles. These drawings can be used as a guide in the mechanical layout of your circuit board.

Board Layout—Art Work

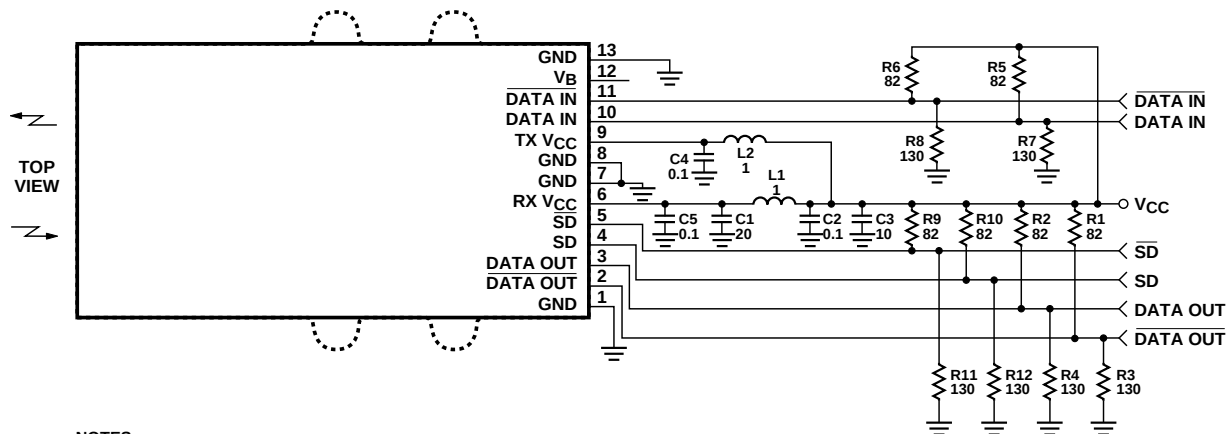
The Applications Engineering group has developed Gerber file artwork for various fiber optic transceiver layouts. Contact your local Hewlett-Packard sales representative for details.

Regulatory Compliance

These transceiver products are intended to enable commercial system designers to develop equipment that complies with the various international regulations governing certification of Information Technology Equipment. See Table 1 for details. Additional information is available from your Hewlett-Packard sales representative.



(a) HFBR-5111

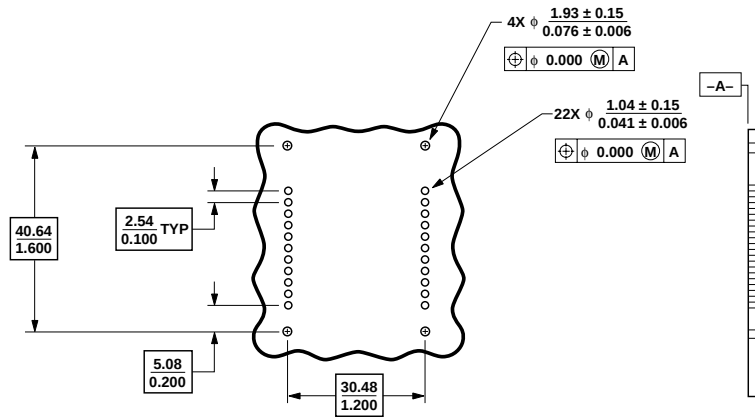


NOTES:

1. PLACE TERMINATION RESISTORS NEAR INPUT DATA PINS OF TRANSCEIVER AND PHY DEVICES.
2. MAKE DIFFERENTIAL SIGNAL PATHS SHORT AND OF THE SAME LENGTH WITH EQUAL TERMINATIONS TO $V_{CC} - 2$ VOLTS.
3. SIGNAL TRACES SHOULD BE 50Ω TRANSMISSION LINES: MICROSTRIP (OR STRIPLINE). USE GROUND PLANE (OR MULTI-LAYER) PRINTED CIRCUIT BOARD FOR BEST HIGH FREQUENCY PERFORMANCE.
4. RESISTORS IN Ω . CAPACITORS IN MICROFARADS. INDUCTORS IN MICROHENRIES.
5. USE HIGH-FREQUENCY MONOLITHIC CERAMIC BYPASS CAPACITORS AND LOW SERIES DC RESISTANCE INDUCTORS. FERRITE INDUCTORS CAN BE USED.
6. CAUTION: DO NOT DIRECTLY CONNECT FIBER-OPTIC MODULE PECL OUTPUTS (DATA, $\overline{\text{DATA}}$, SIGNAL DETECT, $\overline{\text{SIGNAL DETECT}}$) TO GROUND WITHOUT PROPER CURRENT LIMITING IMPEDANCE.
7. DEVICE GROUND PINS SHOULD BE DIRECTLY AND INDIVIDUALLY CONNECTED TO GROUND.
8. DEVICE SOLDER POSTS SHOULD BE DIRECTLY CONNECTED TO PCB FOR OPTIMUM MECHANICAL SUPPORT.

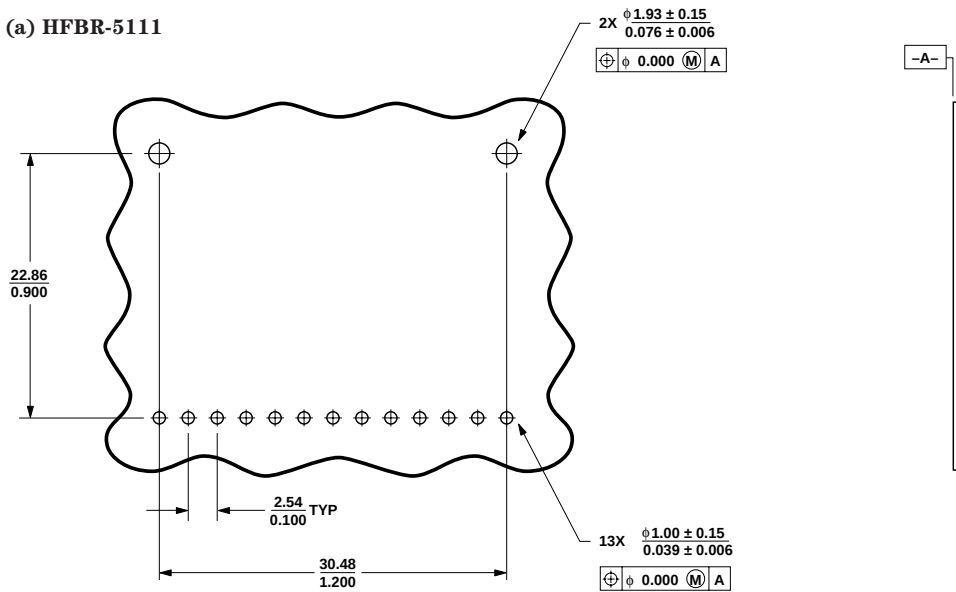
(b) HFBR-5112/-5113

Figure 7. Recommended Decoupling Circuit Diagram.



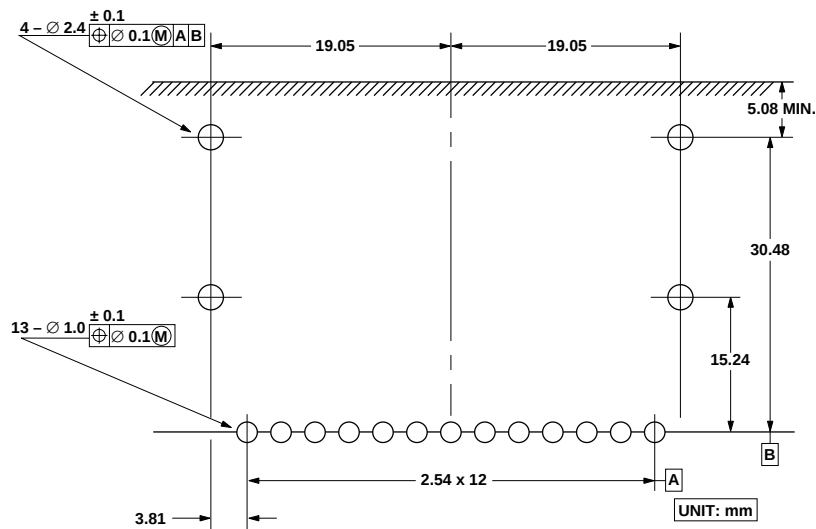
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS OVER INCHES.
2. DIMENSIONS PER ANSI Y 14.5 M.

(a) HFBR-5111



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS OVER INCHES.
2. DIMENSIONS PER ANSI Y 14.5 M.

(b) HFBR-5112



NOTES:
1. TOLERANCE ± 0.05 mm, UNLESS OTHERWISE SPECIFIED.
2. SOLDER POSTS SHOULD BE CONNECTED TO PCB FOR OPTIMUM MECHANICAL SUPPORT.

(c) HFBR-5113

Figure 8. Board Layout-Hole Pattern.

Electrostatic Discharge

There are two design cases in which immunity to ESD damage is important.

The first is during handling of the transceiver prior to mounting it on the circuit board. It is important to use normal ESD handling precautions for ESD-sensitive devices. These precautions include using grounded wrist straps, work benches, and floor mats in ESD-controlled areas.

The second case to consider is static discharges to the exterior of the equipment chassis containing the transceiver parts. To the extent that the MIC connector is exposed to the outside of the equipment chassis, it may be subject to whatever ESD system level test criteria that the equipment is intended to meet.

Electromagnetic Interference (EMI)

Most equipment designs utilizing these high speed transceivers from Hewlett-Packard will be required to meet the requirements of FCC in the United

States, CENELEC EN55022 (CISPR 22) in Europe and VCCI in Japan. Hence, the HFBR-511X Series of fiber optic transceivers meet the regulatory requirements listed in Table 1.

Immunity

Equipment utilizing these transceivers will be subject to radio-frequency electromagnetic fields in some environments. These transceivers have a high immunity to such fields. The internal construction of the HFBR-511X Series is similar to that of the HFBR-510X/-520X series. Therefore, for additional information regarding EMI susceptibility, ESD, and conducted noise testing procedures and results, please refer to Application Note 1075, *Testing and Measuring Electromagnetic Compatibility Performance of the HFBR-510X/-520X Fiber Optic Transceivers*.

Flammability Rating

The housing material of the HFBR-5111/-5112/-5113 transceiver has been approved for UL flammability rating of 94V-0 under General Electric's UL file

number E121562 and similarly under CSA file number LS88480.

Transceiver Reliability and Performance Qualification Data

As with all HP components, the HFBR-511X series transceivers undergo extensive Hewlett-Packard reliability and performance qualification testing. Details are available from your Hewlett-Packard sales representative.

These transceivers are manufactured at the Hewlett-Packard Singapore location which is an ISO 9001 certified facility.

Ordering Information

The Hewlett-Packard FDDI transceivers are available packaged with or without key inserts per Table 2. The key inserts are colored-coded plastic parts with an identifying key letter molded into the top surface of each key.

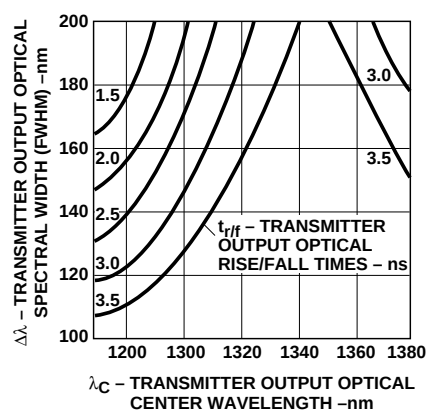
The HFBR-5111/-5112/-5113 products are available through the Hewlett-Packard Component Field Sales Offices and Authorized Distributors worldwide.

Table 1. Regulatory Compliance Table

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883C Method 3015.4	Meets Class 2 (2000 to 3999 Volts) Withstands up to 2200 V applied between electrical pins.
Electrostatic Discharge (ESD) to the MIC Receptacle	Variation of IEC 801-2	Typically withstand at least 25 kV without damage when the MIC Receptacle is contacted by a Human Body Model probe.
Electromagnetic Interference (EMC)	FCC Class B CENELEC CEN55022 Class B (CISPR 22B) VCCI Class 2	Typically provide a 13 dB margin to the noted standard limits when tested at a certified test range with the transceiver mounted to a circuit card without a chassis enclosure.
Immunity	Variation of IEC 801-3	Typically show no measurable effect from a 10 V/m field swept from 10 to 450 MHz applied to the transceiver when mounted to a circuit card without a chassis enclosure.

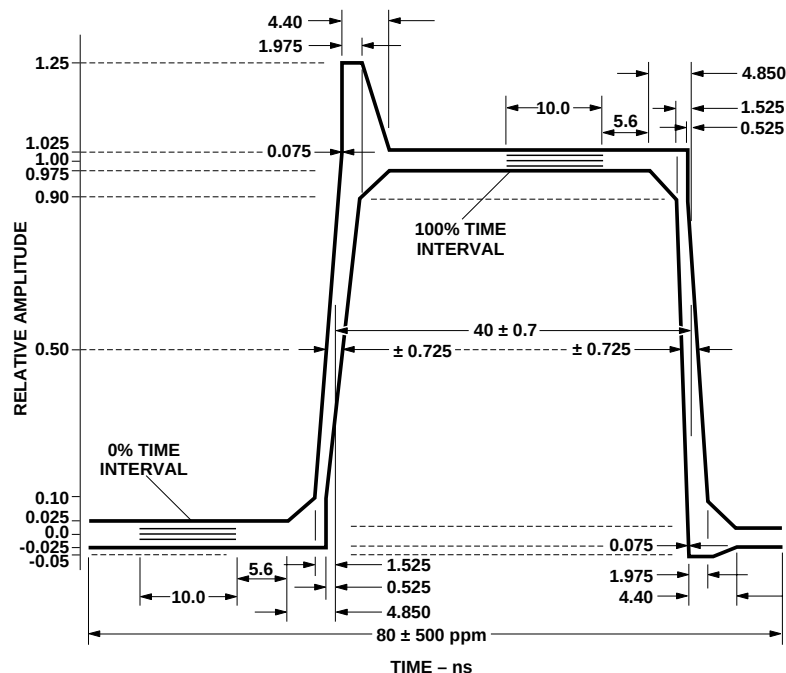
Table 2. Ordering Information

Part Number	Description
Transceivers	
HFBR-5111	2x11 Transceiver with a set of 4 key inserts (A, B, M, and S)
HFBR-5111 Option FDA	2x11 Transceiver with A-key installed
HFBR-5111 Option FDB	2x11 Transceiver with B-key installed
HFBR-5111 Option FDM	2x11 Transceiver with M-key installed
HFBR-5111 Option FDS	2x11 Transceiver with S-key installed
HFBR-5111 Option FDN	2x11 Transceiver with no key inserts included
HFBR-5112	Narrow 1x13 Transceiver with a set of 4 key inserts (A, B, M, and S)
HFBR-5112 Option FDA	Narrow 1x13 Transceiver with A-key installed
HFBR-5112 Option FDB	Narrow 1x13 Transceiver with B-key installed
HFBR-5112 Option FDM	Narrow 1x13 Transceiver with M-key installed
HFBR-5112 Option FDS	Narrow 1x13 Transceiver with S-key installed
HFBR-5112 Option FDN	Narrow 1x13 Transceiver with no key inserts included
HFBR-5113	Standard 1x13 Transceiver with a set of 4 key inserts (A, B, M, and S)
HFBR-5113 Option FDA	Standard 1x13 Transceiver with A-key installed
HFBR-5113 Option FDB	Standard 1x13 Transceiver with B-key installed
HFBR-5113 Option FDM	Standard 1x13 Transceiver with M-key installed
HFBR-5113 Option FDS	Standard 1x13 Transceiver with S-key installed
HFBR-5113 Option FDN	Standard 1x13 Transceiver with no key inserts included
Accessories	
HFBR-5001	One Port Process Plug
HFBR-5198	One Bag of 4 Key Inserts (A,B,M, and S)



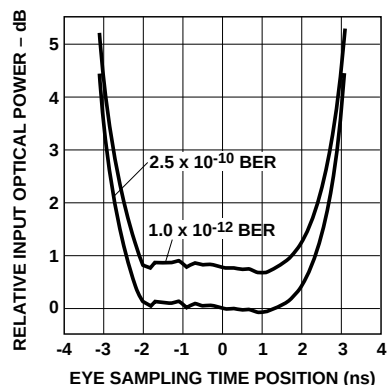
HFBR-511X FDDI TRANSMITTER TEST RESULTS OF λ_C , $\Delta\lambda$ AND $t_{r/f}$ ARE CORRELATED AND COMPLY WITH THE ALLOWED SPECTRAL WIDTH AS A FUNCTION OF CENTER WAVELENGTH FOR VARIOUS RISE AND FALL TIMES.

Figure 9. Transmitter Output Optical Spectral Width (FWHM) vs. Transmitter Output Optical Wavelength and Rise/Fall Times.



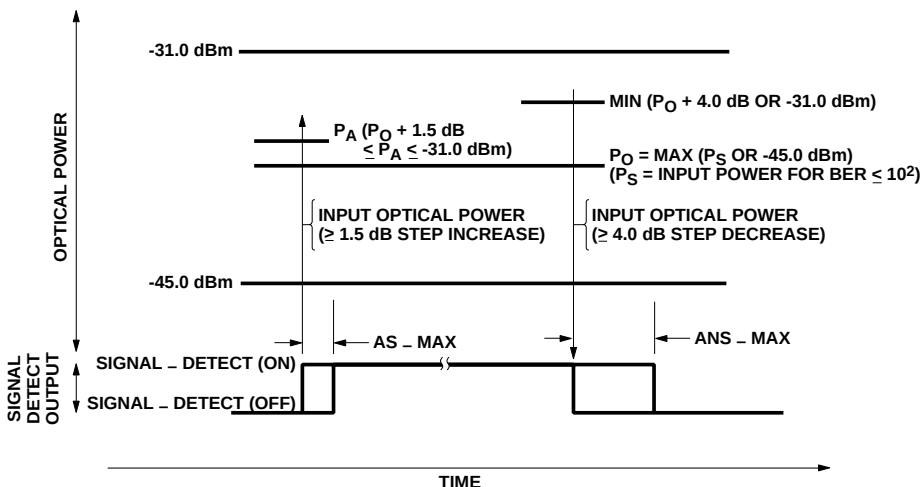
THE HFBR-511X OUTPUT OPTICAL PULSE SHAPE FITS WITHIN THE BOUNDARIES OF THE PULSE ENVELOPE FOR RISE AND FALL TIME MEASUREMENTS.

Figure 10. Output Optical Pulse Envelope.



CONDITIONS:
 1. $T_A = 25^\circ \text{C}$
 2. $V_{CC} = 5 \text{ Vdc}$
 3. INPUT OPTICAL RISE/FALL TIMES = 1.0/2.1 ns.
 4. INPUT OPTICAL POWER IS NORMALIZED TO CENTER OF DATA SYMBOL.
 5. NOTE 20 AND 21 APPLY.

Figure 11. Relative Input Optical Power vs. Eye Sampling Time Position.



AS - MAX — MAXIMUM ACQUISITION TIME (SIGNAL).
 AS - MAX IS THE MAXIMUM SIGNAL - DETECT ASSERTION TIME FOR THE STATION.
 AS - MAX SHALL NOT EXCEED 100.0 μs . THE DEFAULT VALUE OF AS - MAX IS 100.0 μs .
 ANS - MAX — MAXIMUM ACQUISITION TIME (NO SIGNAL).
 ANS - MAX IS THE MAXIMUM SIGNAL - DETECT DEASSERTION TIME FOR THE STATION.
 ANS - MAX SHALL NOT EXCEED 350 μs . THE DEFAULT VALUE OF AS - MAX IS 350 μs .

Figure 12. Signal Detect Thresholds and Timing.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Storage Temperature	T_S	-40		100	°C	
Lead Soldering Temperature	T_{SOLD}			260	°C	
Lead Soldering Time	t_{SOLD}			10	sec.	
Supply Voltage	V_{CC}	-0.5		7.0	V	
Data Input Voltage	V_I	-0.5		V_{CC}	V	
Differential Input Voltage	V_D			1.4	V	Note 1
Output Current	I_O			50	mA	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Ambient Operating Temperature	T_A	0		70	°C	
Supply Voltage	V_{CC}	4.75		5.25	V	
Data Input Voltage – Low	$V_{IL} - V_{CC}$	-1.810		-1.475	V	
Data Input Voltage – High	$V_{IH} - V_{CC}$	-1.165		-0.880	V	
Data and Signal Detect Output Load	R_L		50		Ω	Note 2
Signaling Rate	f_S	10	125		MBd	Note 3 Figures 5, 6

Transmitter Electrical Characteristics

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.75\text{ V}$ to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		145	185	mA	Note 4
Power Dissipation	P_{DISS}		0.76	0.97	W	
Threshold Voltage	$V_{BB} - V_{CC}$	-1.42	-1.3	-1.24	V	Note 5
Data Input Current – Low	I_{IL}	-350	0		μA	
Data Input Current – High	I_{IH}		14	350	μA	

Receiver Electrical Characteristics

($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 4.75\text{ V}$ to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Supply Current	I_{CC}		102	165	mA	Note 6
Power Dissipation	P_{DISS}		0.3	0.5	W	Note 7
Data Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 8
Data Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 8
Data Output Rise Time	t_r	0.35		2.2	ns	Note 9
Data Output Fall Time	t_f	0.35		2.2	ns	Note 9
Signal Detect Output Voltage – Low	$V_{OL} - V_{CC}$	-1.840		-1.620	V	Note 8
Signal Detect Output Voltage – High	$V_{OH} - V_{CC}$	-1.045		-0.880	V	Note 8
Signal Detect Output Rise Time	t_r	0.35		2.2	ns	Note 9
Signal Detect Output Fall Time	t_f	0.35		2.2	ns	Note 9

Transmitter Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Output Optical Power 62.5/125 μm, NA = 0.275 Fiber	P _O	-19 -20	-16.8	-14	dBm avg.	Note 13
Output Optical Power 50/1255 μm, NA = 0.20 Fiber	P _O	-22.5 -23.5	-20.3	-14	dBm avg.	Note 13
Optical Extinction Ratio			0.001 -50	0.03 -35	% dB	Note 14
Output Optical Power at Logic “0” State	P _O (“0”)			-45	dBm avg.	Note 15
Center Wavelength	λ _C	1270	1308	1380	nm	Note 16 Figure 9
Spectral Width – FWHM	Δλ		137	170	nm	Note 16 Figure 9
Optical Rise Time	t _r	0.6	1.0	3.0	ns	Note 16, 17 Figure 9, 10
Optical Fall Time	t _f	0.6	2.1	3.0	ns	Note 16, 17 Figure 9, 10
Duty Cycle Distortion Contributed by the Transmitter	DCD		0.02	0.6	ns p-p	Note 18
Data Dependent Jitter Contributed by the Transmitter	DDJ		0.02	0.6	ns p-p	Note 19
Random Jitter Contributed by the Transmitter	RJ		0	0.69	ns p-p	Note 20

Receiver Optical Characteristics

(T_A = 0°C to 70°C, V_{CC} = 4.75 V to 5.25 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Reference
Input Optical Power Minimum at Window Edge	P _{IN Min.} (W)		-33.5	-31	dBm avg.	Note 21 Figure 11
Input Optical Power Minimum at Eye Center	P _{IN Min.} (C)		-34.5	-31.8	dBm avg.	Note 22 Figure 11
Input Optical Power Maximum	P _{IN Max.}	-14	-11.8		dBm avg.	Note 21
Operating Wavelength	λ	1270		1380	nm	
Duty Cycle Distortion Contributed by the Receiver	DCD		0.02	0.4	ns p-p	Note 10
Data Dependent Jitter Contributed by the Receiver	DDJ		0.35	1.0	ns p-p	Note 11
Random Jitter Contributed by the Receiver	RJ		1.0	2.14	ns p-p	Note 12
Signal Detect – Asserted	P _A	P _D + 1.5 dB		-33	dBm avg.	Note 23, 24 Figure 12
Signal Detect – Deasserted	P _D	-45			dBm avg.	Note 25, 26 Figure 12
Signal Detect – Hysteresis	P _A - P _D	1.5	2.4		dB	Figure 12
Signal Detect Assert Time (off to on)	AS_Max	0	55	100	μs	Note 23, 24 Figure 12
Signal Detect Deassert Time (on to off)	ANS_Max	0	110	350	μs	Note 25, 26 Figure 12

Notes:

1. This is the maximum voltage that can be applied across the Differential Transmitter Data Inputs to prevent damage to the input ESD protection circuit.
2. The outputs are terminated with 50 Ω connected to $V_{CC} - 2$ V.
3. The specified signaling rate of 10 MBd to 125 MBd guarantees operation of the transmitter and receiver link to the full conditions listed in the FDDI Physical Layer Medium Dependent standard. Specifically, the link bit error ratio will be equal to or better than 2.5×10^{-10} for any valid FDDI pattern. The transmitter section of the link is capable of dc to 125 MBd. The receiver is internally ac-coupled which limits the lower signaling rate to 10 MBd. For purposes of definition, the symbol rate (Baud), also called signaling rate, f_s , is the reciprocal of the shortest symbol time. Data rate (bits/sec) is the symbol rate divided by the encoding factor used to encode the data (symbols/bit).
4. The power supply current needed to operate the transmitter is provided to differential ECL circuitry. This circuitry maintains a nearly constant current flow from the power supply. Constant current operation helps to prevent unwanted electrical noise from being generated and conducted or emitted to neighboring circuitry.
5. This value is measured with an output load $R_L = 10$ k Ω .
6. This value is measured with the outputs terminated into 50 Ω connected to $V_{CC} - 2$ V and an Input Optical Power level of -14 dBm average.
7. The power dissipation value is the power dissipated in the receiver itself. Power dissipation is calculated as the sum of the products of supply voltage and currents, minus the sum of the products of the output voltages and currents.
8. This value is measured with respect to V_{CC} with the output terminated into 50 Ω connected to $V_{CC} - 2$ V.
9. The output rise and fall times are measured between 20% and 80% levels with the output connected to $V_{CC} - 2$ V through 50 Ω .
10. Duty Cycle Distortion contributed by the receiver is measured at the 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave),

input signal. The input optical power level is -20 dBm average. See Application Information - Transmitter Jitter Section for further information.

11. Data Dependent Jitter contributed by the receiver is specified with the FDDI DDJ test pattern described in the FDDI PMD Annex A.5. The input optical power level is -20 dBm average. See Application Information - Transmitter Jitter Section for further information.
12. Random Jitter contributed by the receiver is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. The input optical power level is at maximum " $P_{IN Min. (W)}$." See Application Information - Transmitter Jitter Section for further information.
13. These optical power values are measured with the following conditions:
 - The Beginning of Life (BOL) to the End of Life (EOL) optical power degradation is typically 1.5 dB per the industry convention for long wavelength LEDs. The actual degradation observed in Hewlett-Packard's 1300 nm LED products is < 1 dB, as specified in this data sheet.
 - Over the specified operation voltage and temperature ranges.
 - With HALT Line State, (12.5 MHz square-wave), input signal.
 - At the end of one meter of noted optical fiber with cladding modes removed.The average power value can be converted to a peak power value by adding 3 dB. Higher output optical power transmitters are available on special request.
14. The Extinction Ratio is a measure of the modulation depth of the optical signal. The data "0" output optical power is compared to the data "1" peak output optical power and expressed as a percentage. With the transmitter driven by a HALT Line State (12.5 MHz square-wave) signal, the average optical power is measured. The data "1" peak power is then calculated by adding 3 dB to the measured average optical power. The data "0" output optical power is found by measuring the optical power when the transmitter is driven by a logic "0" input. The extinction ratio is the ratio of the optical power at the "0" level compared to the optical

power at the "1" level expressed as a percentage or in decibels.

15. The transmitter provides compliance with the need for Transmit_Disable commands from the FDDI SMT layer by providing an Output Optical Power level of < -45 dBm average in response to a logic "0" input. This specification applies to either 62.5/125 μ m or 50/125 μ m fiber cables.
16. This parameter complies with the FDDI PMD requirements for the tradeoffs between center wavelength, spectral width, and rise/fall times shown in Figure 9.
17. This parameter complies with the optical pulse envelope from the FDDI PMD shown in Figure 10. The optical rise and fall times are measured from 10% to 90% when the transmitter is driven by the FDDI HALT Line State (12.5 MHz square-wave) input signal.
18. Duty Cycle Distortion contributed by the transmitter is measured at a 50% threshold using an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.
19. Data Dependent Jitter contributed by the transmitter is specified with the FDDI test pattern described in FDDI PMD Annex A.5. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.
20. Random Jitter contributed by the transmitter is specified with an IDLE Line State, 125 MBd (62.5 MHz square-wave), input signal. See Application Information - Transceiver Jitter Performance Section of this data sheet for further details.
21. This specification is intended to indicate the performance of the receiver section of the transceiver when Input Optical Power signal characteristics are present per the following definitions. The Input Optical Power dynamic range from the minimum level (with a window time-width) to the maximum level is the range over which the receiver is guaranteed to provide output data with a Bit Error Ratio (BER) better than or equal to 2.5×10^{-10} .
 - At the Beginning of Life (BOL).
 - Over the specified operation temperature and voltage ranges.

- Input symbol pattern is the FDDI test pattern defined in FDDI PMD Annex A.5 with 4B/5B NRZI encoded data that contains a duty cycle base-line wander effect of 50 kHz. This sequence causes a near worst case condition for inter-symbol interference.
- Receiver data window time-width is 2.13 ns or greater and centered at mid-symbol. This worst case window time-width is the minimum allowed eye-opening presented to the FDDI PHY PM_Data indication input (PHY input) per the example in FDDI PMD Annex E. This minimum window time-width of 2.13 ns is based upon the worst case FDDI PMD Active Input Interface optical conditions for peak-to-peak DCD (1.0 ns), DDJ (1.2 ns) and RJ (0.76 ns) presented to the receiver.

To test a receiver with the worst case FDDI PMD Active Input jitter condition requires exacting control over DCD, DDJ and RJ jitter components that is difficult to implement with production test equipment. The receiver can be equivalently tested to the worst case FDDI PMD input jitter conditions and meet the minimum output data window time-width of 2.13 ns. This is accomplished by using a nearly ideal input optical signal (no DCD, insignificant DDJ and RJ) and measuring for a wider

window time-width of 4.6 ns. This is possible due to the cumulative effect of jitter components through their superposition (DCD and DDJ are directly additive and RJ components are rms additive). Specifically, when a nearly ideal input optical test signal is used and the maximum receiver peak-to-peak jitter contributions of DCD (0.4 ns), DDJ (1.0 ns), and RJ (2.14 ns) exist, the minimum window time-width becomes $8.0 \text{ ns} - 0.4 \text{ ns} - 1.0 \text{ ns} - 2.14 \text{ ns} = 4.46 \text{ ns}$, or conservatively 4.6 ns. This wider window time-width of 4.6 ns guarantees the FDDI PMD Annex E minimum window time-width of 2.13 ns under worst case input jitter conditions to the Hewlett-Packard receiver.

- Transmitter operating with an IDLE Line State pattern, 125 MBd (62.5 MHz square-wave), input signal to simulate any cross-talk present between the transmitter and receiver sections of the transmitter.
22. All conditions of Note 21 apply except that the measurement is made at the center of the symbol with no window time-width.
 23. This value is measured during the transition from low to high levels of input optical power.
 24. The Signal Detect output shall be asserted within 100 μs after a step increase of the Input Optical Power.

The step will be from a low Input Optical Power, $\leq -45 \text{ dBm}$, into the range between greater than P_A , and -14 dBm . The BER of the receiver output will be 10^{-2} or better during the time, LS_Max (15 μs) after Signal Detect has been asserted. See Figure 12 for more information.

25. This value is measured during the transition from high to low levels of input optical power. The maximum value will occur when the input optical power is either -45 dBm average or when the input optical power yields a BER of 10^{-2} or better, whichever power is higher.
26. Signal detect output shall be deasserted within 350 μs after a step decrease in the Input Optical Power from a level which is the lower of: -31 dBm or $P_D + 4 \text{ dB}$ (P_D is the power level at which signal detect was deasserted), to a power level of -45 dBm or less. This step decrease will have occurred in less than 8 ns. The receiver output will have a BER of 10^{-2} or better for a period of 12 μs or until signal detect is deasserted. The input data stream is the Quiet Line State. Also, signal detect will be deasserted within a maximum of 350 μs after the BER of the receiver output degrades above 10^{-2} for an input optical data stream that decays with a negative ramp function instead of a step function. See Figure 12 for more information.