EV2064

EVALUATION BOARD

Quad Serial Backplane Device

Introduction

The S2064 evaluation board provides a flexible platform for verifying the operation of the S2064 Quad Serial Backplane device. This document provides information on the evaluation board's contents. It should be used in conjunction with the S2064 product data sheet. Contact your local AMCC field applications engineer or regional sales manager to discuss any questions or concerns you may have.

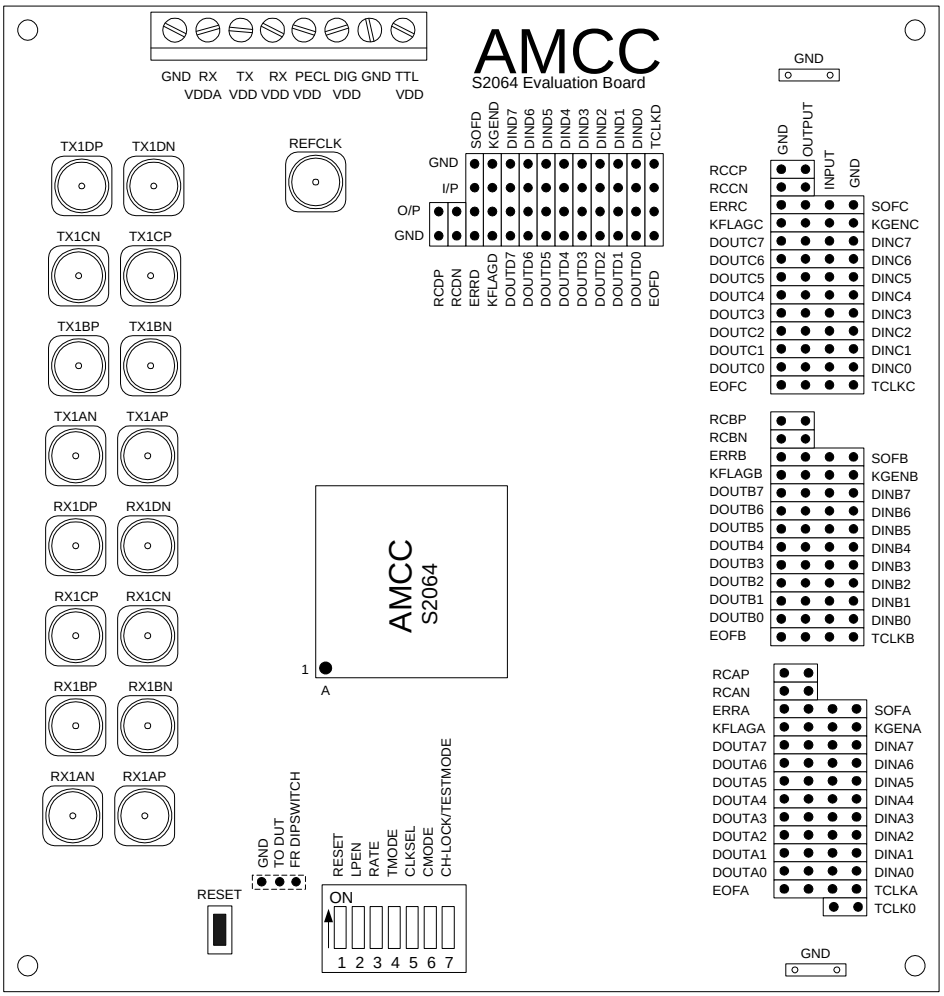
EV2064 Kit Contents

S2064 evaluation board
EV2064 Device Specification (This document)
Four minicoax cables (To loop back clock in parallel loopback configuration)

Board Description

The top view of the EV2064 evaluation board is shown in Figure 1. The high speed differential LVPECL receive RXxP/N, and transmit TXxP/N, where x = A through D, are brought in and out on SMA connectors as shown on the left side of the board.

Figure 1. S2064 Evaluation Board



The reference clock is brought in through the SMA connector labeled REFCLK. Power and ground are brought in through the connector at the top of the board. The S2064 voltage is specified at 3.3V +/- 5%. Parallel I/O are brought in and out on the connector banks on the right side and top of the board; there is one connector bank for each channel (A through D). Input and output static control signals are controlled with the use of the DIP switch at the bottom of the board. DIP switch settings are outlined in Table 1. Moving the switch to the on position creates a logic 1 (High), moving it away from the on setting creates a logic 0 (Low).

Table 1. DIP Switch Settings

DIP Name	Description
RESET	When Low, the S2064 is held in reset, When High, the S2064 operates normally.
LPEN	Loopback Enable. When Low, the device performs normal transceiver operation. When High the serial output for each channel is looped back to its input. The serial outputs are squelched when LPEN = High.
RATE	When Low the S2064 operates with the serial output rate equal to the VCO frequency. When High the S2064 operates with the VCO internally divided by 2 for all functions.
TMODE	Transmit Mode Control. When TMODE is Low, REFCLK is used to clock data on DINx[7:0], SOFx, and KGENx into the S2064. When TMODE is High, TCLKx is used to clock data into the S2064. In Channel Lock mode (CH_LOCK HIGH), all four channels are clocked by TCLKA. In independent mode (CH_LOCK LOW) each channel is clocked by its respective TCLK.
CLKSEL	REFCLK Select input. This signal configures the PLL for the appropriate REFCLK frequency. When CLKSEL = 0, the REFCLK frequency should equal the parallel word rate. When CLKSEL = 1, the REFCLK frequency should be 1/2 the parallel word rate (and is internally x2 multiplied).
CMODE	Clock Mode Control for receiver data stream. When Low, the rate of the parallel output clock (RCxP/N) is 1/2 the data rate, for ping/pong clocking. When High, the rate of the parallel output clock (RCxP/N) is equal to the data rate.
CH_LOCK/TESTMODE	Parallel input mode control. Channel Lock High locks all four channels together. (see Device Specification). Channel Lock Low provides independent channel operation.

Test Setups

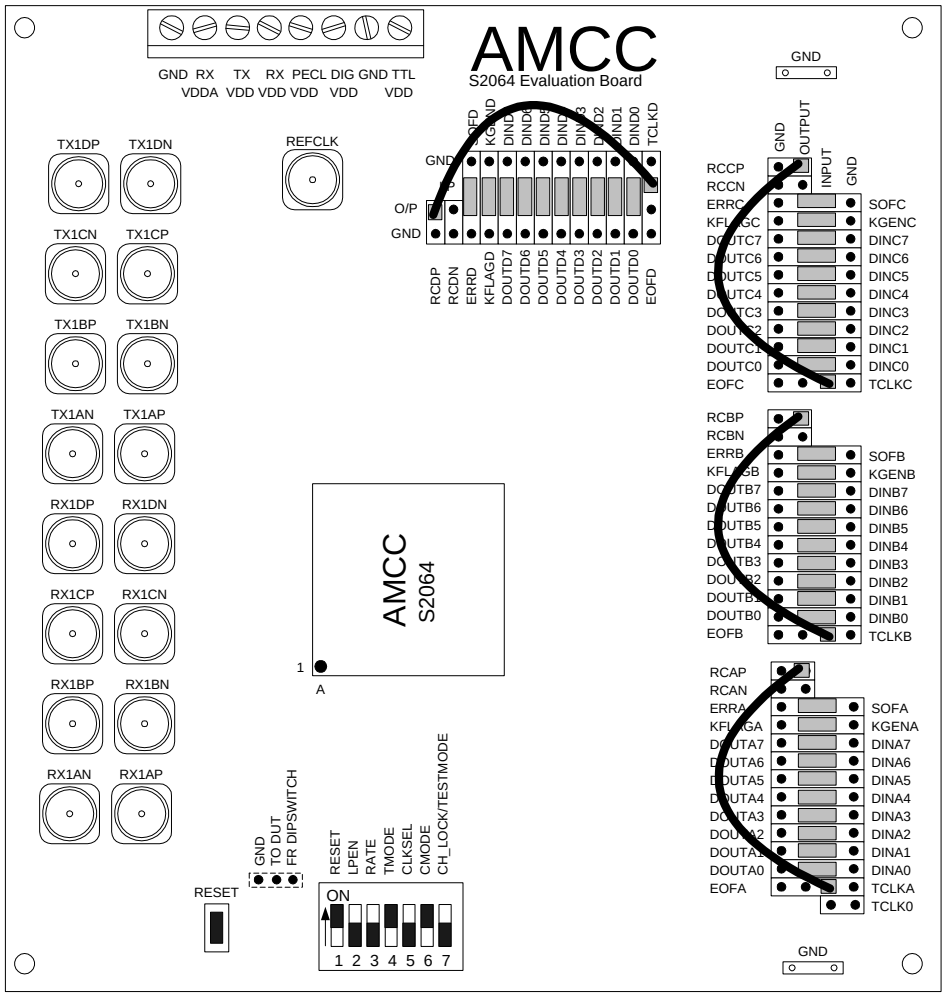
The typical test performed with the S2064 evaluation board is jitter testing. In each case it is easiest to configure the evaluation board for serial I/O, looping back the parallel I/O with jumpers. Serial I/O (parallel loopback) configuration is shown in Figure 2 and described below.

DIP switch settings for parallel loopback:

RESET	HIGH
LPEN	LOW
RATE	HIGH or LOW (determined by desired serial data rate)
TMODE	HIGH
CLKSEL	HIGH or LOW (determined by desired reference clock rate)
CMODE	HIGH
CH-LOCK/TEST MODE	LOW

In order to configure the board for parallel loopback, the parallel input data must be clocked into the device with the TCLKx input clocks as shown in Figure 2. This clock is provided by looping the RCxP output clock back into the respective TCLKx input with one of the minicoax cables provided in the EV2064 Kit. These cables need only be connected for the channel(s) under test.

Figure 2. Parallel Loopback Configuration



Note: The following pin names on the S2064 data sheet are labeled differently on the board:

PIN NAMES	BOARD LABEL
DOUTx8	KFLAGx
DOUTx9	ERRx
DINx8	KGENx
DINx9	SOFx
TBC	TCLKx
RBC1x	RCxP
RBC0x	RCxN
COM_DETx	EOFx

Schematic/Bill of Materials

Figures 3 and 4 provide a schematic representation of the S2064 evaluation board. The bill of materials is outlined in Tables 2 and 3.

Figure 3. EV2064 Schematic

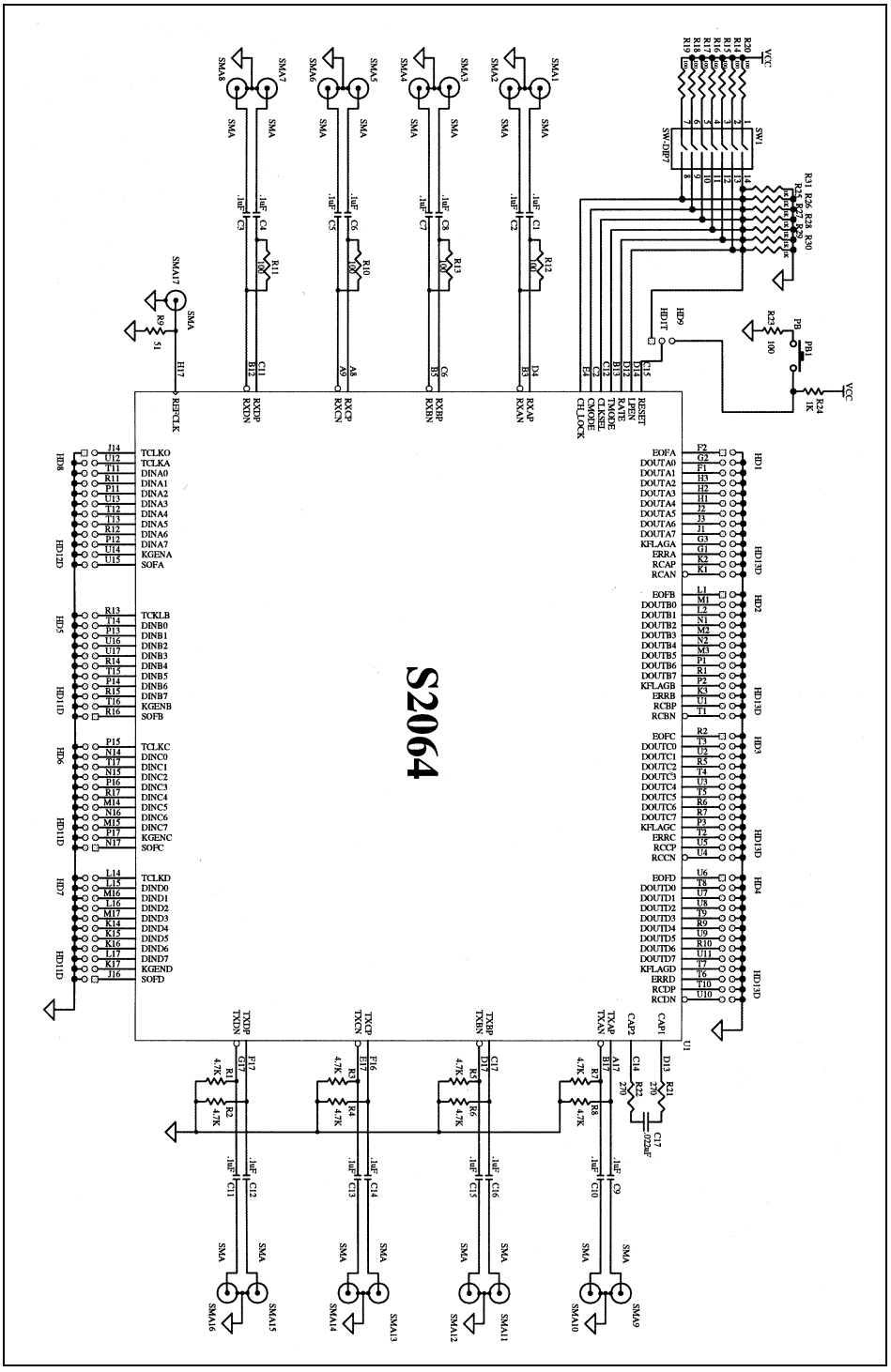


Figure 4. EV2064 Power and Ground Connections

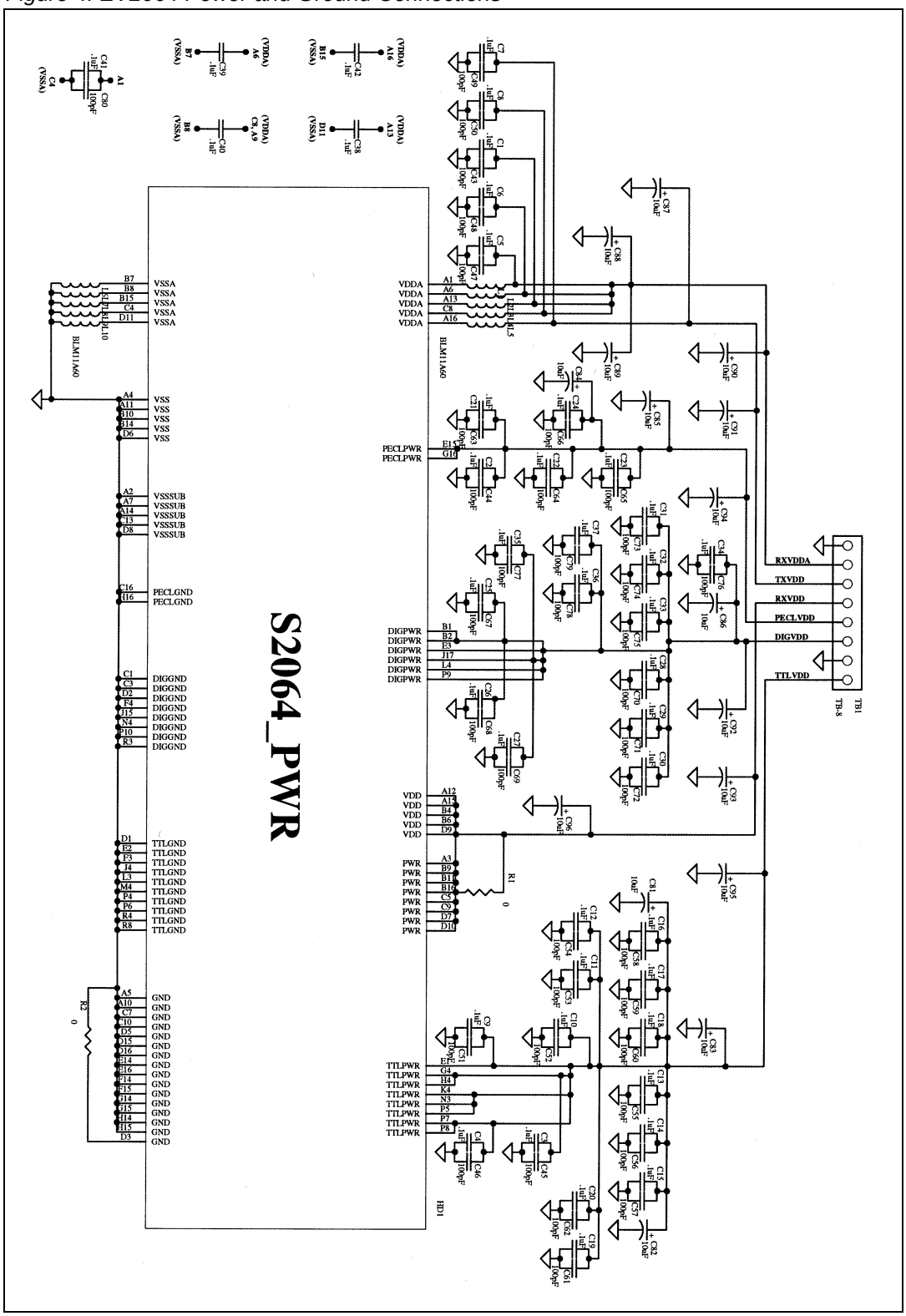


Table 2. S2064 Evaluation Board Bill of Materials

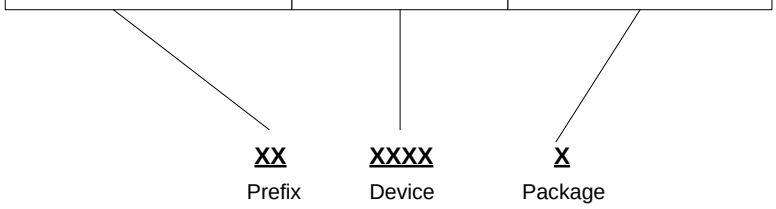
Quantity	Component Value	Designators
16	0.1 µF	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16
1	0.022 µF	C17
8	1 kΩ	R24 R25 R26 R27 R28 R29 R30 R31
8	4.7 kΩ	R1 R2 R3 R4 R5 R6 R7 R8
1	51 Ω	R9
12	100 Ω	R10 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R23
2	270 Ω	R21 R22
1	HD1T	HD9
3	HD11D	H5 H6 H7
1	HD12D	HD8
4	HD13D	HD1 HD2 HD3 HD4
1	PB	PB1
1	S2064	U1
17	SMA	SMA1 SMA2 SMA3 SMA4 SMA5 SMA6 SMA7 SMA8 SMA9 SMA10 SMA11 SMA12 SMA13 SMA14 SMA15 SMA16 SMA17
1	SW-DIP7	SW1

Table 3. S2064 Power and Ground Bill of Materials

Quantity	Component Value	Designators
42	0.1 µF	C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42
2	0 Ω	R1 R2
16	10 µF	C81 C82 C83 C84 C85 C86 C87 C88 C89 C90 C91 C92 C93 C94 C95 C96
38	100 pF	C43 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C56 C57 C58 C59 C60 C61 C62 C63 C64 C65 C66 C67 C68 C69 C70 C71 C72 C73 C74 C75 C76 C77 C78 C79 C80
10	BLM11A60	L1 L2 L3 L4 L5 L6 L7 L8 L9 L10
1	S2064_PWR	HD1
1	TB-8	TB1

Ordering Information

Prefix	Device	Package
EV - Evaluation Board	2064	A - 208 TBGA



Applied Micro Circuits Corporation
6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 — (800) 755-2622 — Fax: (858) 450-9885
http://www.amcc.com