EV3026

EVALUATION BOARD

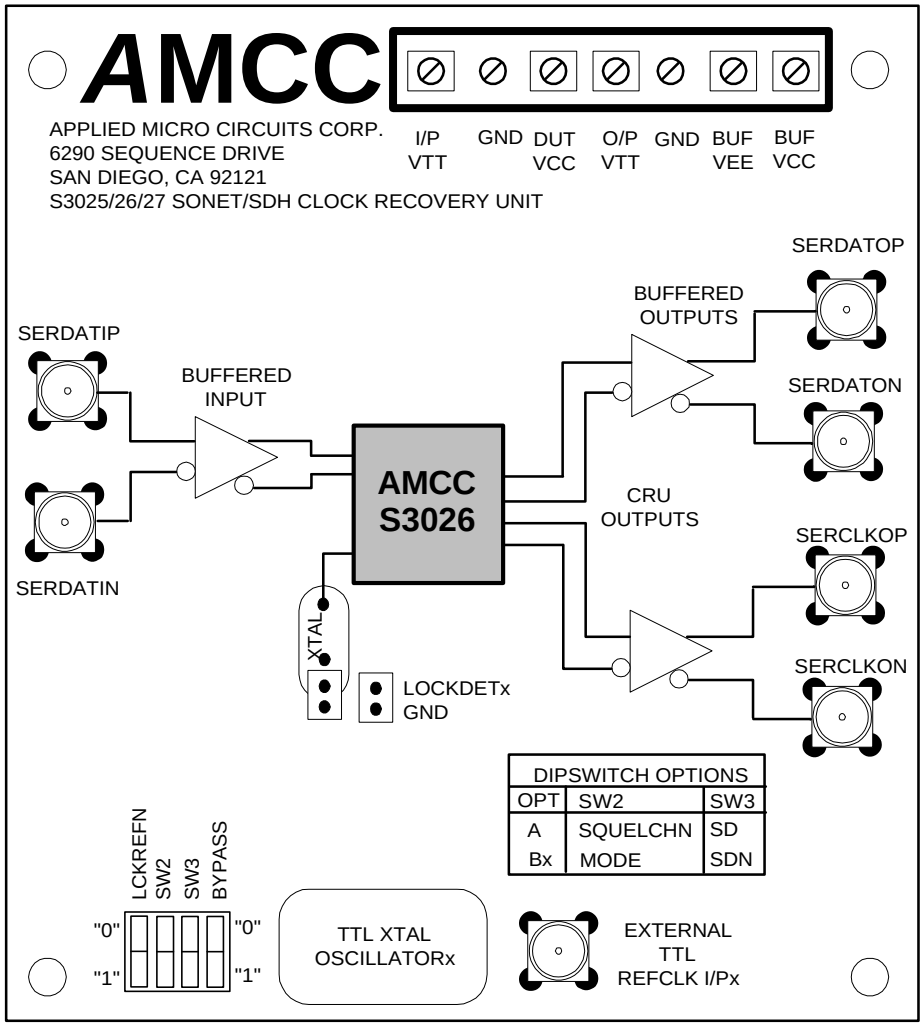
SONET/SDH Clock Recovery Unit

Description

The S3026 evaluation board provides a flexible platform for verifying the operation of the S3026 Clock Recovery Unit (CRU). This document provides information on the board contents and layout. It should be used in conjunction with the S3026 data sheet, which contains full technical details on the chips operation.

The S3026 board is factory configured as “option B” allowing control of the operating speed via the MODE signal (SW2) and providing a test point to monitor the LOCKDET output. Option B allows operation of the S3026 with either an on-board TTL crystal oscillator or with an external oscillator connected via the external TTL REFCLK I/Px connector.

Figure 1. Evaluation Board Layout Top View



Electrical Connections

Power Connections

Terminal posts are provided at the top edge of the board allowing separate control of voltage levels for the input signal termination, the S3026 itself, and 1

the S3026 output terminations.

The buffers translate between the external test equipment environment or other standard ECL and/or +5V referenced ECL systems to supply the correct +5V referenced ECL to the device. The separately powered output buffers allow easy connection to the 50 Ω to ground inputs of high performance oscilloscopes and spectrum analyzers as well as the standard ECL I/O of serial Bit Error Rate Testers (BERT) and jitter analyzers. Table 1 illustrates the nominal input voltages for IP VTT, DUT VCC and O/P VTT. The options for BUF VEE and BUF VCC are paired vertically.

Table 1. Power Connections for DUT and Test Equipment Interface

Power Supply	Nominal Input Voltage
I/P VTT	0V / -2.0V / +3V
DUT VCC	5.0V
GND	0.0V
O/P VTT	DUT VCC -2V
BUF VEE	-3.0V / 0.0V / -5.0V
BUF VCC	2.0V / 5.0V / 0.0V

SMA Connectors

Six coaxial SMA connectors are provided for the differential serial data input/output signals and output clock. An additional SMA connector is provided for an optional external reference clock. (See Figure 1 for locations.)

Serial Data In [SERDATIP/N] - Buffered Differential AC coupled PECL inputs. The clock is recovered from the transitions on these inputs. On-board termination of 50 Ω to I/P VTT is provided, allowing proper termination of PECL, ECL, or ground terminated data sources.

Serial Data Out [SERDATOP/N] - Buffered Differential PECL outputs. The delayed version of the input serial data retimed by the recovered serial clock. The buffered outputs can drive PECL, ECL, or ground terminated instrument inputs. Driven inputs must provide a 50 Ω DC termination to the respective reference. These are the recommended outputs for connection of the evaluation board to monitoring instrumentation.

Serial Clock Out [SERCLKOP/N] - Buffered Differential PECL outputs. The recovered serial clock, with the rising edge of SERCLKOP centered in the SERDATOP/N bit period. The buffered outputs can drive PECL, ECL, or ground terminated instrument inputs. Driven inputs must provide a 50 Ω DC termination to the respective reference. These are the recommended outputs for connection of the evaluation board to monitoring instrumentation.

Note: Accurate measurement also requires the removal of on-board zero Ω jumpers for correct impedance matching to external 50 Ω cabling and instrumentation. Please consult AMCC for appropriate in-factory reconfiguration.

External TTL Reference Clock [EXTERNAL TTL REFCLK I/Px] - TTL input providing access to the TLL Reference Clock (TTLREF) input of the S3026. This input allows operation at other than the two available SONET/SDH data rates. The provided TTL crystal oscillator must be removed if use of an external reference is desired. This connector can also be used to monitor the provided TTL oscillator output.

Lock Detect [LOCKDET] - PECL output (Test Point). In addition to AMS connectors, the LOCKDET output is available on a test pin post for monitoring with a high impedance DVM or scope probe.

DIP Switch

The four element DIP switch allows control of the static inputs of the S3026. The OFF (open = 1) condition of the DIP switch asserts a logic high on the assigned signal, and the ON condition asserts a logic low. In option B, SW2 controls the MODE input. OFF allows operation at 622.08 Mbit/s, ON selects 155.52 Mbit/s.

SW3 of the DIP switch controls the PECL SDN input. ON allows the S3026 to recover the clock from the serial data stream. OFF will force the S3026 to lock to the reference clock. LCKREFN when ON will also force the S3026 to lock to the reference clock. BYPASS should be ON for normal operation.

Figure 2. S3026 Evaluation Board Schematic

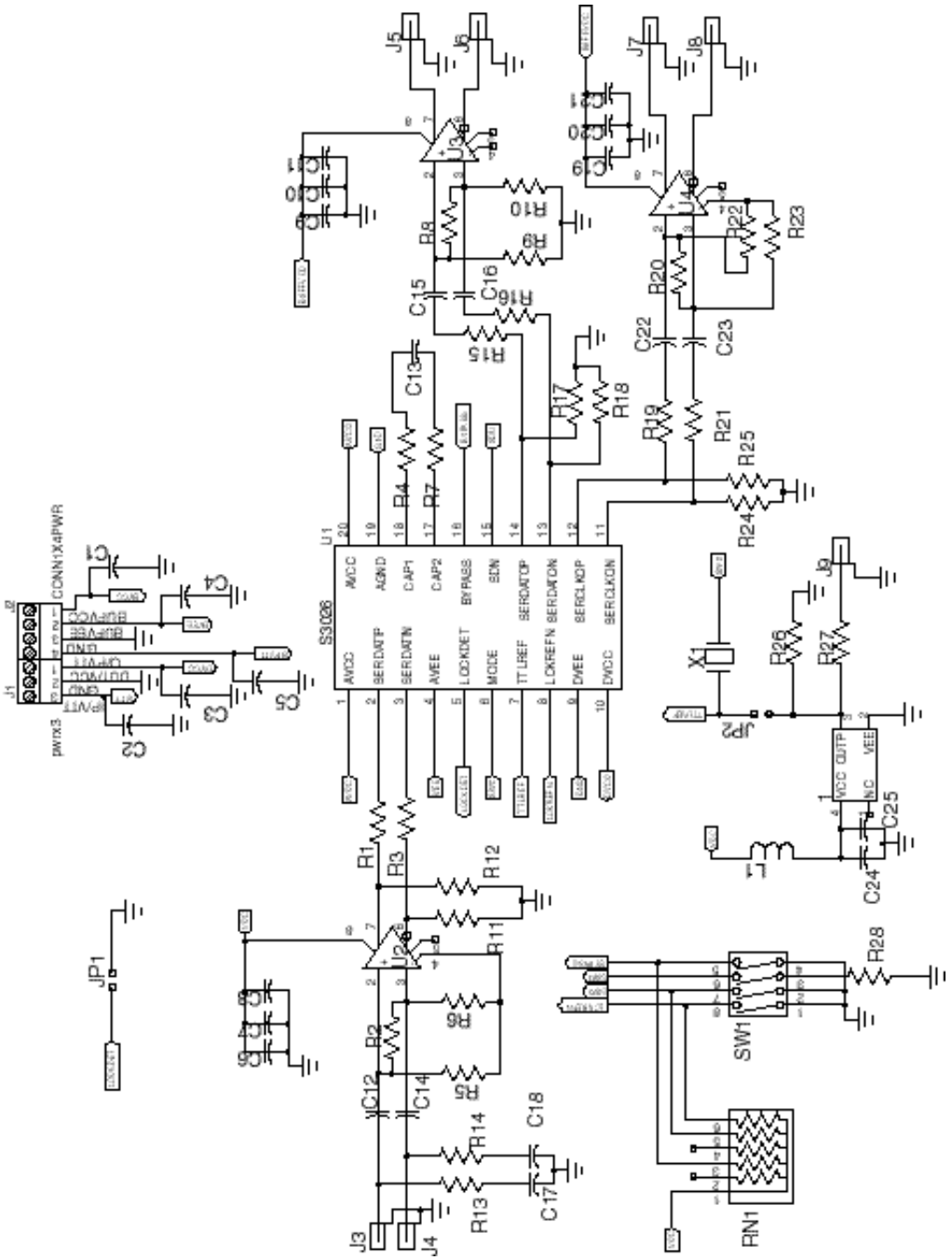


Table 2. EV3026 Bill of Materials

Count	Component Name	Pattern	Value	Ref Des
3	CC0402	0402	0.1 µF	C12
				C15
				C22
3	CC0604	0603	0.1 µF	C14
				C16
				C23
5	CC0604	0603	10 µF	C1
				C2
				C3
				C4
				C5
5	CC0805	0805	0.1 µF	C7
				C10
				C18
				C20
				C24
3	CC0805	0805	1 µF	C9
				C13
				C19
1	CC0805	0805	10 µF	C6
5	CC0805	0805	100 pF	C8
				C11
				C17
				C21
				C25
1	CONN1X4PWR	CONN1X4PWR		J2
1	CRYSTAL		not used	X1
1	DIP4		dip4	SW1
1	IND	1206	f.b.	L1
2	JP1X2	JP1X2		JP1
				JP2

Table 2. EV3026 Bill of Materials

Count	Component Name	Pattern	Value	Ref Des
3	MC100EL16	SO8		U2
				U3
				U4
1	OSCTTL	OSC	19.44 MHz	1
1	PWRCONX3		pwrx3	J1
2	RC0603	0603	1 kΩ	R22
				R23
2	RC0603	0603	50 Ω	R24
				R25
2	RC0603	0603	51 Ω	R13
				R14
2	RC0603	0603	330 Ω	R11
				R12
3	RC0805	0805	0 Ω	R15
				R16
				R21
2	RC0805	0805	0 Ω	R1
				R27
1	RC0805	0805	0 Ω	R3
4	RC0805	0805	1 kΩ	R5
				R6
				R9
				R10
1	RC0805	0805	2 kΩ	R28
2	RC0805	0805	50 Ω	R17
				R18
1	RC0805	0805	51 Ω (opt)	R26
2	RC0805	0805	82 Ω	R4
				R7
3	RC0805	0805	100 Ω	R2
				R8

Table 2. EV3026 Bill of Materials

Count	Component Name	Pattern	Value	Ref Des
				R20
1	RC0805	0805	0 Ω	R19
1	RES6SIPB	SIP6	1 kΩ	RN1
1	S3026		S3026	U1
7	SMA-EDGE	SMA-EDGE		J3
				J4
				J5
				J6
				J7
				J8
				J9

Ordering Information

Prefix	Device	Package	Speed Grade
EV - Evaluation Board	3026	A- 20 TSSOP	1 - 155 Mbps Blank - 622 Mbps

X	XXXX	X	X
Prefix	Device	Package	Speed Grade

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