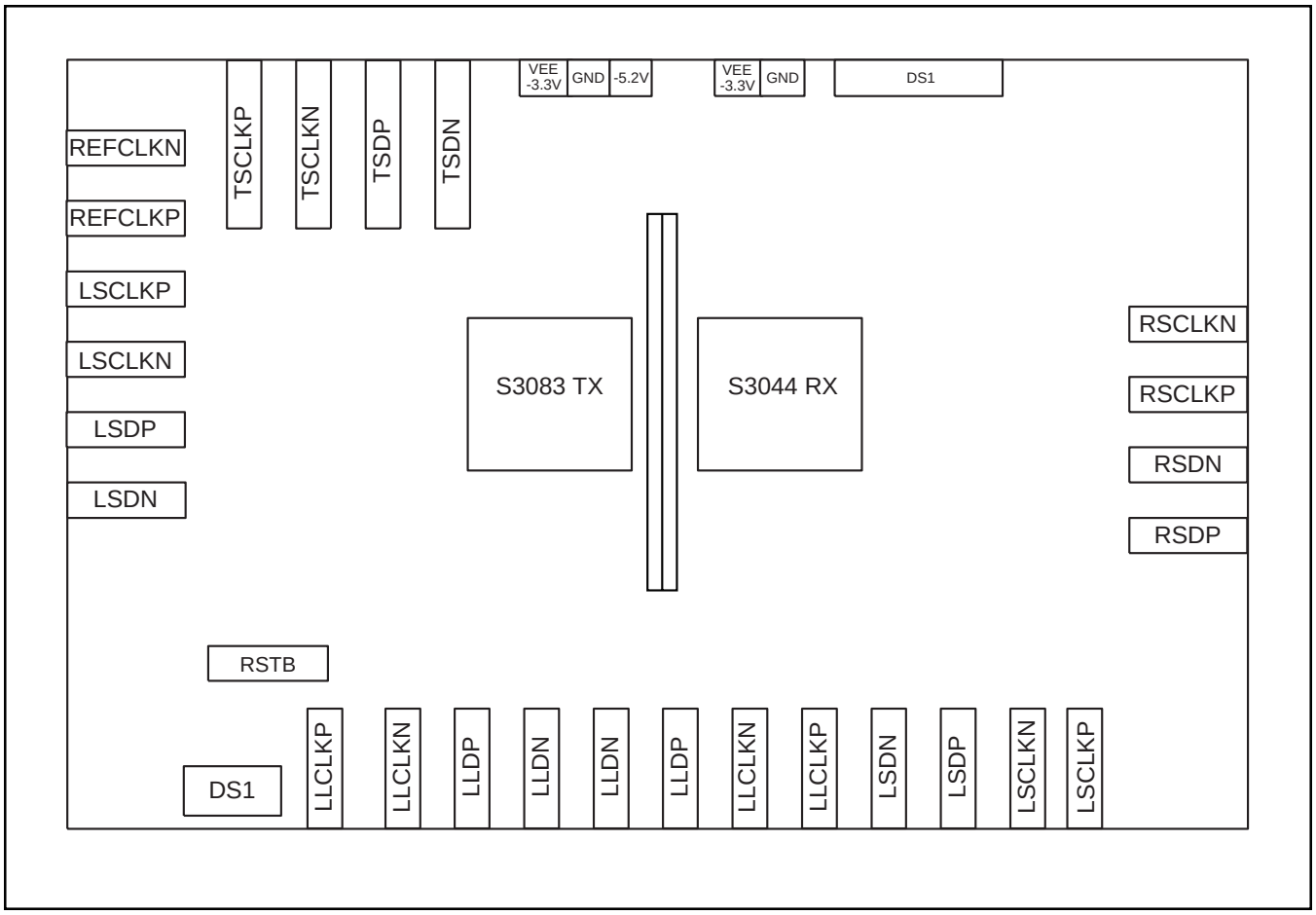
DESCRIPTION

The S3083/S3044 Evaluation Board provides a flexible platform for verifying the operation of the S3083/S3044 transceiver interface circuit. This document provides information on the board contents. It should be used in conjunction with the S3083 and S3044 data sheets, which contains the full technical details on the chips operation.

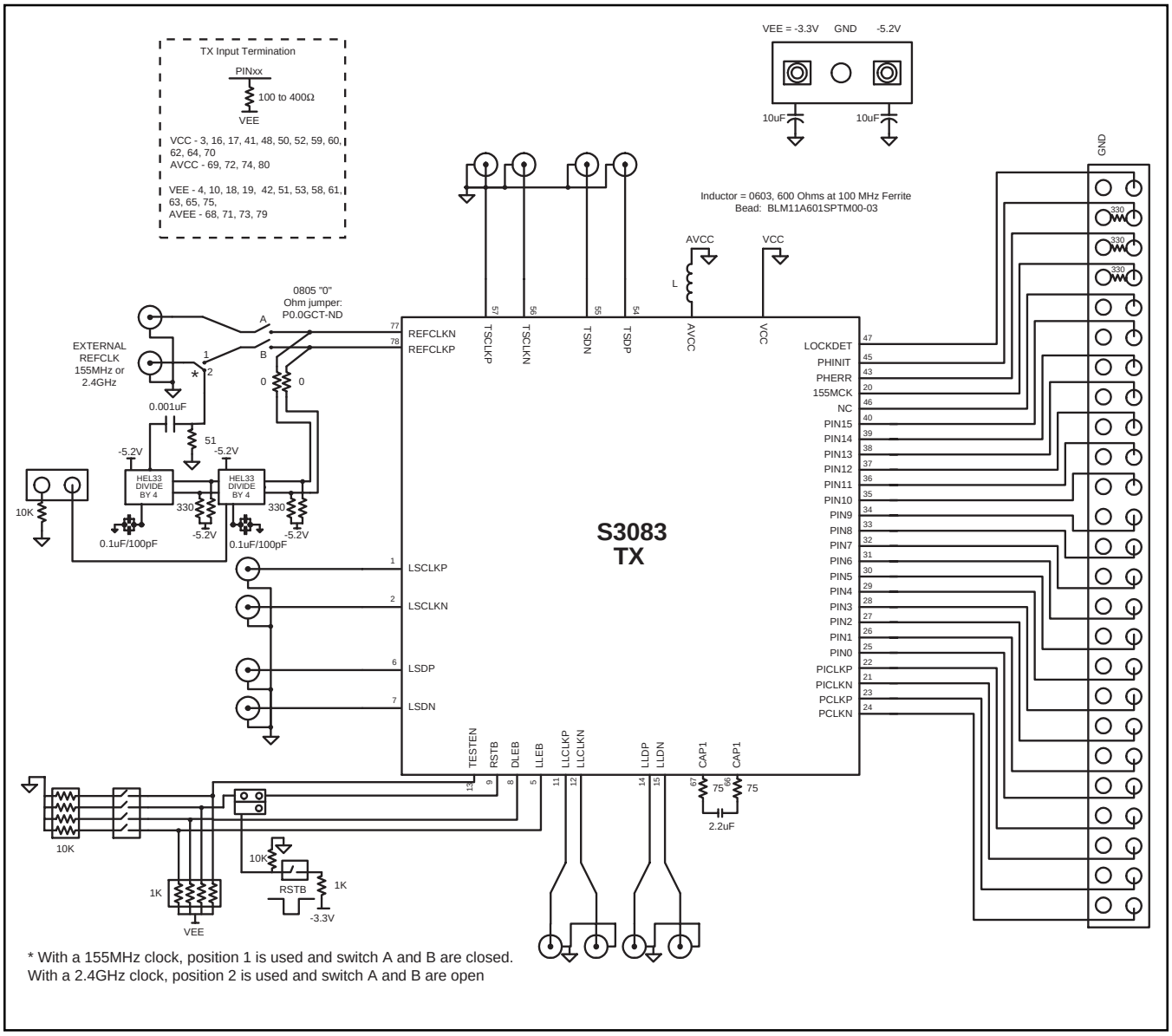
Figure 1 shows the outline of the S3083/S3044 Evaluation Board, and Figure 5 shows the block diagram of how the S3083/S3044 Evaluation Board should be connected to test equipment for Bit Error Rate (BER) testing. In this configuration the S3083/S3044 is configured for use with the internal VCO, using a 155.52 MHz reference and operating at STS-48/STM-16 rate. Figure 6 shows the block diagram for jitter generation testing of the S3083/S3044 Evaluation Board with jitter analyzer test equipment. Figure 7 shows the block diagram for Line Loopback (LLEB) mode. Figure 8 shows the block diagram for Diagnostic Loopback (DLEB) mode.

Figure 1. Evaluation Board Top View



1. Note: DS = Dip Switch

Figure 2. Schematic of the S3083 Evaluation Board



* With a 155MHz clock, position 1 is used and switch A and B are closed.
With a 2.4GHz clock, position 2 is used and switch A and B are open

Figure 3. Schematic of the S3044 Evaluation Board

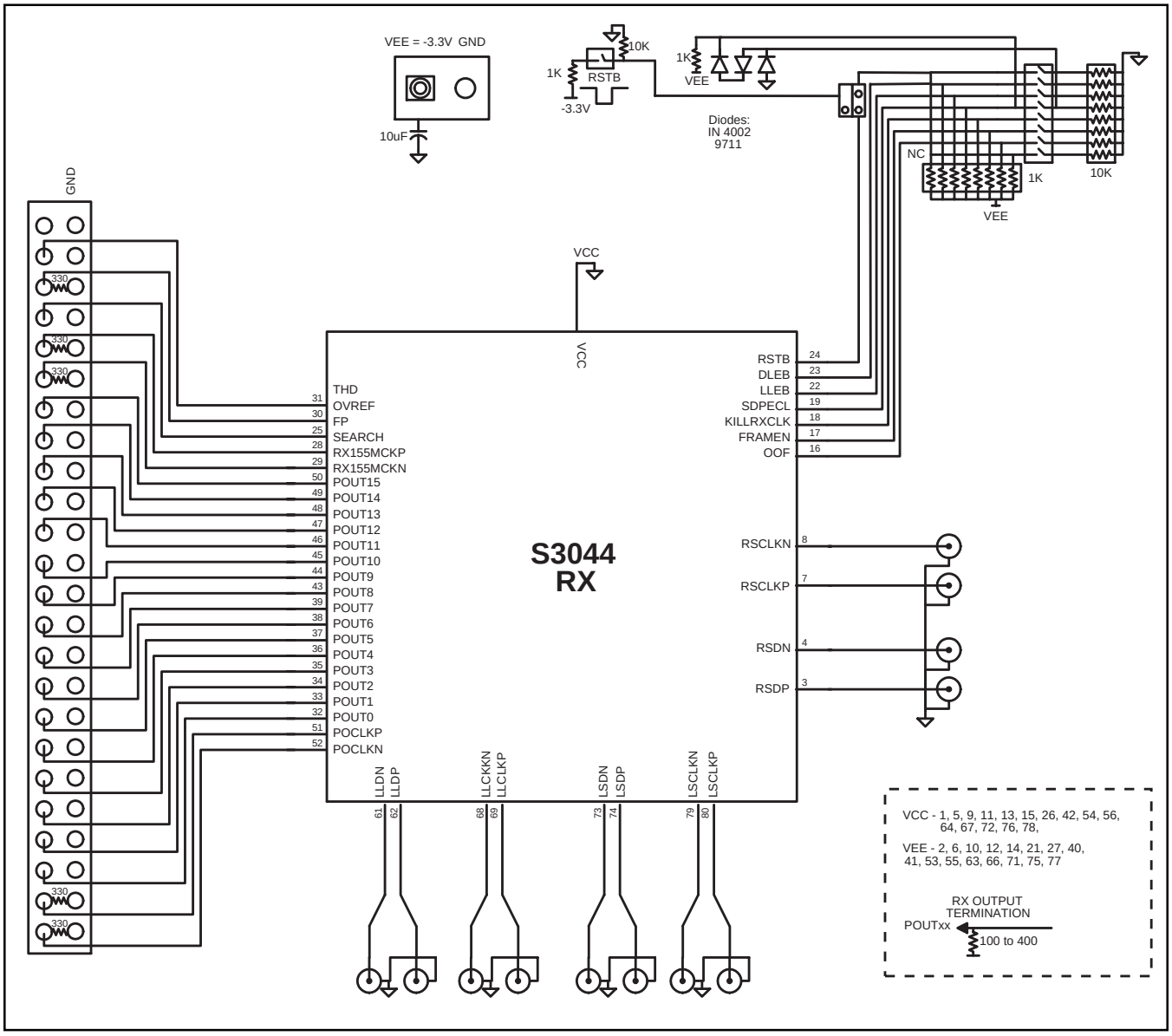
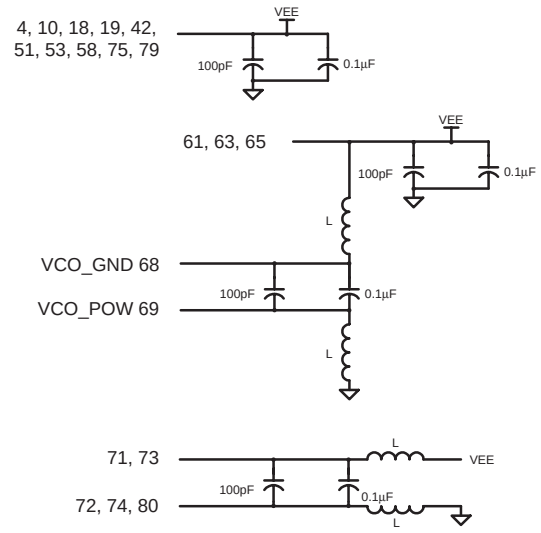


Figure 4. Power and Ground Connections

S3083 TX Power and Ground Connections



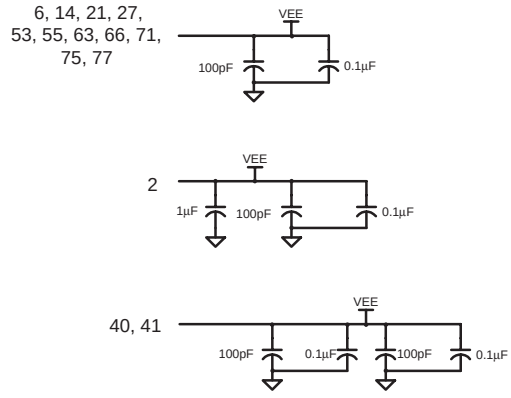
Ground (VCC) = 3, 16, 17, 41, 48, 50, 52, 59, 60, 62, 64, 70

Capacitors 0603 X7R

Inductors (L) = 0603, 600 Ohms at 100 MHz Ferrite Bead: BLM11A601SPTM00-03

S3044 RX Power and Ground Connections

Pins 10, 12 are tied to VEE



Ground (VCC) = 1, 5, 9, 11, 13, 15, 26, 42, 54, 56, 64, 67, 72, 76, 78

0603 X7R Capacitors

Figure 5 depicts how the S3083/S3044 Evaluation board can be connected for BER measurements, and shows all of the dip switch settings and the power supply requirements for use with test equipment that utilizes 50 ohms to ground termination.

Figure 5. BER Test Setup (S3083/S3044 Setup for Normal Operation Serial In Serial Out)

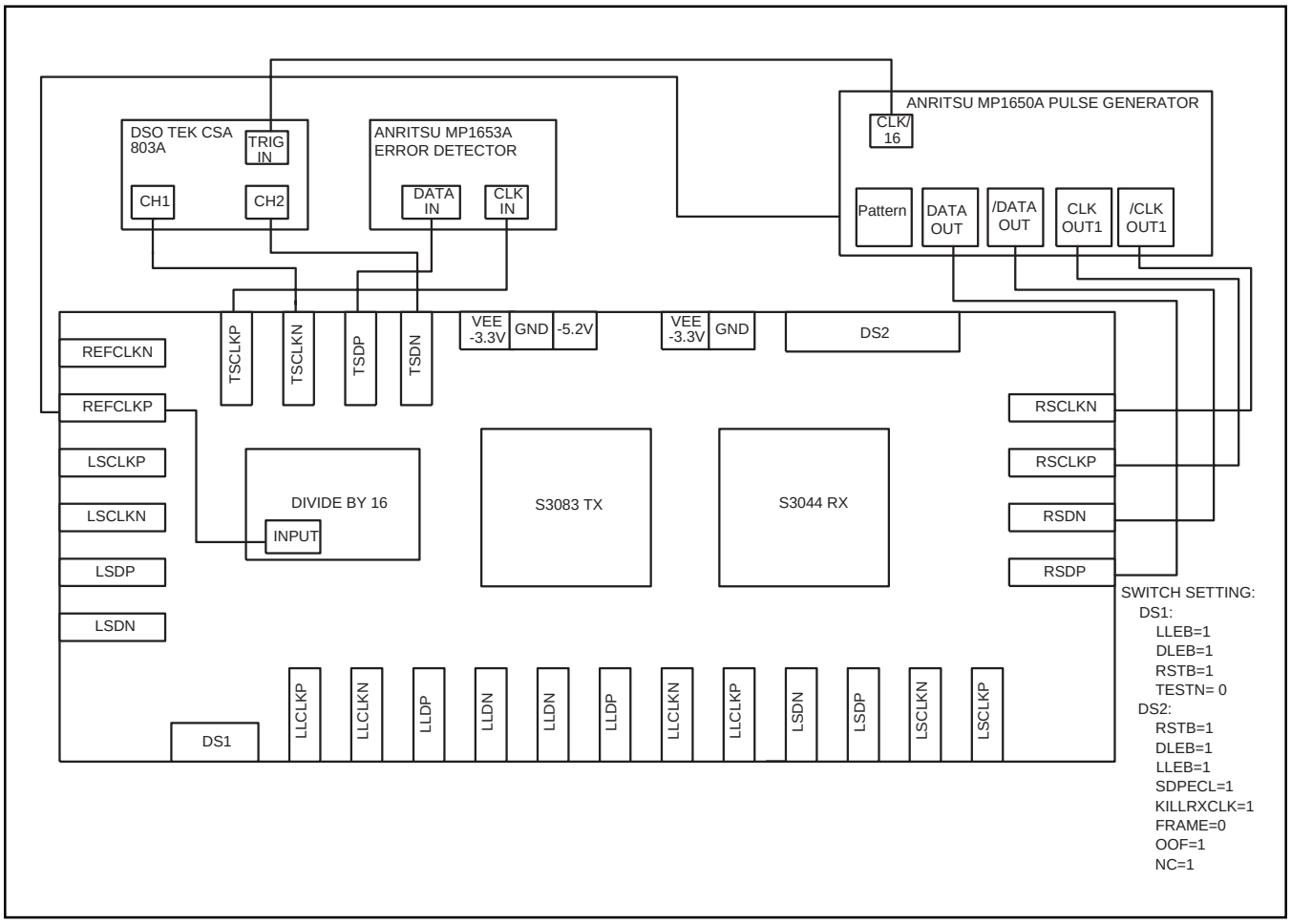


Figure 6 depicts how the S3083/S3044 Evaluation board can be setup for Jitter Generation measurements, and shows all of the dip switch settings and the power supply requirements for use with test equipment that utilizes 50 ohms to ground termination.

Figure 6. Jitter Generation Test Setup (Setup for Jitter Generation Measurement)

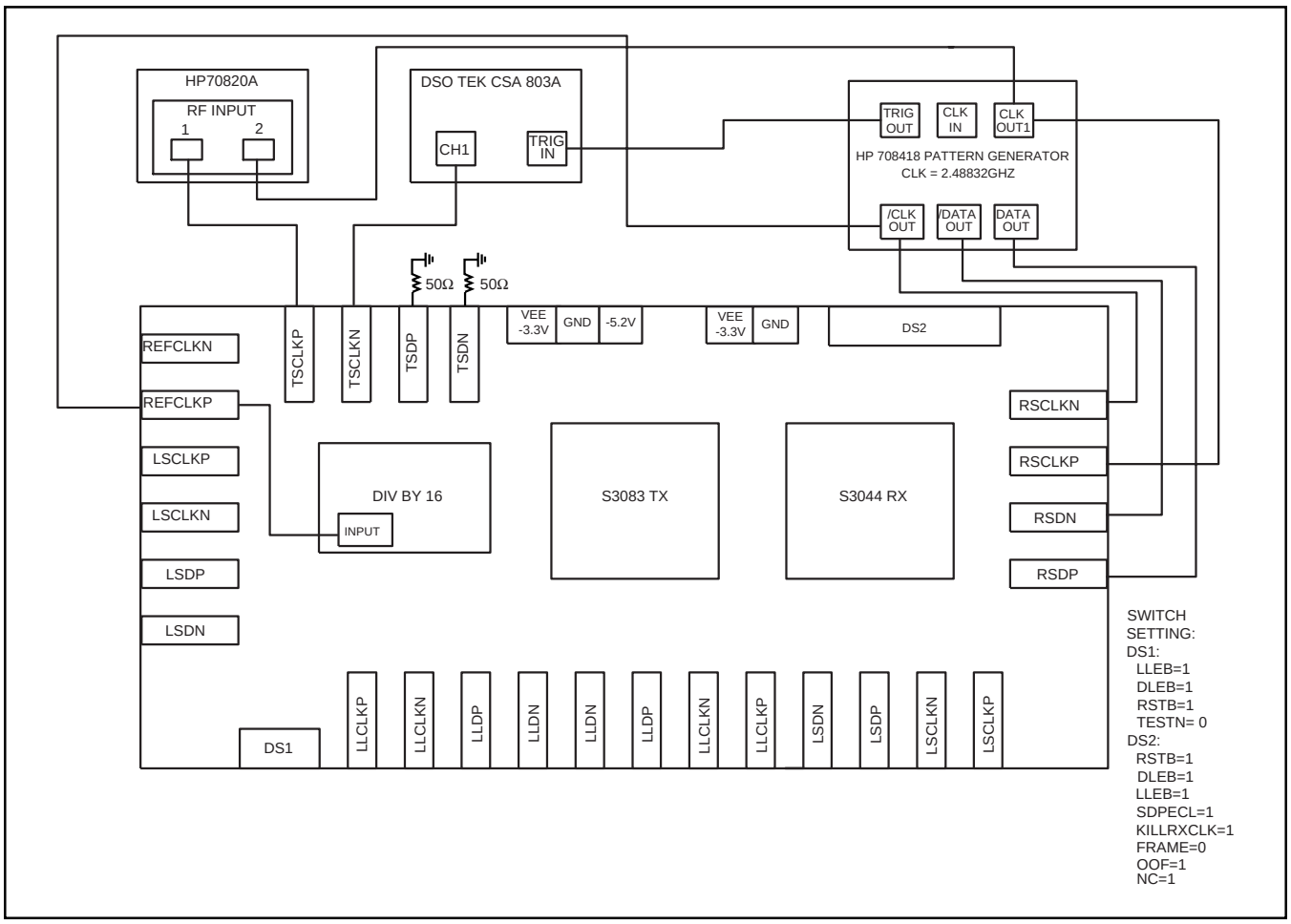


Figure 7 depicts how the S3083/S3044 Evaluation board can be setup for Line Loop Back mode, and shows all of the dip switch settings and the power supply requirements for use with test equipment that utilizes 50 ohms to ground termination.

Figure 7. Line Loopback (LLEB) Test Setup

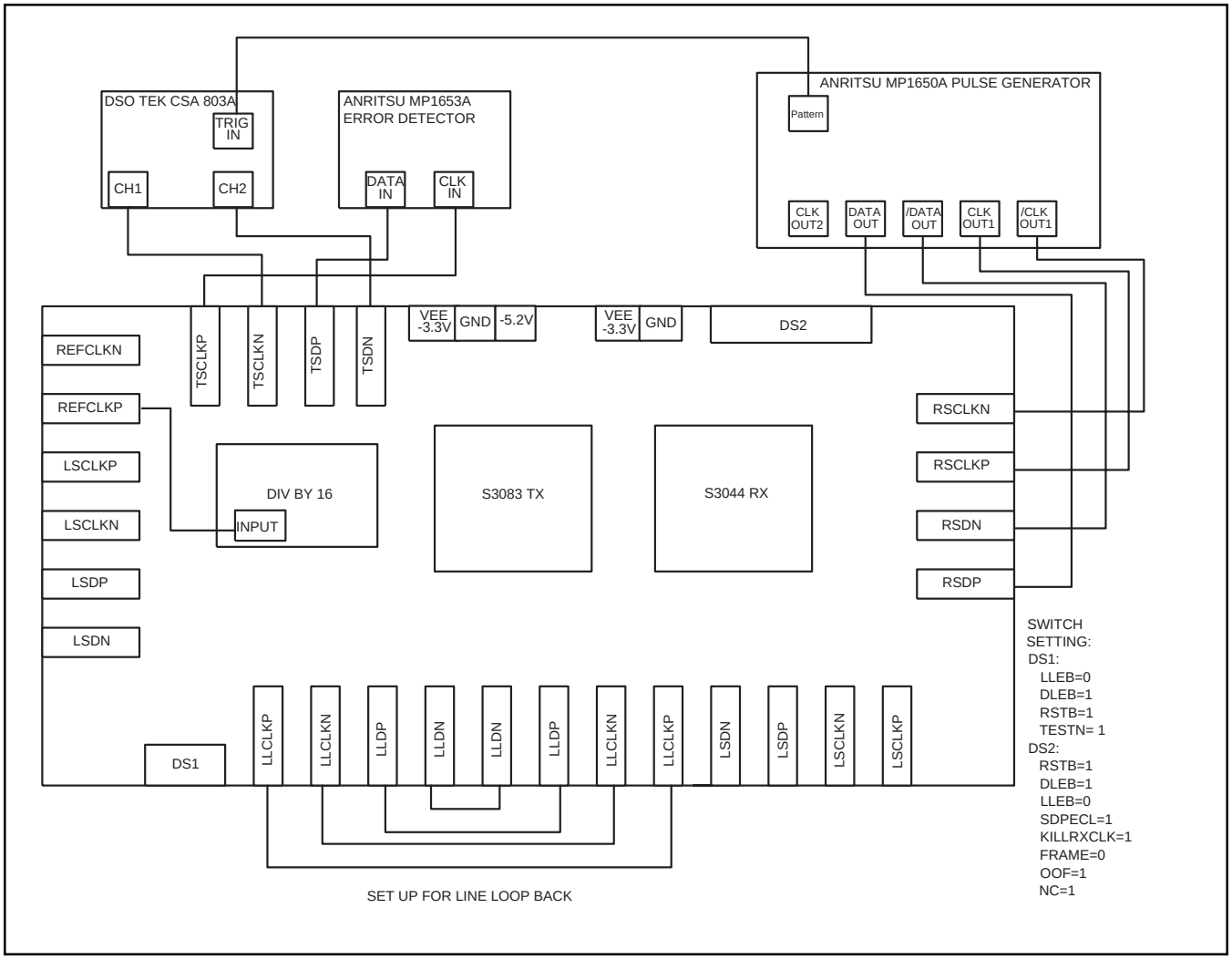


Figure 8 depicts how the S3083/S3044 Evaluation board can be setup for Diagnostic Loop Back mode, and shows all of the dip switch settings and the power supply requirements for use with test equipment that utilizes 50 ohms to ground termination.

Figure 8. Diagnostic Loopback (DLEB) Test Setup

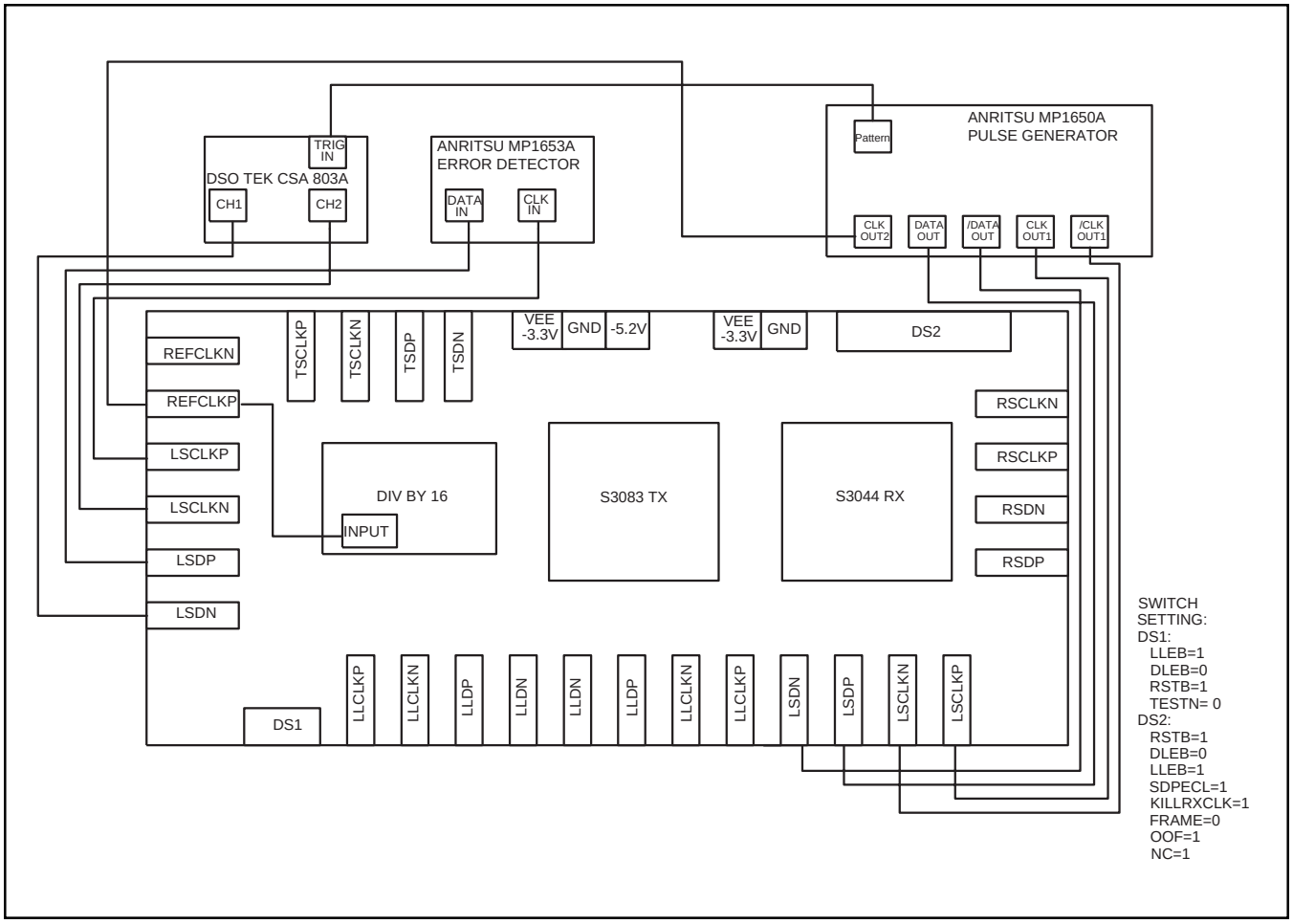
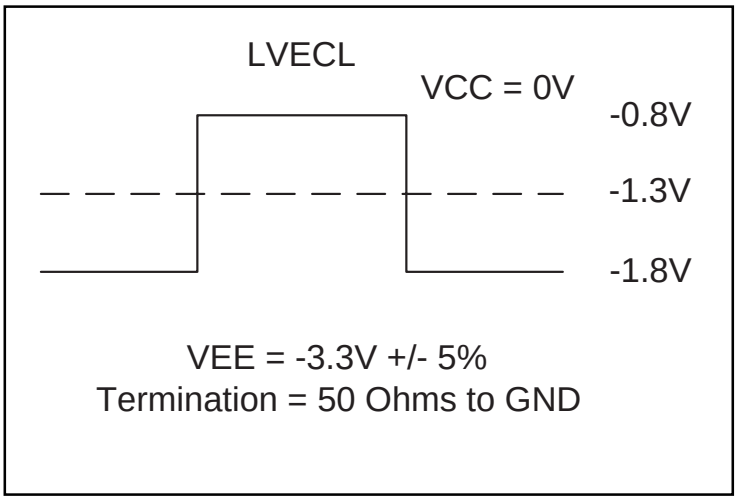


Table 1. Power Connections for DUT and Test Equipment Interface

Power Supply	Nominal Input Voltage	Type of Signal	ECL Output Termination
DUT VCC DUT VEE	0V -3.3V	LVECL	50 Ohms to GND

Figure 9. LVPECL Signal Waveform



ELECTRICAL CONNECTIONS

Power Connections

Terminal posts are provided at the top edge of the board for VEE. The S3083/S3044 Evaluation Board has been configured with ECL I/O. Figure 9 demonstrates the type of input that the S3083/S3044 Evaluation Board requires.

SMA Connectors

SMA connectors are provided for the differential serial data input/output signals and output clock. Additional SMA connectors are provided for an optional differential serial input clock, the external TTL reference clock and the optional external Parallel Input clock.

S3044 SMA Connectors

Loopback Serial Clock [LSCLKP/N] – LVPECL Differential inputs. Clock input from the transmitter that is synchronous with the LSD inputs. This clock is used during local loopback testing to perform the framing and deserialization functions.

Loopback Serial Data [LSDP/N] – LVPECL Differential inputs. Serial data stream connected to the transmitter for loopback testing. These inputs are clocked by the LSCLK inputs.

Line Loopback Clock [LLCLKP/N] – Low swing CML Differential outputs. A buffered version of the RSCLK or LSCLK input.

Line Loopback Data [LLDP/N] – Low swing CML Differential outputs. A retimed version of the incoming data stream [RSD].

Receive Serial Data [RSDP/N] – LVPECL Differential inputs. Serial data inputs of the S3044.

Receive Serial Clock [RSCLKP/N] – LVPECL Differential inputs. These inputs are used to supply a clock input for the RSDP/N.

S3083 SMA Connectors

Loopback Serial Clock [LSCLKP/N] – Low swing CML Differential outputs. Serial clock signals connected to a companion S3044 device for diagnostic loopback purposes. The LSD outputs are updated on the falling edge of the LSCLK.

Loopback Serial Data [LSDP/N] – Low swing CML Differential outputs. Serial data stream connected to a companion S3044 device for diagnostic loopback purposes. The LSD outputs are updated on the falling edge of the LSCLK.

Line Loopback Clock [LLCLKP/N] – LVPECL Differential inputs. Inputs provided from a companion S3044 device. Used to implement a line loopback function in which the receive serial data and clock signals are regenerated and passed through the S3083 transmitter.

Line Loopback Data [LLDP/N] – LVPECL Differential inputs. Inputs provided from a companion S3044 device. Used to implement a line loopback function in which the receive serial data and clock signals are regenerated and passed through the S3083 transmitter.

Transmit Serial Data Out [TSDP/N] – CML Differential outputs. The serial output data stream from the transmitter section of the S3083. The outputs drive 50 ohms to ground terminated instrument inputs.

Transmit Clock Output [TSCLKP/N] – CML Differential outputs. The Transmit serial clock that can be used to re-time the TSDP/N signal. The outputs drive 50 ohms to ground terminated instrument inputs. This clock will be 2.488MHz.

Reference Clock [REFCLKP/N] – LVPECL Differential inputs. These inputs must be provided with a differential level clock of 155.52 MHz.

Parallel I/O Header Terminals

The parallel input (PIN[15:0]) and output (POUT[15:0]) data to and from the S3083/S3044 transceiver are available on a pin header array at the center of the Evaluation board. Ground pin columns are also provided to allow connection with 0.1" grid shielded ribbon cable to parallel data sources and data analyzers.

User selectable jumpers also allow the parallel output data (POUT[7:0]) and the output byte clock (POCLK) to be directly connected to the transmitter parallel data inputs (PIN[7:0]) and the parallel input clock (PICLK). Note: The board must be supplied with an external reference via REFCLKP/N for proper operation.

S3044 Outputs

Parallel Clock [PCLK] — LVPECL output. The word rate output reference from the transmitter PLL. This output is used to coordinate byte-wide transfers via the parallel data bus.

155 MHz Clock Output [155MCK] — LVPECL output. A 155.52 MHz output derived from the S3083 PLL available at the header pin for monitoring.

Frame Pulse [FP] — LVPECL output. Indicates frame boundaries in the incoming data stream (RSDP/N).

Lock Detect [LOCKDET] — LVTTL output. Indicates that the CRU has locked onto the incoming data stream. This signal is set low when the CRU is locked.

Dip Switches

The Evaluation Board is equipped with two DIP switches, to control the static control functions of the on-board devices. For both arrays the OFF (open = “0”) condition of the DIP switch asserts a logic low on the assigned signal, and the ON (closed = “1”) condition asserts a logic high. Figures 5–8 show the particular dip switch settings that are needed for a particular test case.

RSTB Pushbutton Switch — This momentary contact switch controls the master reset of the S3083/S3044.

Please refer to the S3083/S3044 data sheet for details of the specific control functions. Normal mode for this master reset input is normally high. Depressing the switch connects this input to logic zero and resets the S3083/S3044.

Figures 10 through 15 show the layout of the S3083/S3044 Evaluation Board.

Figure 10.

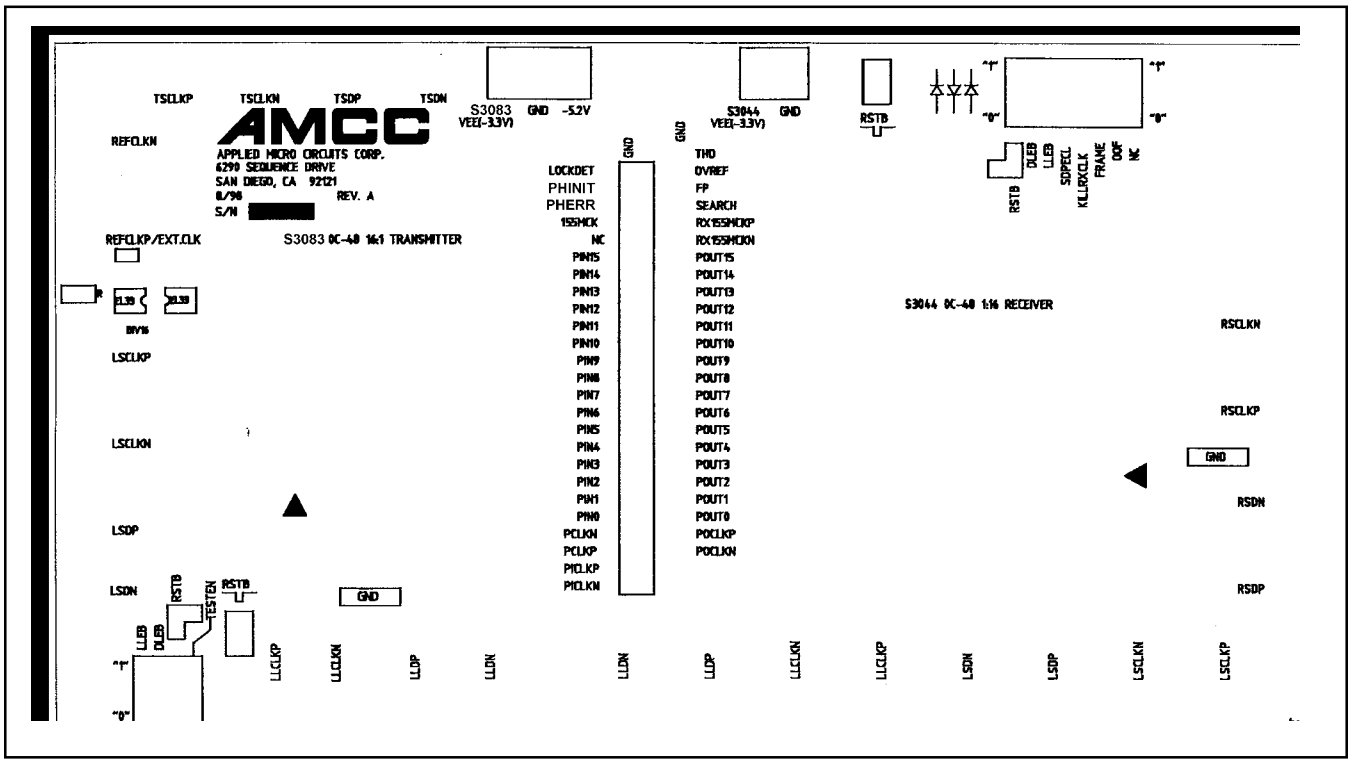


Figure 11.

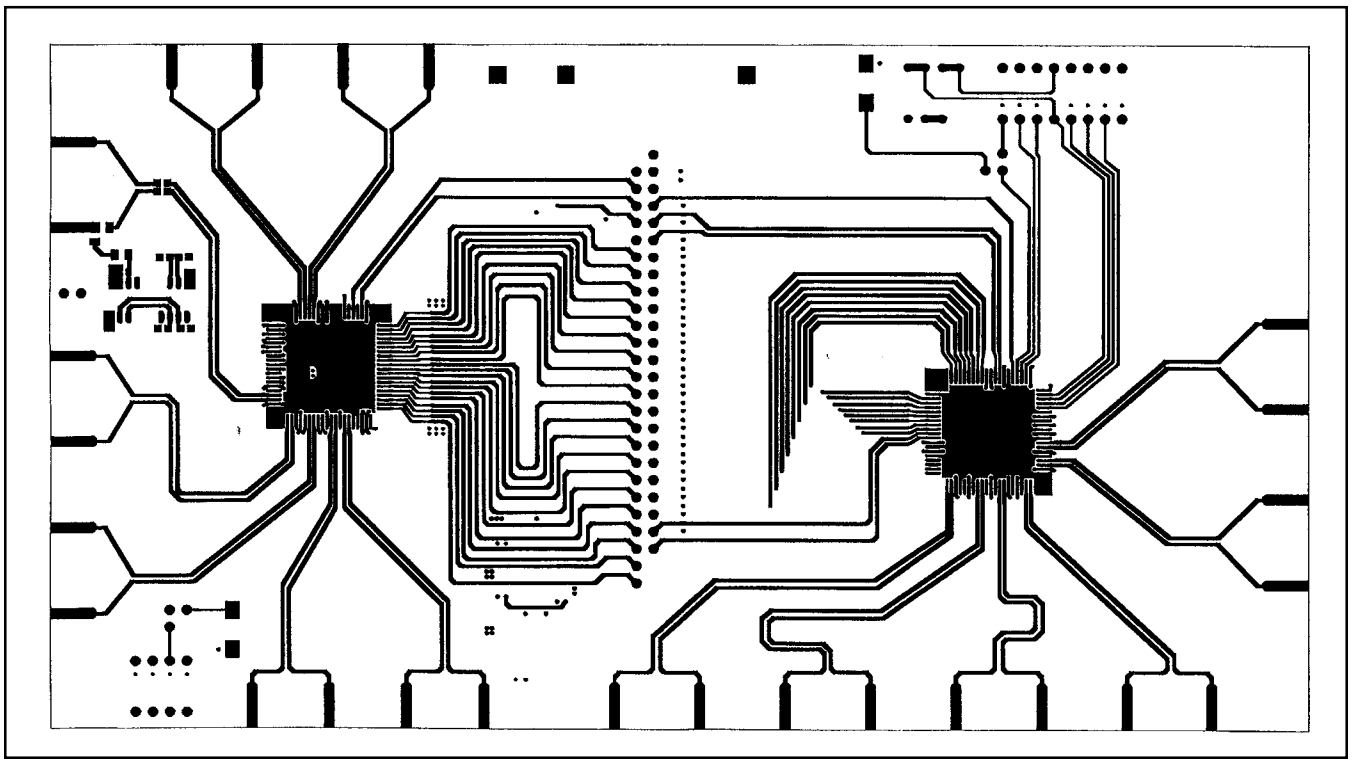


Figure 12.

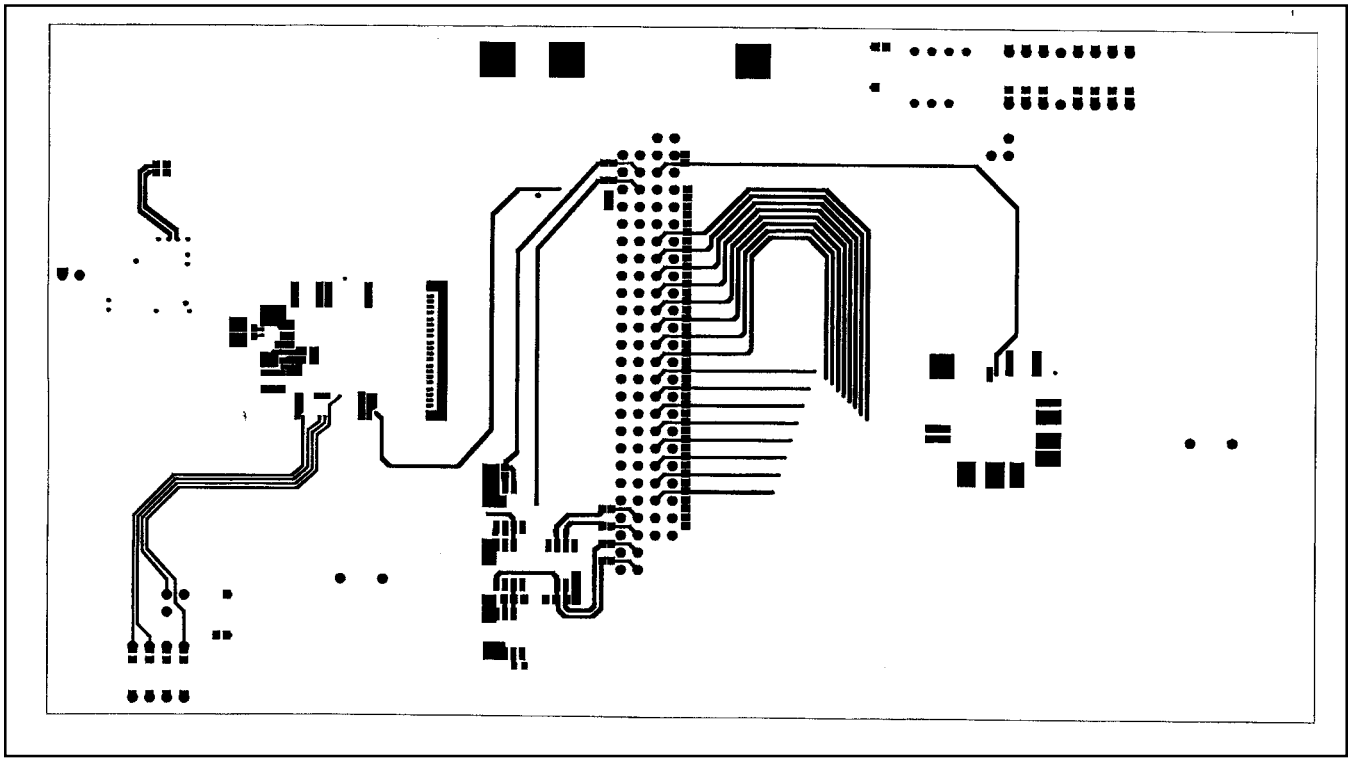


Figure 13.

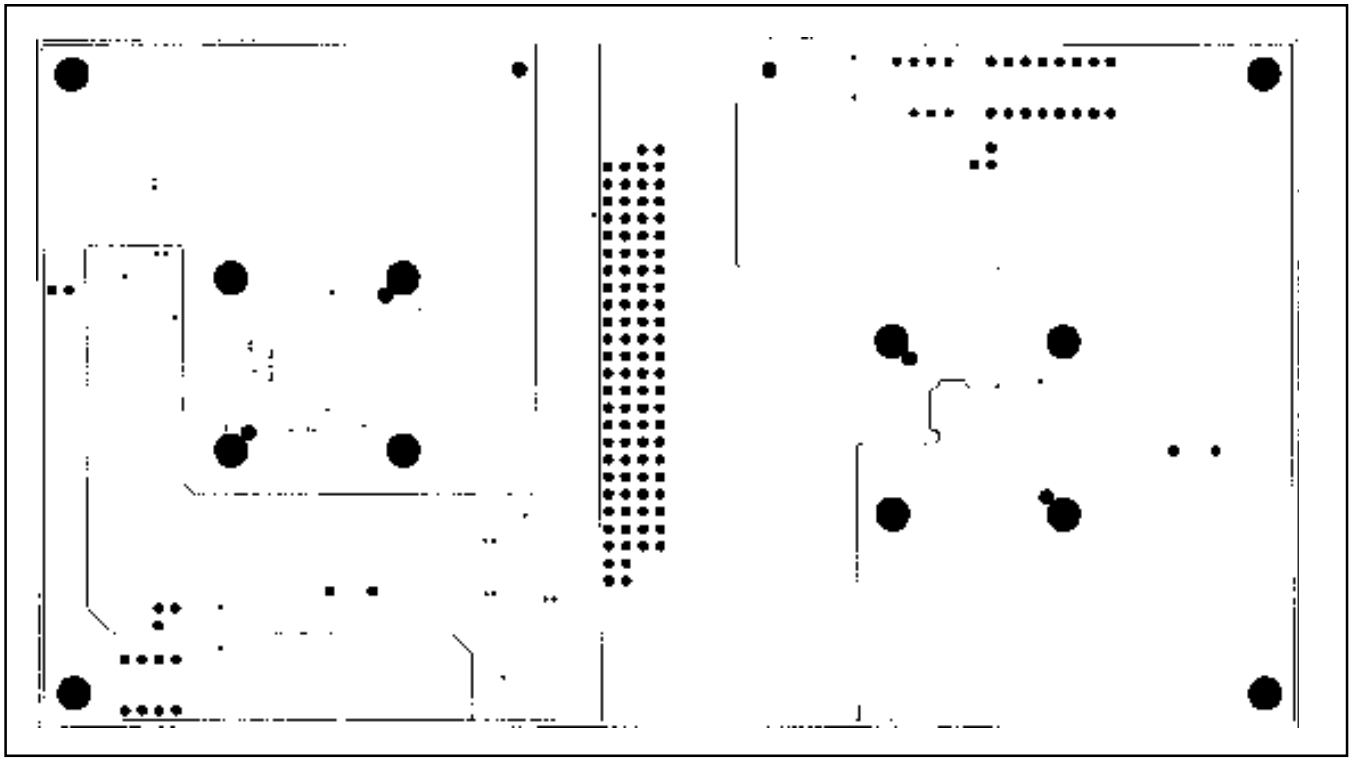


Figure 14.

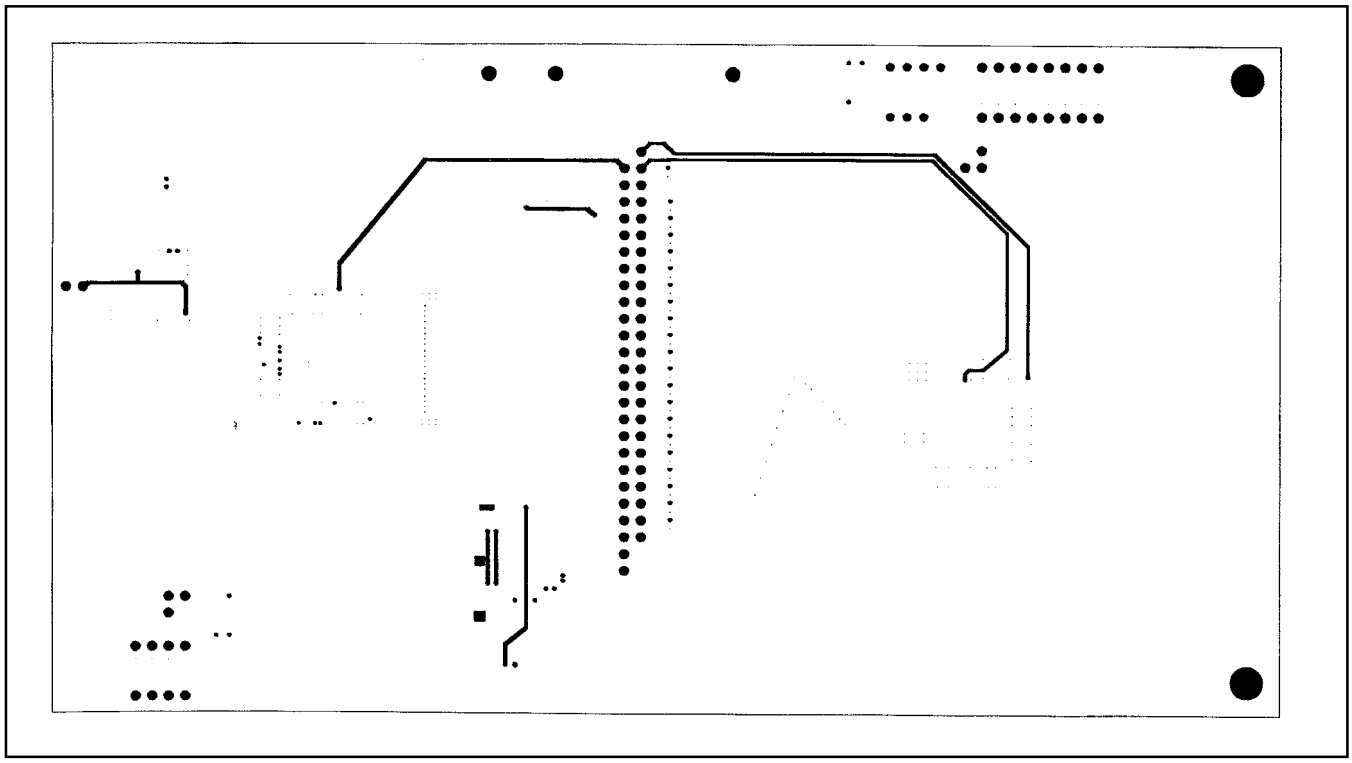
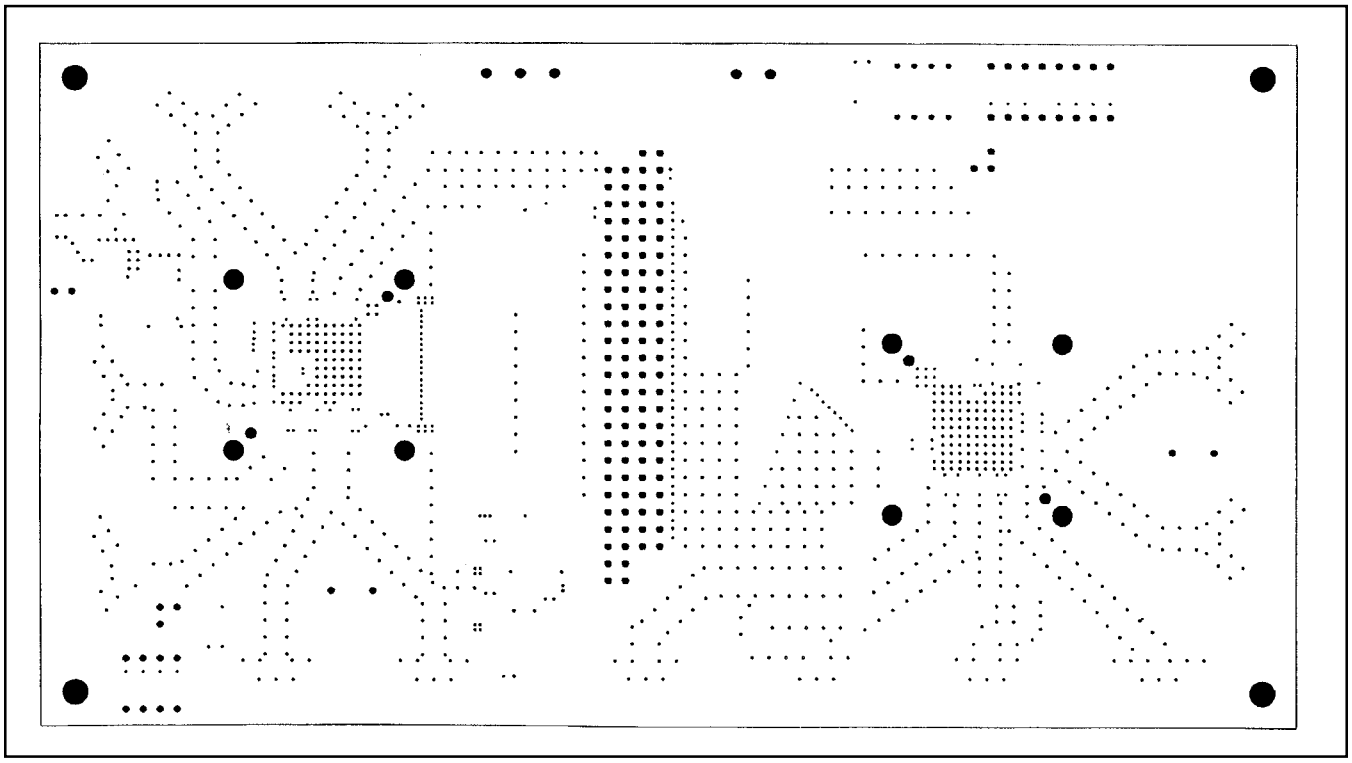
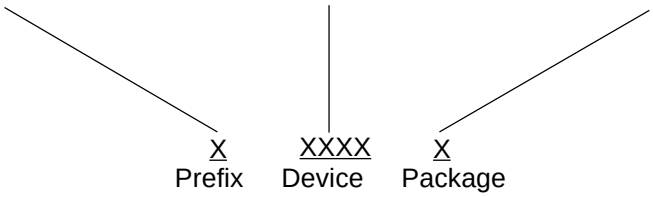


Figure 15.



Ordering Information

PREFIX	DEVICE	PACKAGE
EV – Evaluation Board	3083 3044	QT – 80 PQFP/TEP A – 80 PQFP/TEP



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Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (858) 450-9333 • (800) 755-2622 • Fax: (858) 450-9885
http://www.amcc.com