Preliminary *32K X 8 BIT LOW VOLTAGE CMOS SRAM*

Document Title

32K X 8 BIT LOW VOLTAGE CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
1.0	Initial issue	September 01, 1997	
1.1	Modify 28-pin DIP, SOP and TSOP packages outline dimensions.	January 20, 1998	
1.2	Modify 28-pin SOP and TSOP packages outline drawings and dimensions	June 17, 1998	
1.3	Add -LLU type Change operating voltage Vccmax from 3.3V to 3.6V	April 11, 2001	
1.4	Add Product Family in page 1 Delete I_{CC} item Add I_{CC2}(typ.) I_{CCDR}(typ.) Change I_{SB1}(typ.) I_{CCDR}(max.) Change ordering information from I_{CC1} to I_{CC2}	November 30, 2001	

Preliminary

32K X 8 BIT LOW VOLTAGE CMOS SRAM

Features

- External Operating Voltage: 2.7V to 3.6V
- Access times: 55ns (max.): for VCC = 3.0V to 3.6V
  70ns (max.): for VCC = 2.7V to 3.6V
- Current: Operating (I_{CC1}): -55 series 18mA (typ.)
  -70 series 12mA (typ.)
  Standby (I_{SB1}): 0.05µA (typ.)
- Extended operating temperature range: -40°C to +85°C for -LLU series
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2.0V (min.)
- Available in 28-pin DIP, SOP and TSOP (forward and reverse type) packages

General Description

The A62L256 is a low operating current 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a low power voltage: 2.7V to 3.6V.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
Minimum standby power is drawn by this device when $\overline{CE}$ is at a high level, independent of the other input levels.
Data retention is guaranteed at a power supply voltage as low as 2.0V.

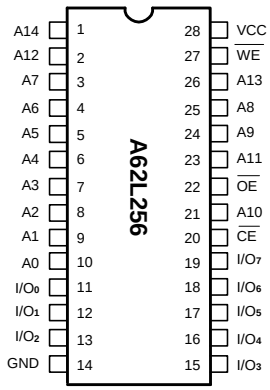
Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I_{CCDR}, Typ.)	Standby (I_{SB1}, Typ.)	Operating (I_{CC2}, Typ.)	
A62L256	-40°C ~ +85°C	2.7V~3.6V	55ns / 70ns	0.02µA	0.05µA	1mA	28L DIP 28L SOP 28L TSOP

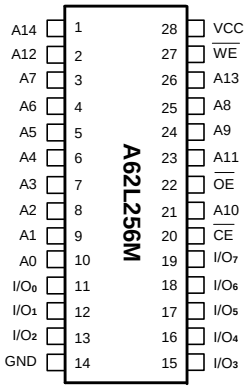
1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

Pin Configurations

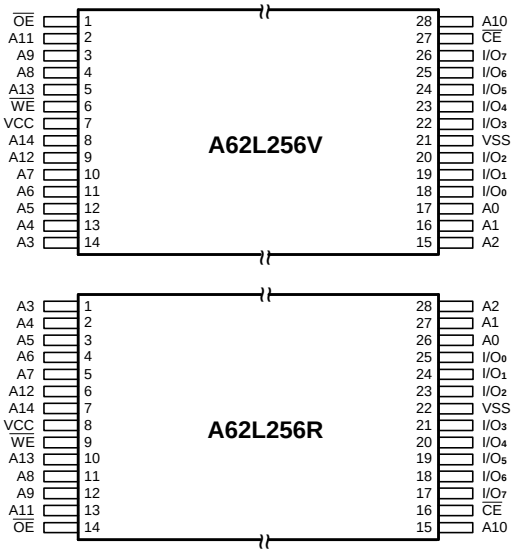
■ DIP



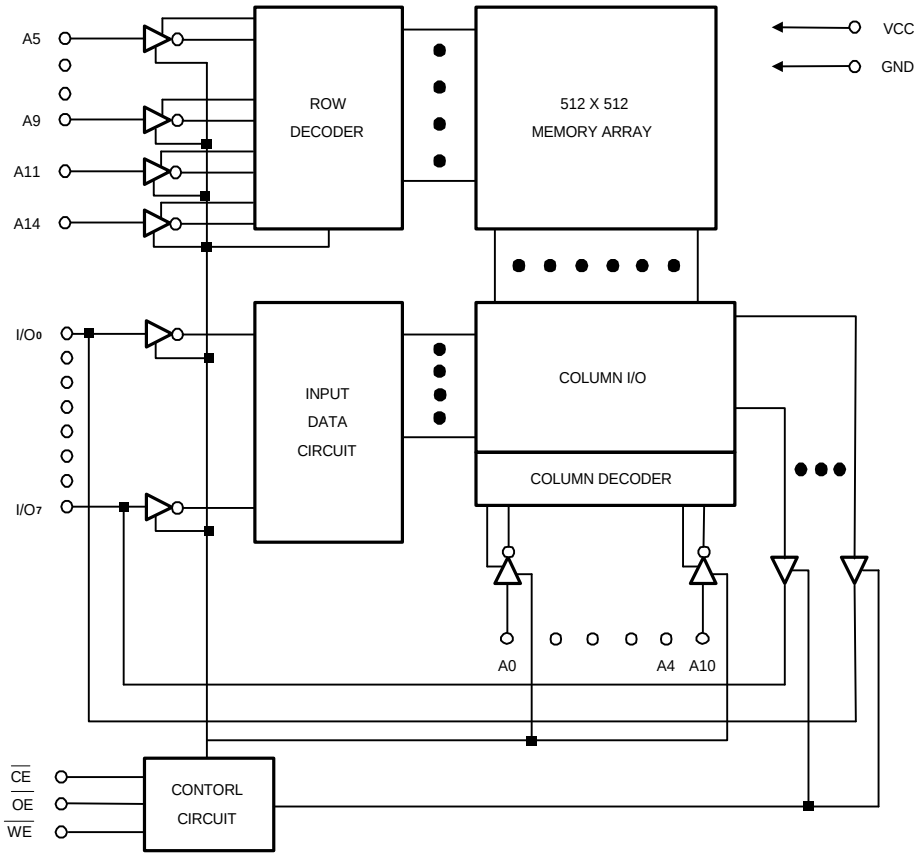
■ SOP



■ TSOP



Block Diagram



Pin Descriptions - DIP/SOP

Pin No.	Symbol	Description
1-10, 21, 23-26	A0 - A14	Address Input
11-13, 15-19	I/O0 - I/O7	Data Input/Output
14	GND	Ground
20	$\overline{CE}$	Chip Enable
22	$\overline{OE}$	Output Enable
27	$\overline{WE}$	Write Enable
28	VCC	Power Supply

Pin Description-TSOP

Pin No.	Symbol	Description
1	$\overline{OE}$	Output Enable
2-5, 8-17, 28	A0 - A14	Address Input
7	VCC	Power Supply
6	$\overline{WE}$	Write Enable
18-20, 22-26	I/O0 - I/O7	Data Input/Output
21	GND	Ground
27	$\overline{CE}$	Chip Enable

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C or -40°C to +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	VCC * 0.7	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	0	+0.3	V

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +3.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C or -40ºC to +85ºC, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	A62L256-55LL/55LLU			A62L256-70LL/70LLU			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
$\|I_{LI}\|$	Input Leakage Current	-	-	1	-	-	1	µA	V_{IN} = GND to VCC
$\|I_{LO}\|$	Output Leakage Current	-	-	1	-	-	1	µA	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC1}	Dynamic Operating Current	-	*18	25	-	**12	20	mA	Min. Cycle, Duty = 100% $\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA
I_{CC2}	Dynamic Operating Current	-	1	3	-	1	3	mA	$\overline{CE}$ = V_{IL}, V_{IH} = VCC V_{IL} = 0V, f = 1 MHz $I_{I/O}$ = 0 mA

Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.

* Testing condition : T_A = 25°C, VCC = 3.0V, Cycle Time = 55 ns
** Testing condition : T_A = 25°C, VCC = 3.0V, Cycle Time = 70 ns

DC Electrical Characteristics (continued)

Symbol	Parameter	A62L256-55LL/70LL			A62L256-55LLU/70LLU			Unit	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{SB}	Supply Current Standby Power	-	-	50	-	-	50	µA	$\overline{CE}$ = V_{IH}
I_{SB1}		-	0.05	2	-	0.05	5	µA	$\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	-	0.3	-	-	0.3	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	VCC - 0.3	-	-	VCC - 0.3	-	-	V	I_{OH} = -1.0mA

Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X: H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

These parameters are sampled and not 100% tested.

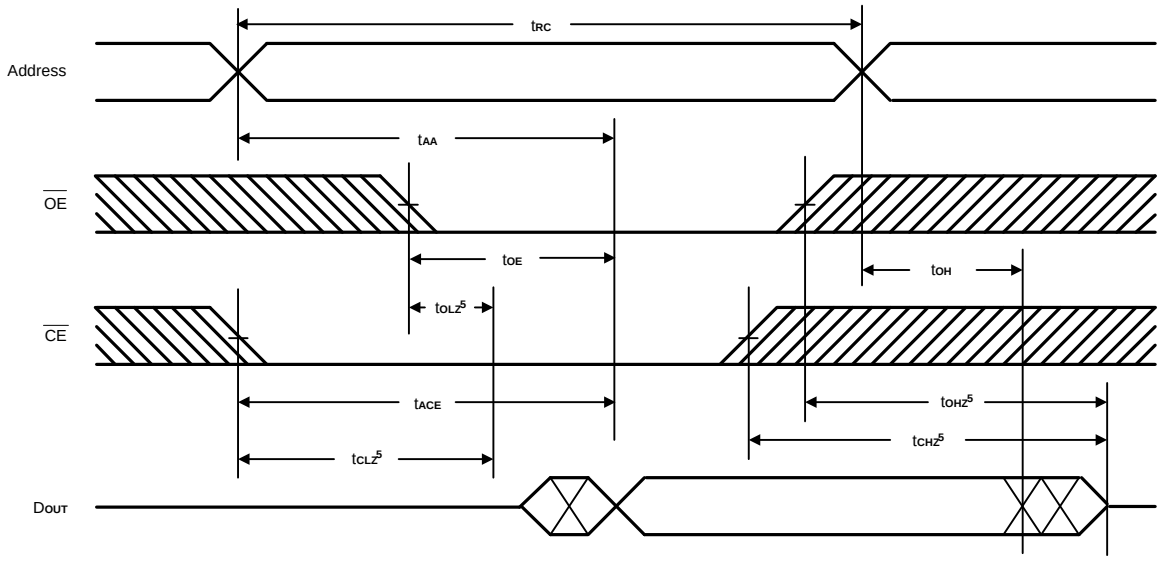
AC Characteristics (T_A = 0°C to +70°C or -40°C to +85°C)

Symbol	Parameter	A62L256-55LL/LLU (VCC = 3.0V to 3.6V)		A62L256-70LL/LLU (VCC = 2.7V to 3.6V)		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55	-	70	-	ns
t_{AA}	Address Access Time	-	55	-	70	ns
t_{ACE}	Chip Enable Access Time	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid	-	30	-	35	ns
t_{CLZ}	Chip Enable to Output in Low Z	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{CHZ}	Chip Disable to Output in High Z	-	20	-	25	ns
t_{OHZ}	Output Disable to Output in High Z	-	20	-	25	ns
t_{OH}	Output Hold from Address Change	5	-	10	-	ns
Write Cycle						
t_{WC}	Write Cycle Time	55	-	70	-	ns
t_{CW}	Chip Enable to End of Write	50	-	60	-	ns
t_{AS}	Address Set up Time	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	50	-	60	-	ns
t_{WP}	Write Pulse Width	40	-	50	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	-	25	-	25	ns
t_{DW}	Data to Write Time Overlap	25	-	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	ns

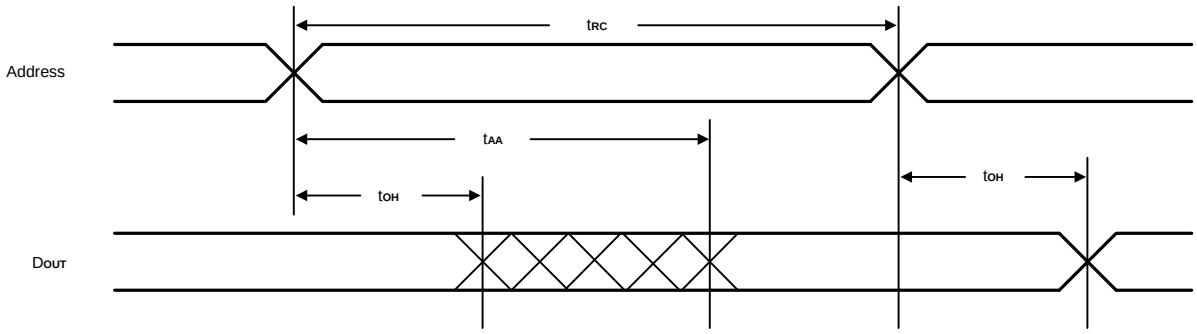
Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1 (1)

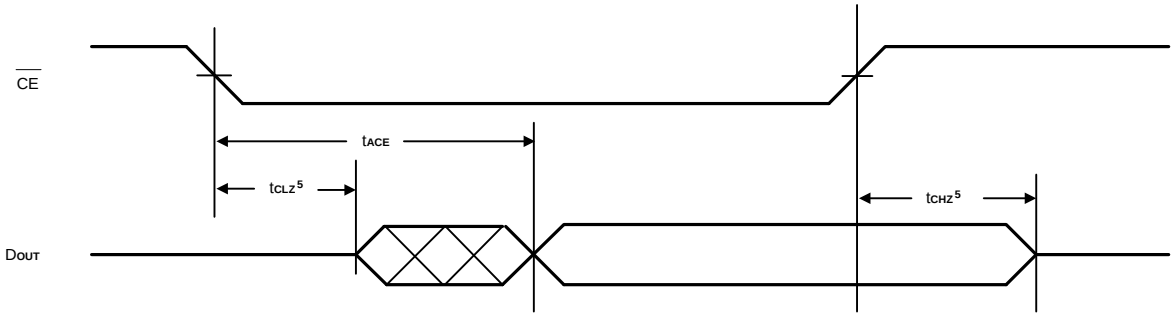


Read Cycle 2 (1, 2, 4)



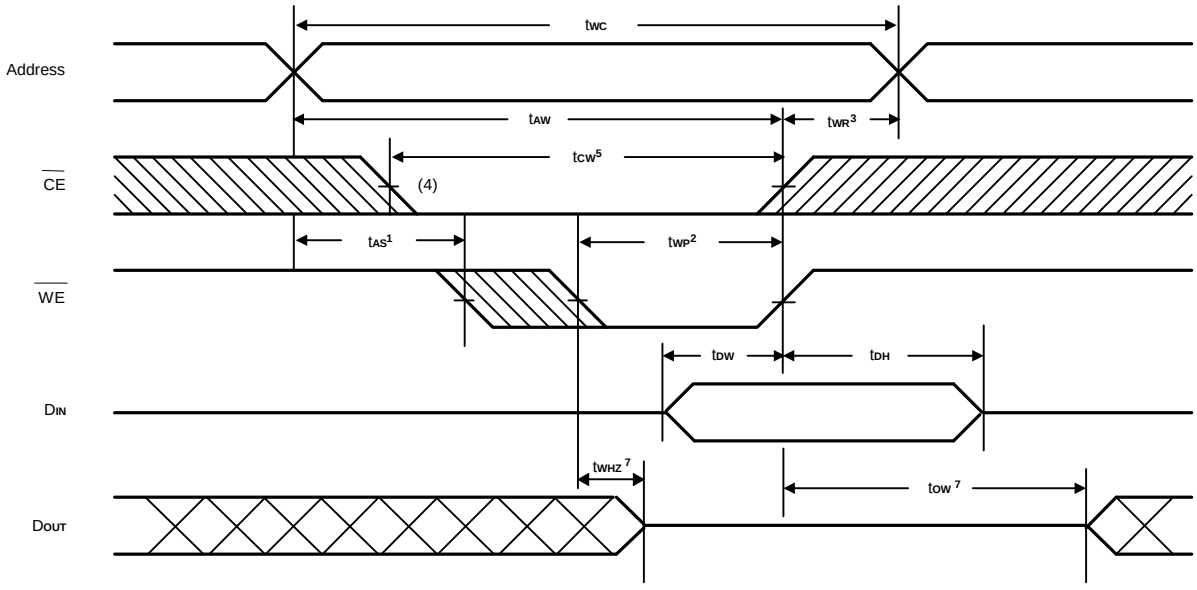
Timing Waveforms (continued)

Read Cycle 3 (1, 3, 4)



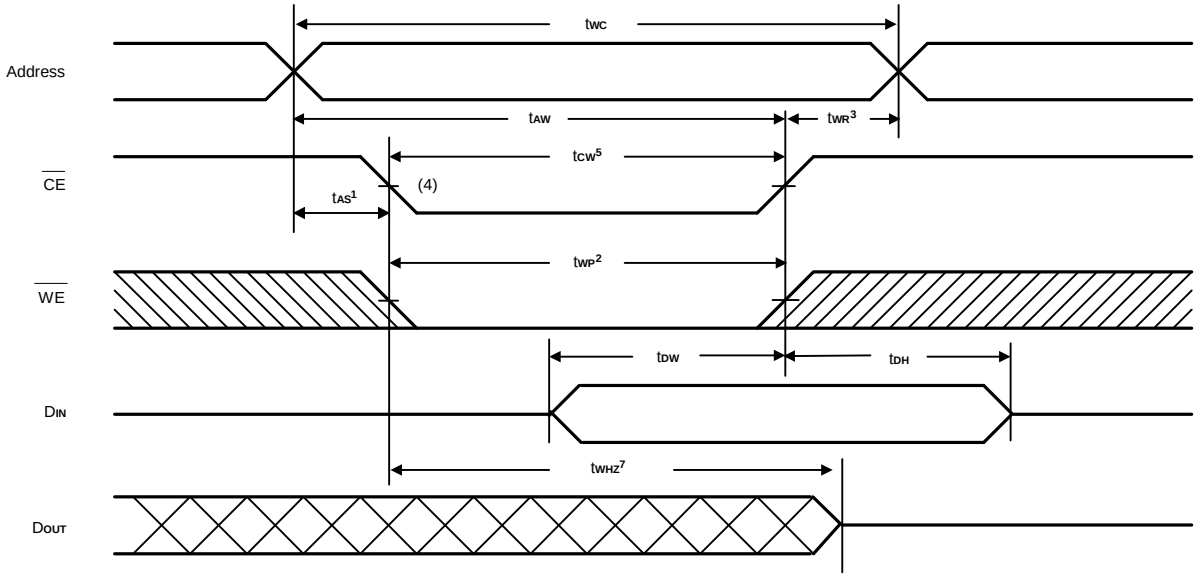
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Write Cycle 1 (6)
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2 (6)
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured form the earliest of $\overline{CE}$ or $\overline{WE}$ going high to the end of the Write cycle.
4. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of Write.
6. $\overline{OE}$ level is high or low.
7. Transition is measured ±500mV from steady. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V, VCC
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	VCC/2
Output Load	See Figure 1

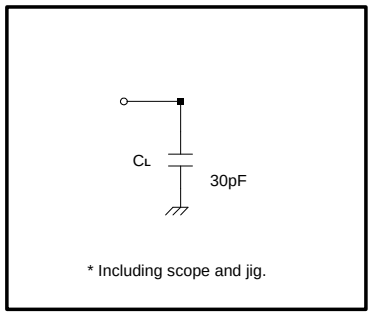


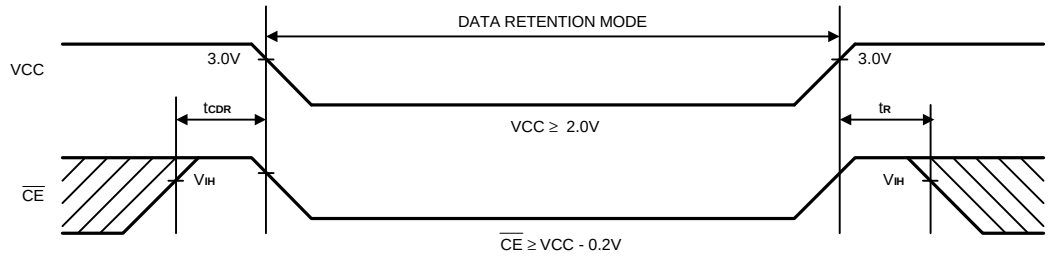
Figure 1. Output Load

Data Retention Characteristics (T_A = 0°C to 70°C or -40°C to +85°C)

Symbol	Parameter		Min.	Typ.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention		2.0	-	3.6	V	$\overline{CE}$ ≥ VCC - 0.2V
I_{CCDR}	Data Retention Current	LL-version	-	0.02	0.5	µA	VCC = 2V, $\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
		LLU-version	-	0.02	2		
t_{CDR}	Chip Disable to Data Retention Time		0		-	ns	See Retention Waveform
t_R	Operation Recovery Time		t_{RC}		-	ns	

Typical values are measured at T_A = 25°C.

Low VCC Data Retention Waveform



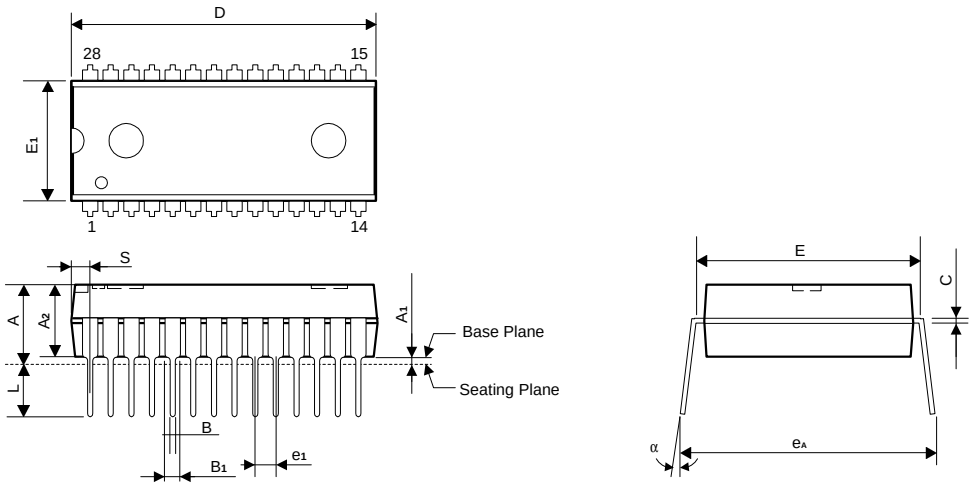
Ordering Information

Part No.	Access Time (ns)	Operating Current (I_{CC2}) Max. (mA)	Standby Current (I_{SB1}) Max. (μA)	Package
A62L256-55LL	55	3	2	28L DIP
A62L256M-55LL		3	2	28L SOP
A62L256V-55LL		3	2	28L TSOP (Forward)
A62L256R-55LL		3	2	28L TSOP (Reverse)
A62L256-70LL	70	3	2	28L DIP
A62L256M-70LL		3	2	28L SOP
A62L256V-70LL		3	2	28L TSOP (Forward)
A62L256R-70LL		3	2	28L TSOP (Reverse)
A62L256-55LLU	55	3	5	28L DIP
A62L256M-55LLU		3	5	28L SOP
A62L256V-55LLU		3	5	28L TSOP (Forward)
A62L256R-55LLU		3	5	28L TSOP (Reverse)
A62L256-70LLU	70	3	5	28L DIP
A62L256M-70LLU		3	5	28L SOP
A62L256V-70LLU		3	5	28L TSOP (Forward)
A62L256R-70LLU		3	5	28L TSOP (Reverse)

Package Information

P-DIP 28L Outline Dimensions

unit: inches/mm



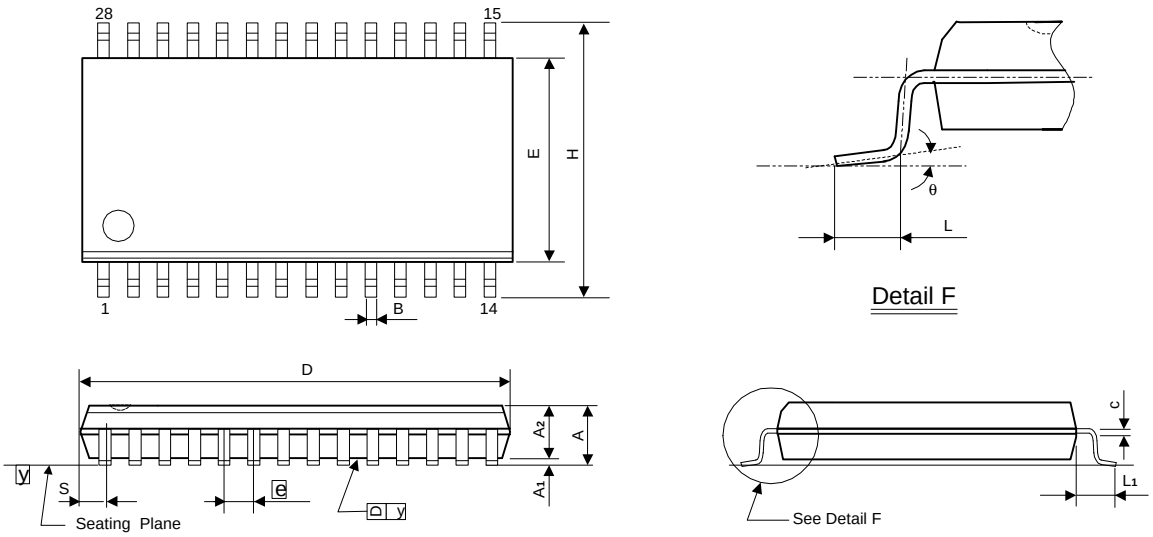
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.210	-	-	5.33
A_1	0.010	-	-	0.25	-	-
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
C	0.008	0.010	0.014	0.20	0.25	0.36
D	-	1.460	1.470	-	37.08	37.34
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0°	-	15°	0°	-	15°
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	-	-	0.090	-	-	2.29

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E_1 does not include resin fins.
3. Dimension S includes end flash.

Package Information

SOP (W.B.) 28L Outline Dimensions

unit: inches/mm



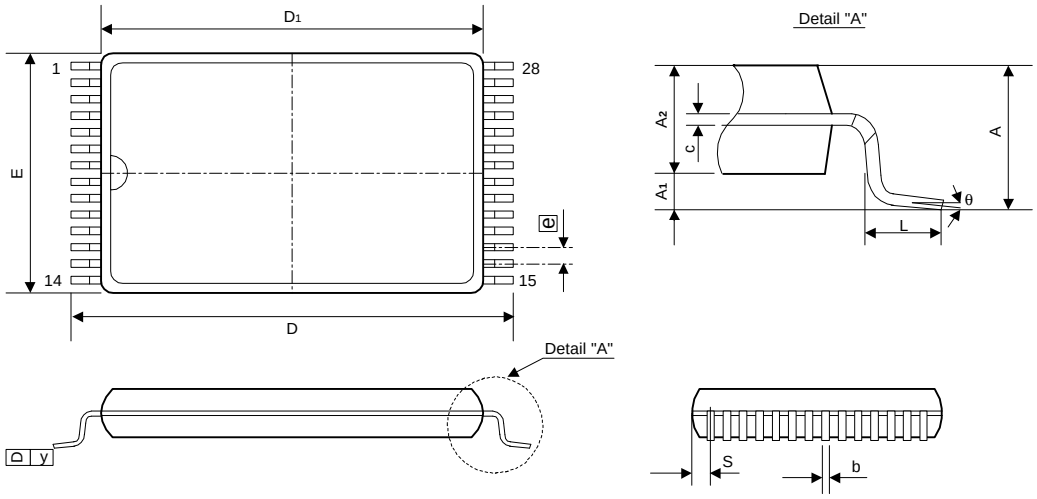
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.112	-	-	2.85
A_1	0.004	-	-	0.10	-	-
A_2	0.093	0.098	0.103	2.36	2.49	2.62
B	0.014	0.016	0.020	0.36	0.41	0.51
C	0.008	0.010	0.012	0.20	0.25	0.30
D	-	0.713	0.728	-	18.11	18.49
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_1	0.059	0.067	0.075	1.50	1.70	1.91
S	-	-	0.047	-	-	1.19
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

TSOP 28L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A_1	0.002	-	-	0.05	-	-
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.005	-	0.008	0.12	-	0.21
E	0.311	0.315	0.319	7.90	8.00	8.10
L	0.012	0.020	0.028	0.30	0.50	0.70
D	0.520	0.528	0.536	13.20	13.40	13.60
D_1	0.461	0.465	0.469	11.70	11.80	11.90
e	0.022 BSC			0.55 BSC		
S	0.017 TYP			0.425 TYP		
y	-	-	0.004	-	-	0.10
θ	0°	-	5°	0°	-	5°

Notes:
1. The maximum value of dimension D_1 includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.