Document Title

128K X 8 BIT LOW VOLTAGE CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	September 5, 2000	Preliminary
0.1	Change max. power supply voltage from 3.3V to 3.6V Change min. V_{IH} from 2.2V to 2.4V Add feature “Interfaces directly with 3.3V typ. logic chip” Remove A62S7308B-10S/SI part	October 12, 2000	
0.2	Add A62S7308B-55S/SI part Change Input Pulse Levels from 0.4V~2.4V to 0V~3.0V in AC Test Conditions table	March 9, 2001	

Preliminary

128K X 8 BIT LOW VOLTAGE CMOS SRAM

Features

- Power supply range: 2.7V to 3.6V
- Access times: 55ns (max.): for VCC = 3.0V to 3.6V
  70ns (max.): for VCC = 2.7V to 3.6V
- Current:
  A62S7308B-S series: Operating: 30mA (max.)
  Standby: 5µA (max.)
  A62S7308B-SI series: Operating: 30mA (max.)
  Standby: 10µA (max.)
- Extended operating temperature range: -25°C to 85°C for -SI series
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 32-pin SOP, TSOP, sTSOP (8X 13.4mm) forward type and 36-ball Mini BGA (6X8) packages
- Interfaces directly with 3.3V typ. logic chip

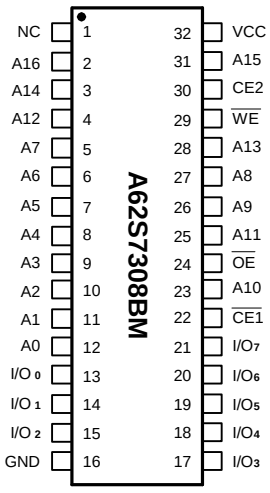
General Description

The A62S7308B is a low operating current 1048,576-bit static random access memory organized as 131,072 words by 8 bits and operates on a low power supply voltage from 2.7V to 3.6V.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

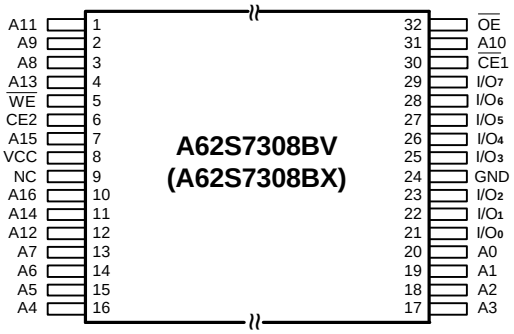
Two chip enable inputs are provided for power down and a device enable and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

■ **SOP**



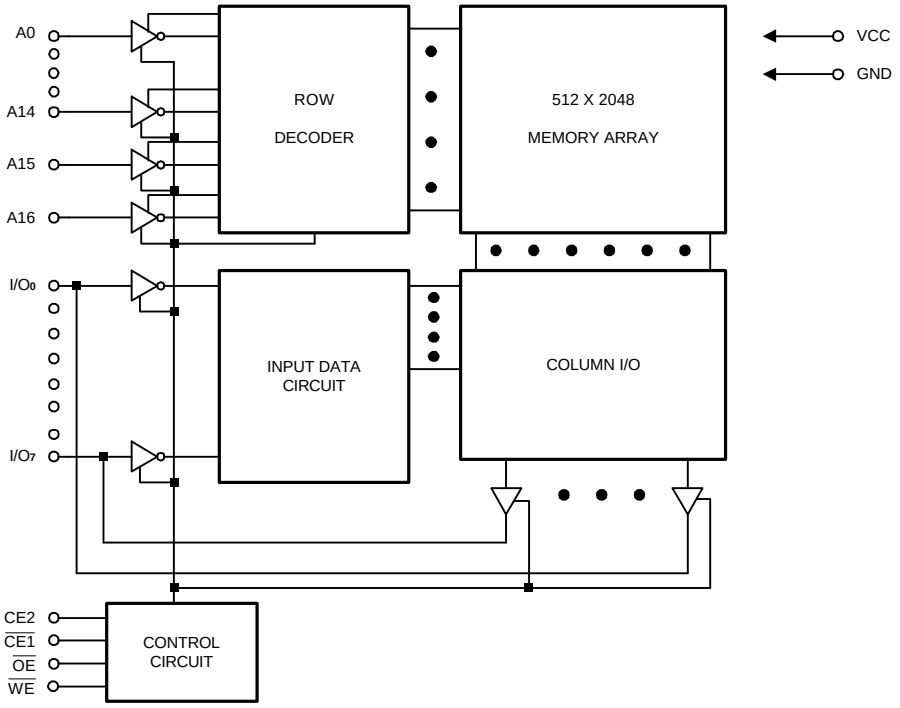
■ **TSOP/(sTSOP) (forward type)**



■ **Mini BGA (6X8) Top View**

	1	2	3	4	5	6
A	A0	A1	CE2	A3	A6	A8
B	I/O_4	A2	$\overline{WE}$	A4	A7	I/O_0
C	I/O_5		NC	A5		I/O_1
D	VSS					VCC
E	VCC					VSS
F	I/O_6		NC	NC		I/O_2
G	I/O_7	$\overline{OE}$	$\overline{CE1}$	A16	A15	I/O_3
H	A9	A10	A11	A12	A13	A14

Block Diagram



Pin Descriptions - SOP

Pin No.	Symbol	Description
1	NC	No Connection
2 - 12, 23, 25 - 28, 31	A0 - A16	Address Inputs
13 - 15, 17 - 21	I/O0 - I/O7	Data Inputs/Outputs
16	GND	Ground
22	$\overline{CE1}$	Chip Enable 1
24	$\overline{OE}$	Output Enable
29	$\overline{WE}$	Write Enable
30	CE2	Chip Enable 2
32	VCC	Power Supply

Pin Description - TSOP/sTSOP

Pin No.	Symbol	Description
1 - 4, 7, 10 - 20, 31	A0 - A16	Address Inputs
5	$\overline{WE}$	Write Enable
6	CE2	Chip Enable 2
8	VCC	Power Supply
9	NC	No Connection
21 - 23, 25 - 29	I/O0 - I/O7	Data Inputs/Outputs
24	GND	Ground
30	$\overline{CE1}$	Chip Enable 1
32	$\overline{OE}$	Output Enable

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C or -25°C to 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to + 4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . -25°C to + 85°C
Storage Temperature, Tstg . .. . -55°C to + 125°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = 0°C to + 70°C or -25°C to 85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	A62S7308B-55S/70S		A62S7308B-55SI/70SI		Unit	Conditions
		Min.	Max.	Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	-	1	µA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	3	-	3	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	30	-	30	mA	Min. Cycle, Duty = 100% $\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0mA
I_{CC2}	Dynamic Operating Current	-	3	-	3	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IH} = VCC , V_{IL} = 0V F = 1MHz, $I_{I/O}$ = 0mA

DC Electrical Characteristics (continued)

Symbol	Parameter	A62S7308B-55S/70S		A62S7308B-55SI/70SI		Unit	Conditions
		Min.	Max.	Min.	Max.		
I_{SB}	Standby Power Supply Current	-	0.3	-	0.3	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		-	5	-	10	µA	CE2 ≤ 0.2V, or $\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V
V_{OL}	Output Low Voltage	-	0.4	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.4	-	2.4	-	V	I_{OH} = -1.0mA

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

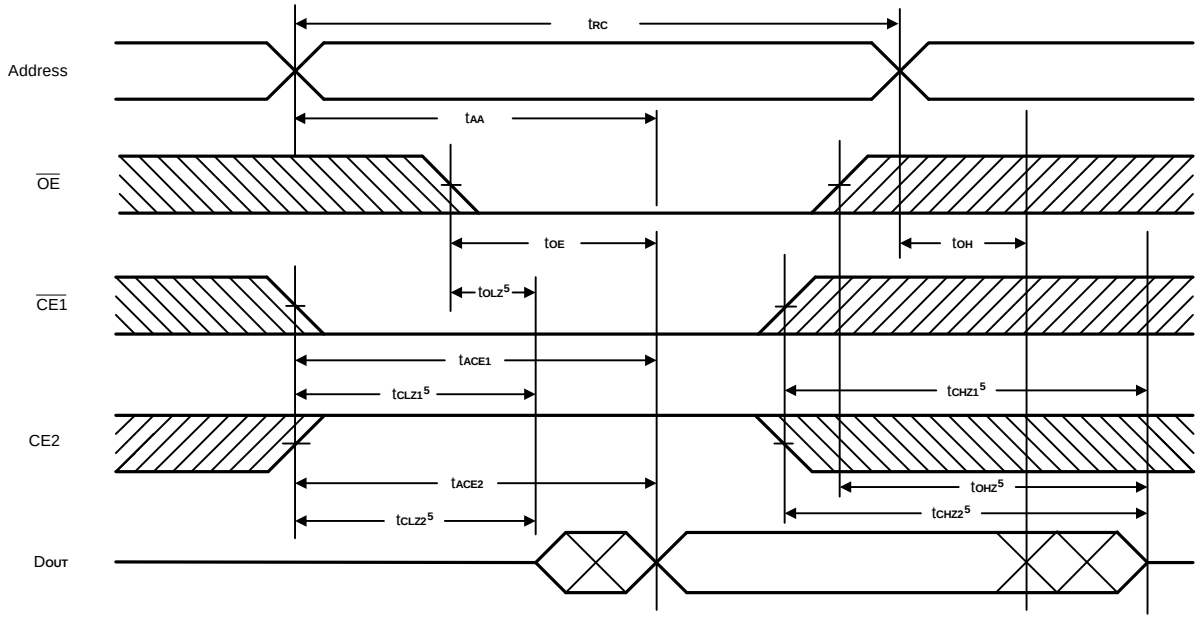
AC Characteristics (T_A = 0°C to + 70°C or -25°C to 85°C)

Symbol	Parameter		A62S7308B-55S/SI (VCC = 3.0V to 3.6V)		A62S7308B-70S/SI (VCC = 2.7V to 3.6V)		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{RC}	Read Cycle Time		55	-	70	-	ns
t_{AA}	Address Access Time		-	55	-	70	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1}$	-	55	-	70	ns
t_{ACE2}		CE2	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid		-	30	-	35	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	10	-	10	-	ns
t_{CLZ2}		CE2	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z		10	-	5	-	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	0	20	0	25	ns
t_{CHZ2}		CE2	0	20	0	25	ns
t_{OHZ}	Output Disable to Output in High Z		0	20	0	25	ns
t_{OH}	Output Hold from Address Change		5	-	10	-	ns
Write Cycle							
t_{WC}	Write Cycle Time		55	-	70	-	ns
t_{CW}	Chip Enable to End of Write		50	-	60	-	ns
t_{AS}	Address Setup Time		0	-	0	-	ns
t_{AW}	Address Valid to End of Write		50	-	60	-	ns
t_{WP}	Write Pulse Width		40	-	50	-	ns
t_{WR}	Write Recovery Time		0	-	0	-	ns
t_{WHZ}	Write to Output in High Z		0	25	0	30	ns
t_{DW}	Data to Write Time Overlap		25	-	30	-	ns
t_{DH}	Data Hold from Write Time		0	-	0	-	ns
t_{OW}	Output Active from End of Write		5	-	5	-	ns

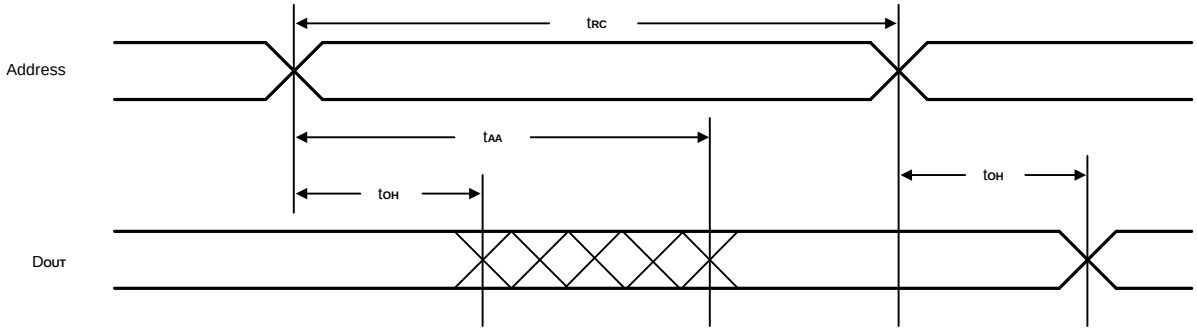
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1 (1)

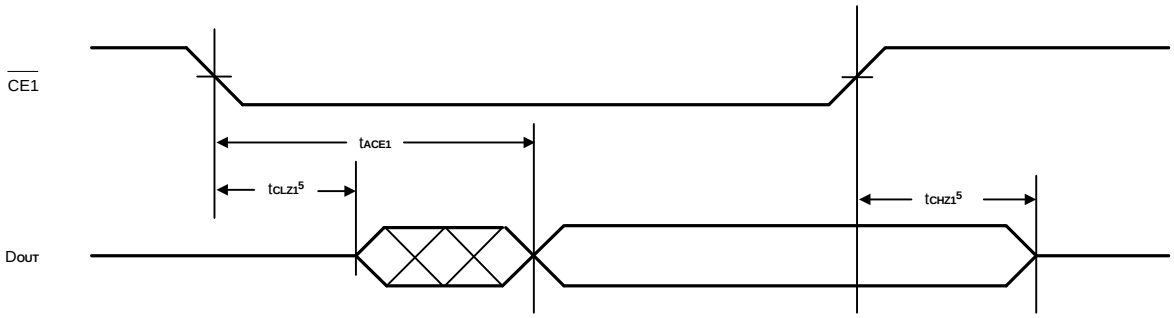


Read Cycle 2 (1, 2, 4)

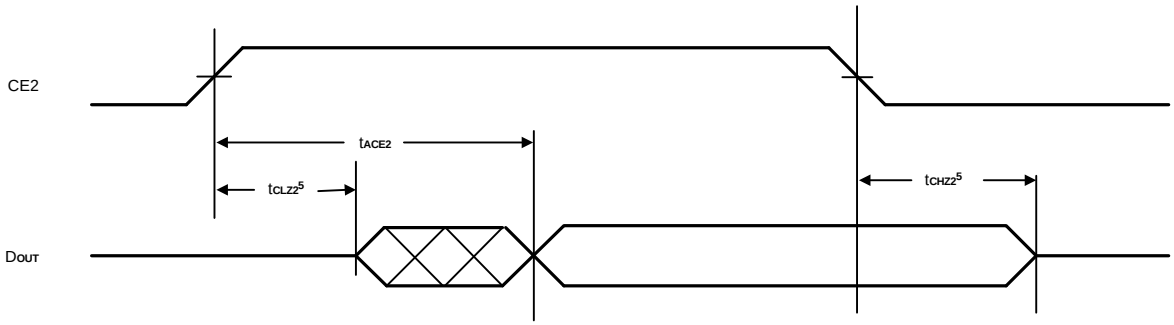


Timing Waveforms (continued)

Read Cycle 3 (1, 3, 4, 6)



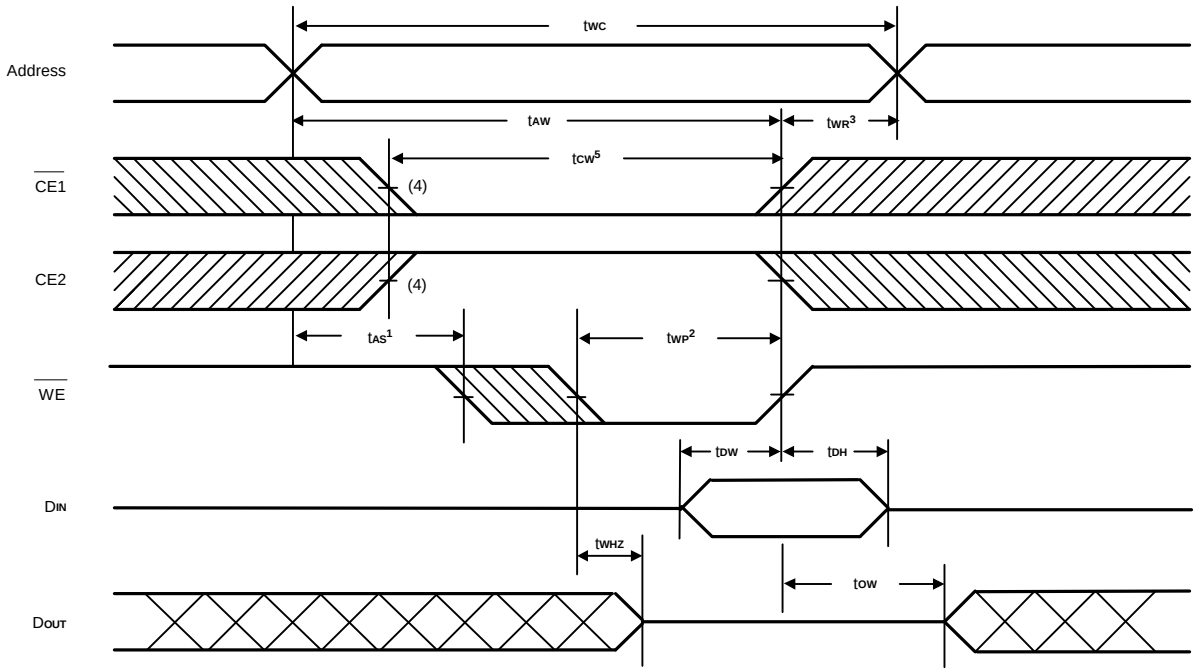
Read Cycle 4 (1, 4, 7, 8)



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

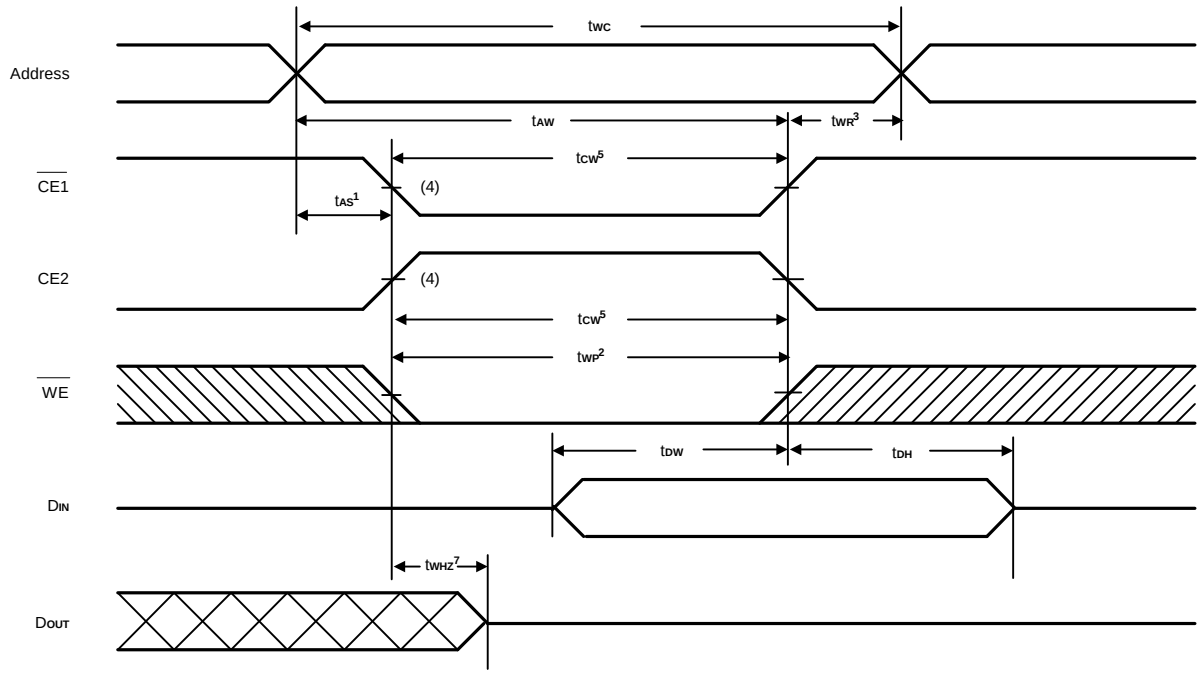
Timing Waveforms (continued)

Write Cycle 1[6]
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2[6]
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

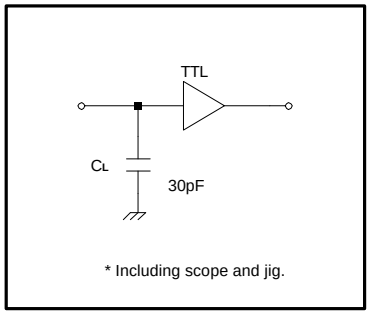


Figure 1. Output Load

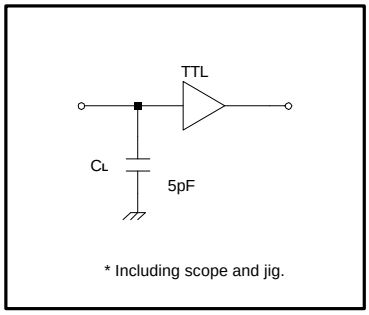


Figure 2. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OHZ}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{WHZ}, and t_{OW}

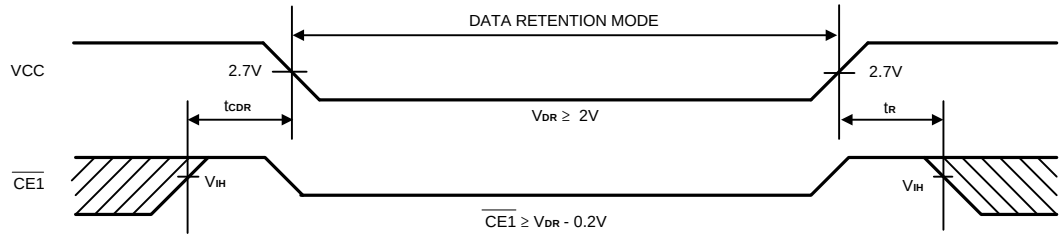
Data Retention Characteristics (T_A = 0°C to + 70°C or -25°C to 85°C)

Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention		2.0	3.6	V	CE2 ≤ 0.2V, or { $\overline{CE1}$ ≥ VCC - 0.2V, CE2 ≥ VCC - 0.2V
I_{CCDR}	Data Retention Current	S-Version	-	2*	µA	VCC = 2.0V, CE2 ≤ 0.2V, or { $\overline{CE1}$ ≥ VCC - 0.2V CE2 ≥ VCC - 0.2V
		SI-Version	-	5**		
t_{CDR}	Chip Disable to Data Retention Time		0	-	ns	See Retention Waveform
t_R	Operation Recovery Time		t_{RC}	-	ns	

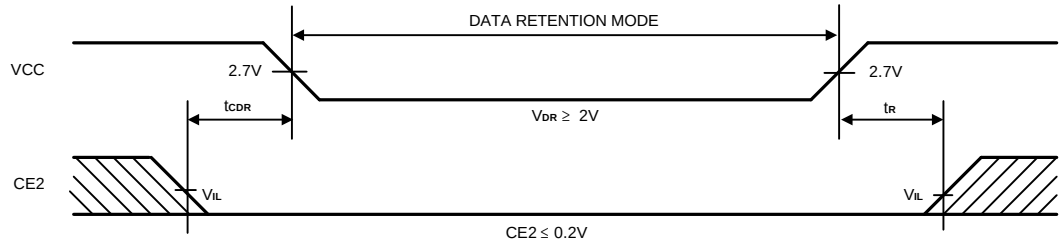
* A62S7308B-55S/70S I_{CCDR}: Max. 1µA at T_A = 0°C to + 40°C

** A62S7308B-55SI/70SI I_{CCDR}: Max. 1µA at T_A = 0°C to + 40°C

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)



Low VCC Data Retention Waveform (2) (CE2 Controlled)



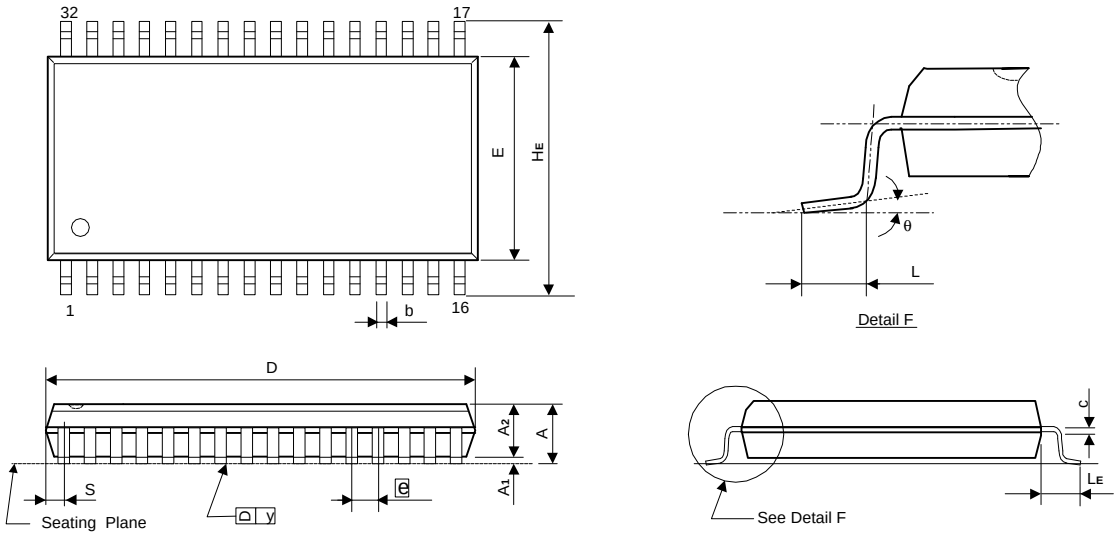
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (μA)	Package
A62S7308BM-55S	55	30	5	32L SOP
A62S7308BM-55SI			10	32L SOP
A62S7308BV-55S			5	32L TSOP
A62S7308BV-55SI			10	32L TSOP
A62S7308BX-55S			5	32L sTSOP
A62S7308BX-55SI			10	32L sTSOP
A62S7308BG-55S			5	36B Mini BGA
A62S7308BG-55SI			10	36B Mini BGA
A62S7308BM-70S	70	30	5	32L SOP
A62S7308BM-70SI			10	32L SOP
A62S7308BV-70S			5	32L TSOP
A62S7308BV-70SI			10	32L TSOP
A62S7308BX-70S			5	32L sTSOP
A62S7308BX-70SI			10	32L sTSOP
A62S7308BG-70S			5	36B Mini BGA
A62S7308BG-70SI			10	36B Mini BGA

Package Information

SOP (W.B.) 32L Outline Dimensions

unit: inches/mm



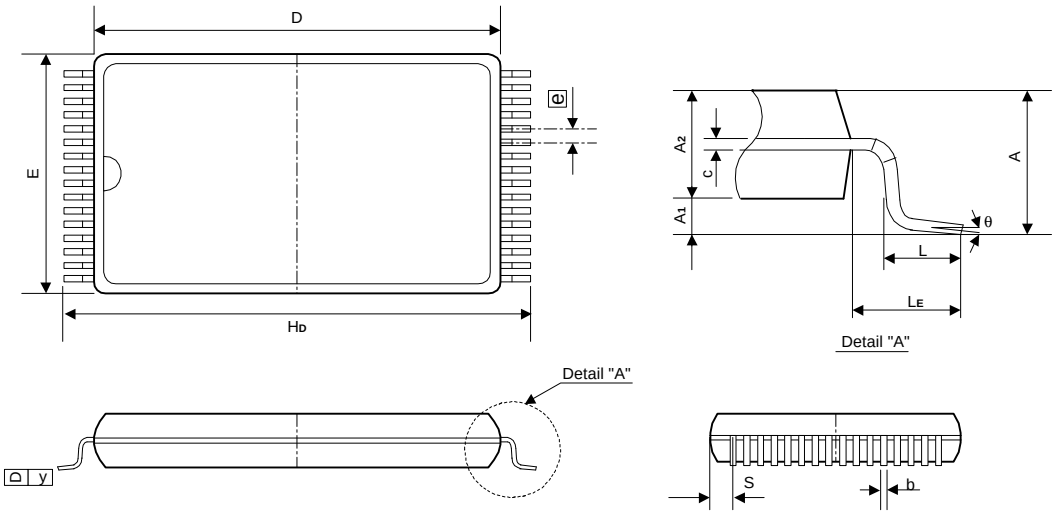
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A_1	0.004	-	-	0.10	-	-
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	-	0.805	0.817	-	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.566	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	-	-	0.036	-	-	0.91
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.11	-	0.20
D	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.315	0.319	-	8.00	8.10
e	0.020 BSC			0.50 BSC		
HD	0.779	0.787	0.795	19.80	20.00	20.20
L	0.016	0.020	0.024	0.40	0.50	0.60
LE	-	0.032	-	-	0.80	-
S	-	-	0.020	-	-	0.50
y	-	-	0.003	-	-	0.08
θ	0°	-	5°	0°	-	5°

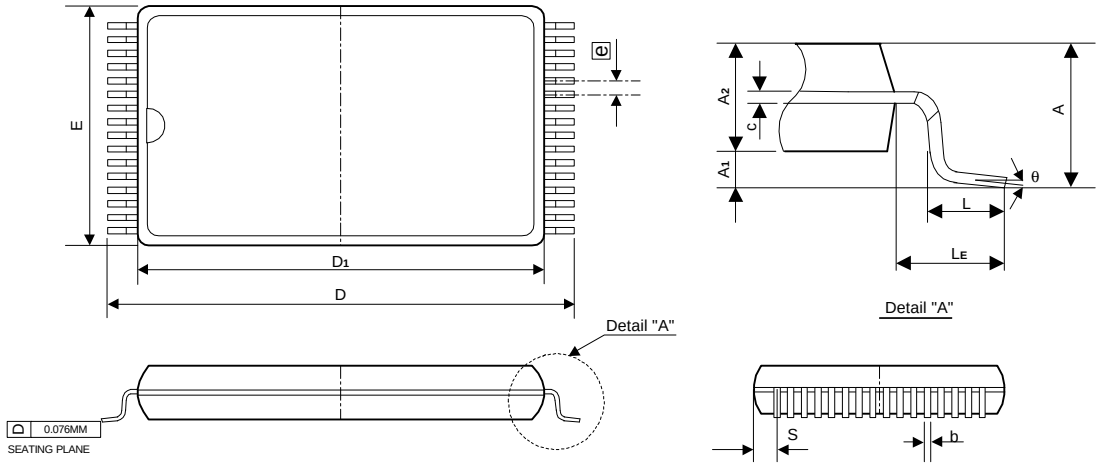
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

sTSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.049	-	-	1.25
A_1	0.002	-	-	0.05	-	-
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.0056	0.0059	0.0062	0.142	0.150	0.158
E	0.311	0.315	0.319	7.90	8.00	8.10
e	0.020 TYP			0.50 TYP		
D	0.520	0.528	0.535	13.20	13.40	13.60
D_1	0.461	0.465	0.469	11.70	11.80	11.90
L	0.012	0.020	0.028	0.30	0.50	0.70
L_E	0.0275	0.0315	0.0355	0.700	0.800	0.900
S	0.0109 TYP			0.278 TYP		
θ	0°	3°	5°	0°	3°	5°

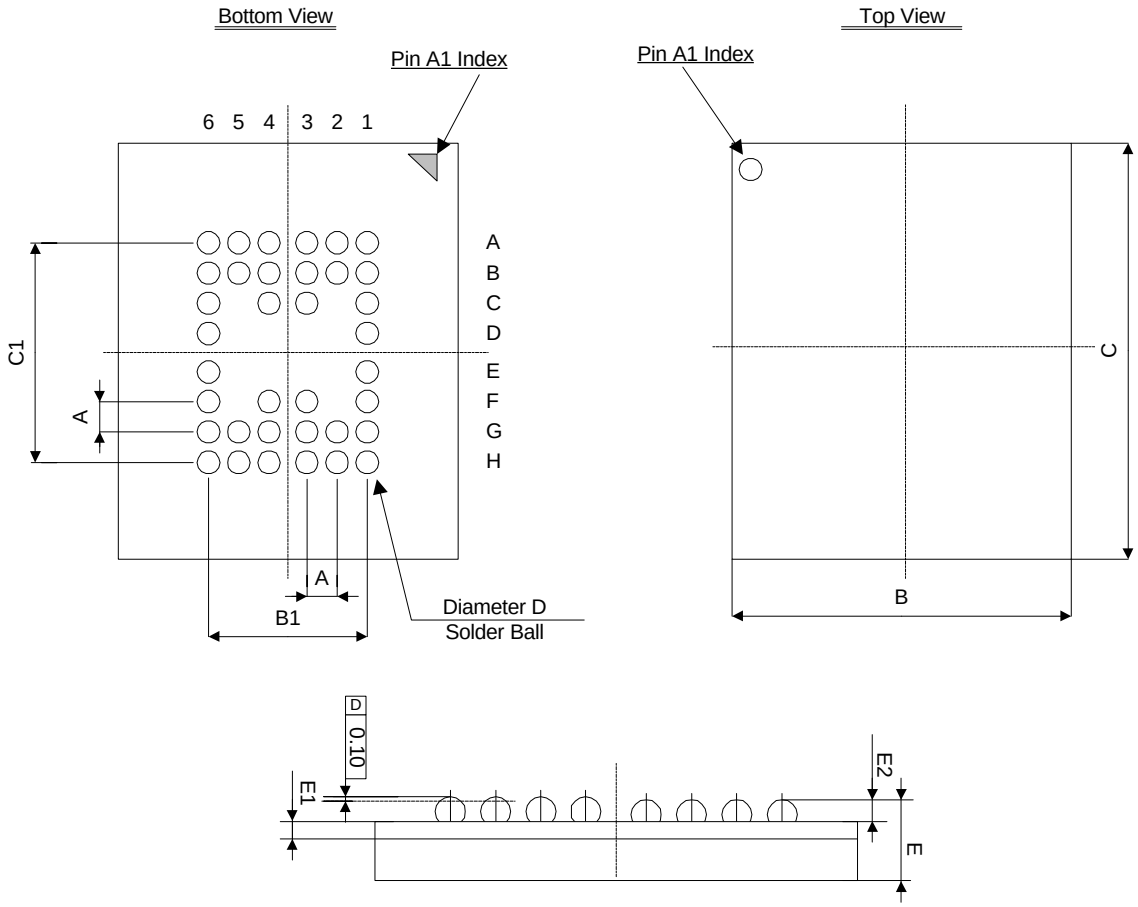
Notes:

1. The maximum value of dimension D_1 includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

Package Information

Mini BGA 6X8 (36 BALLS) Outline Dimensions

unit : millimeter(mm)



Symbol	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	1.00	1.10	1.20
E1	-	0.36	-
E2	-	0.22	-