Document Title

512K X 16 BIT LOW VOLTAGE CMOS SRAM

Revision History

Rev. No.	History	Issue Date	Remark
0.2	Add Product Family and 55ns specification	March 20, 2002	Preliminary

LP62S16512-T Series

Preliminary — 512K X 16 BIT LOW VOLTAGE CMOS SRAM

Features

- Operating voltage: 2.7V to 3.6V
- Access times: 55/70 ns (max.)
- Current:
  Very low power version: Operating: 50mA (max.)
  Standby: 20µA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Data retention voltage: 2.0V (min.)
- Available in 48-ball CSP (8×10mm) packages

General Description

The LP62S16512-T is a low operating current 8,388,608-bit static random access memory organized as 524,288 words by 16 bits and operates on low power voltage from 2.7V to 3.6V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.
Two chip enable input is provided for POWER-DOWN, device enable. Two byte enable inputs and an output enable input are included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2.0V.

Product Family

Product Family	Operating Temperature	VCC Range	Speed	Power Dissipation			Package Type
				Data Retention (I_{CCDR}, Typ.)	Standby (I_{SB1}, Typ.)	Operating (I_{CC2}, Typ.)	
LP62S16512	-40°C ~ +85°C	2.7V~3.6V	55ns / 70ns	0.3µA	0.5µA	4mA	48 CSP

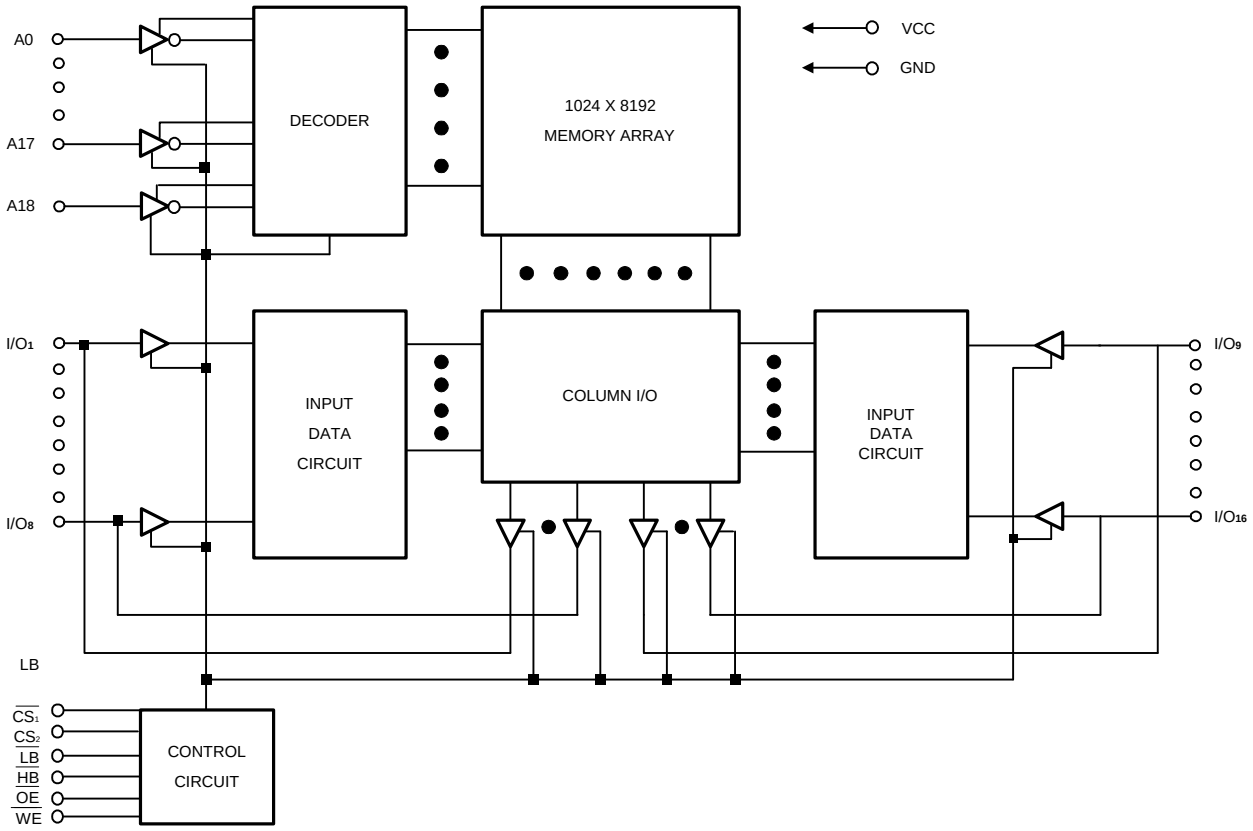
1. Typical values are measured at VCC = 3.0V, T_A = 25°C and not 100% tested.
2. Data retention current VCC = 2.0V.

Pin Configurations

■ **CSP (Chip Size Package)**
48-pin Top View

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CS_2
B	I/O_9	$\overline{HB}$	A3	A4	$\overline{CS_1}$	I/O_1
C	I/O_{10}	I/O_{11}	A5	A6	I/O_2	I/O_3
D	GND	I/O_{12}	A17	A7	I/O_4	VCC
E	VCC	I/O_{13}	NC	A16	I/O_5	GND
F	I/O_{15}	I/O_{14}	A14	A15	I/O_6	I/O_7
G	I/O_{16}	NC	A12	A13	$\overline{WE}$	I/O_8
H	A18	A8	A9	A10	A11	NC

Block Diagram



Pin Description - CSP

Symbol	Description	Symbol	Description
A0 - A18	Address Inputs	$\overline{HB}$	Higher Byte Enable Input (I/O_9 - I/O_{16})
$\overline{CS_1}$, CS_2	Chip Enable	$\overline{OE}$	Output Enable
I/O_1 - I/O_{16}	Data Input/Output	VCC	Power Supply
$\overline{WE}$	Write Enable Input	GND	Ground
$\overline{LB}$	Byte Enable Input (I/O_1 - I/O_8)	NC	No Connection

Recommended DC Operating Conditions

(T_A = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3	3.6	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND .....-0.5V to +4.0V
IN, IN/OUT Volt to GND ..... -0.5V to VCC + 0.5V
Operating Temperature, Topr .....-25°C to +85°C
Storage Temperature, Tstg.....-55°C to +125°C
Power Dissipation, P_T.....0.7W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = -25°C to + 85°C, VCC = 2.7V to 3.6V, GND = 0V)

Symbol	Parameter	LP62S16512-55/70LLT		Unit	Conditions
		Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	µA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{LB}$ = $\overline{HB}$ = V_{IH} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	5	mA	$\overline{CS_1}$ = V_{IL} , CS_2 = V_{IH} , $\overline{LB}$ = V_{IL} or $\overline{HB}$ = V_{IL} , $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	50	mA	Min. Cycle, Duty = 100%, $\overline{CS_1}$ = V_{IL} , CS_2 = V_{IH} , $\overline{LB}$ = V_{IL} or $\overline{HB}$ = V_{IL} $I_{I/O}$ = 0mA
I_{CC2}		-	15	mA	$\overline{CS_1}$ ≤ 0.2V, CS_2 ≥ VCC-0.2V , $\overline{LB}$ ≤ 0.2V or $\overline{HB}$ ≤ 0.2V f = 1MHz , $I_{I/O}$ = 0mA
I_{SB}	Standby Current	-	1	mA	$\overline{CS_1}$ = V_{IH} or CS_2 = V_{IL} or $\overline{LB}$ = $\overline{HB}$ = V_{IH}
I_{SB1}		-	20	µA	$\overline{CS_1}$ ≥ VCC - 0.2V or CS_2 ≤ 0.2V or $\overline{LB}$ = $\overline{HB}$ ≥ VCC-0.2V V_{IN} ≥ VCC-0.2V or V_{IN} ≤ 0.2V
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.2	-	V	I_{OH} = -1.0 mA

Truth Table

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{HB}$	I/O_1 to I/O_8 Mode	I/O_9 to I/O_{16} Mode	VCC Current
H	X	X	X	X	X	High - Z	High - Z	I_{SB1}, I_{SB}
X	L	X	X	X	X	High - Z	High - Z	I_{SB1}, I_{SB}
X	X	X	X	H	H	High - Z	High - Z	I_{SB1}, I_{SB}
L	H	L	H	L	L	Read	Read	I_{CC1}, I_{CC2}, I_{CC}
				L	H	Read	High - Z	I_{CC1}, I_{CC2}, I_{CC}
				H	L	High - Z	Read	I_{CC1}, I_{CC2}, I_{CC}
L	H	X	L	L	L	Write	Write	I_{CC1}, I_{CC2}, I_{CC}
				L	H	Write	High - Z	I_{CC1}, I_{CC2}, I_{CC}
				H	L	High - Z	Write	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	H	L	X	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}
L	H	H	H	X	L	High - Z	High - Z	I_{CC1}, I_{CC2}, I_{CC}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

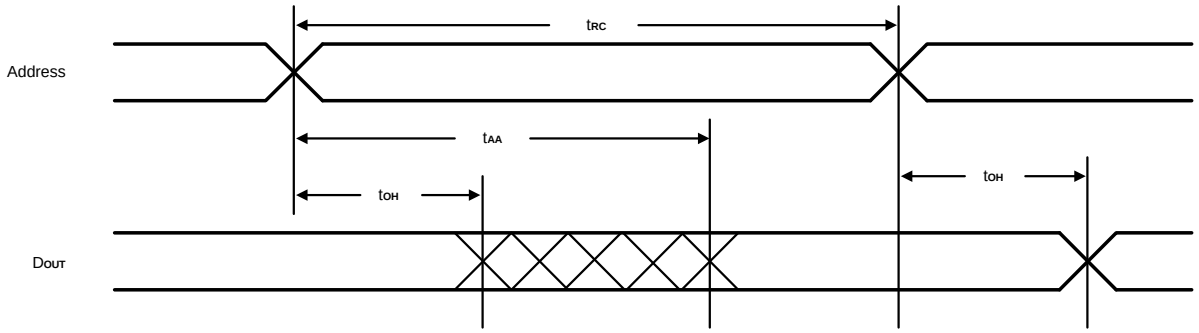
AC Characteristics (T_A = -25°C to +85°C, VCC = 2.7V to 3.6V)

Symbol	Parameter	LP62S16512-55LLT		LP62S16512-70LLT		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55	-	70	-	ns
t_{AA}	Address Access Time	-	55	-	70	ns
t_{ACS1} , t_{ACS2}	Chip Enable Access Time	-	55	-	70	ns
t_{BE}	Byte Enable Access Time	-	55	-	70	ns
t_{OE}	Output Enable to Output Valid	-	25	-	35	ns
t_{CLZ1} , t_{CLZ2}	Chip Enable to Output in Low Z	10	-	10	-	ns
t_{BLZ}	Byte Enable to Output in Low Z	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{CHZ1} , t_{CHZ2}	Chip Disable to Output in High Z	-	20	-	25	ns
t_{BHZ}	Byte Disable to Output in High Z	-	20	-	25	ns
t_{OHZ}	Output Disable to Output in High Z	-	20	-	25	ns
t_{OH}	Output Hold from Address Change	5	-	5	-	ns
Write Cycle						
t_{WC}	Write Cycle Time	55	-	70	-	ns
t_{CW1} , t_{CW2}	Chip Enable to End of Write	50	-	60	-	ns
t_{BW}	Byte Enable to End of Write	50	-	60	-	ns
t_{AS}	Address Setup Time	0	-	0	-	ns
t_{AW}	Address Valid to End of Write	50	-	60	-	ns
t_{WP}	Write Pulse Width	40	-	50	-	ns
t_{WR}	Write Recovery Time	0	-	0	-	ns
t_{WHZ}	Write to Output in High Z	-	25	-	25	ns
t_{DW}	Data to Write Time Overlap	25	-	30	-	ns
t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{OW}	Output Active from End of Write	5	-	5	-	ns

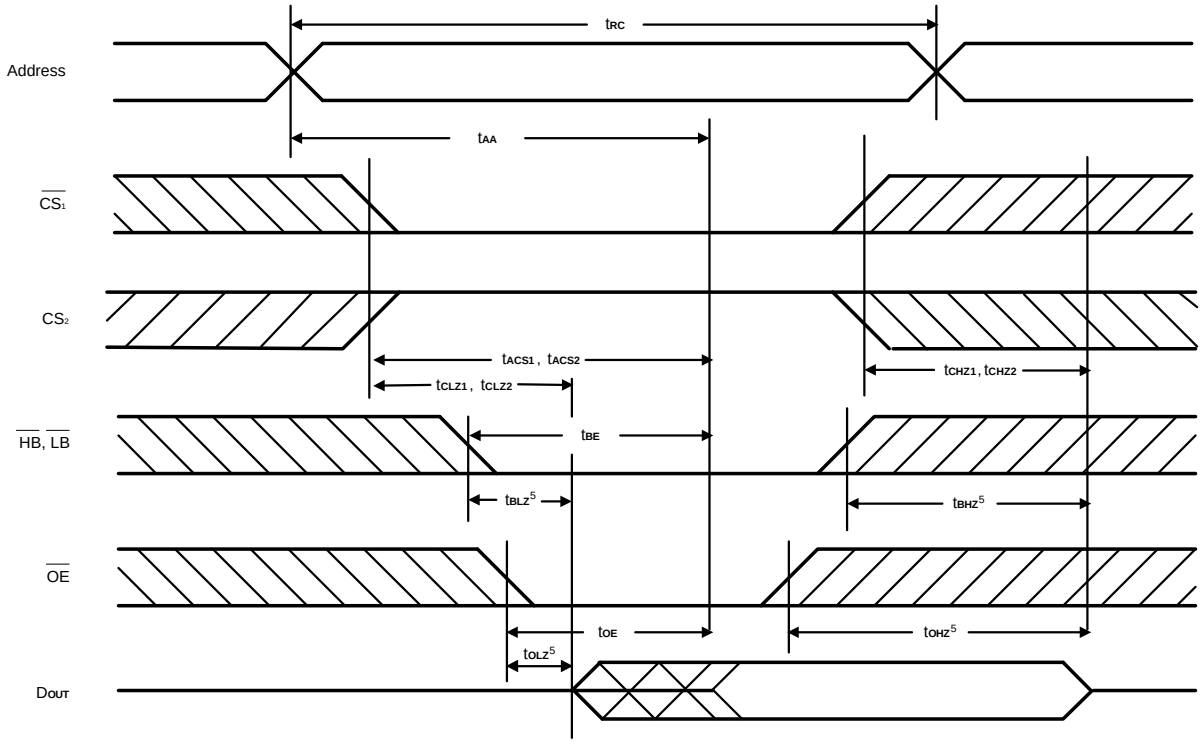
Note: t_{CLZ1} , t_{CLZ2} , t_{BLZ} , t_{OLZ} , t_{CHZ1}, t_{CHZ2} , t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1[1, 2, 4]



Read Cycle 2[1, 2, 3]

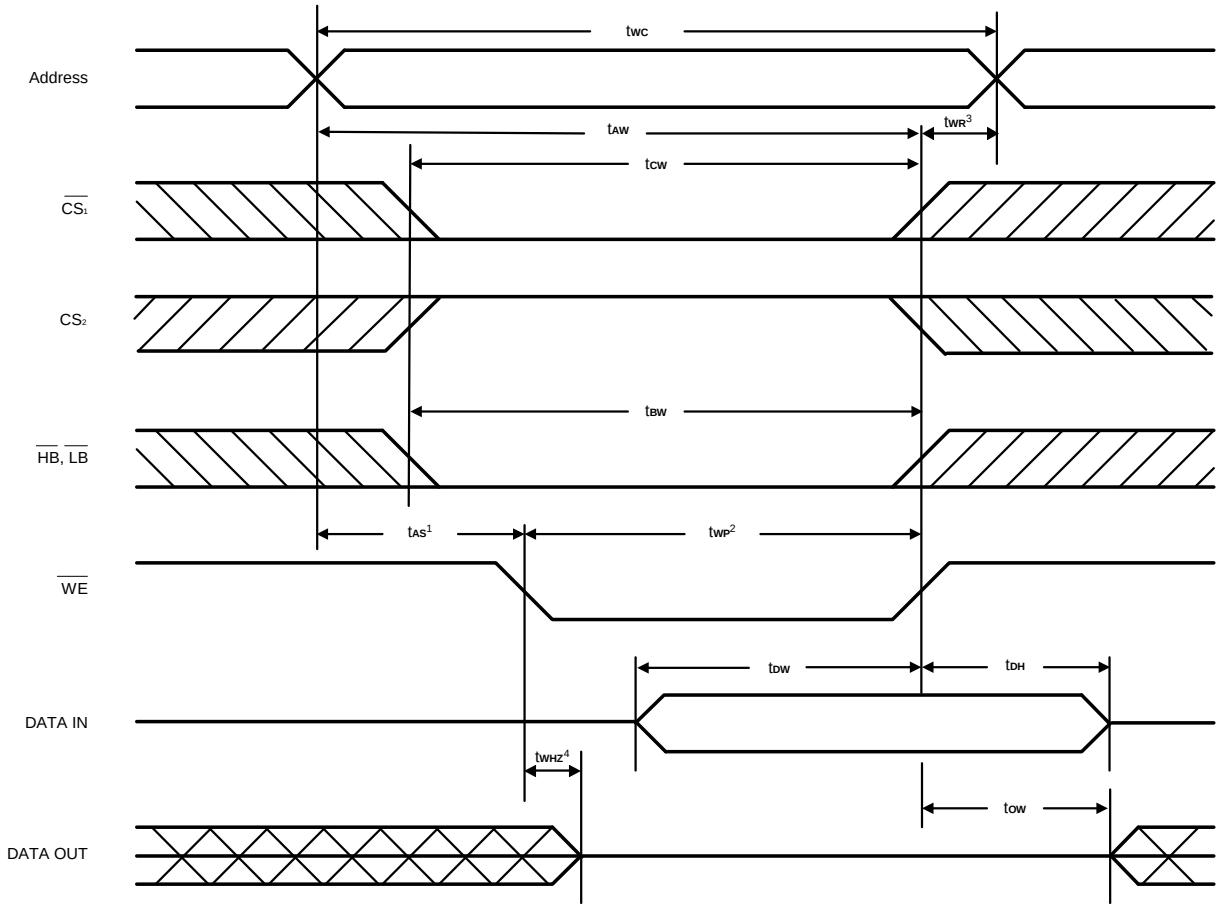


Notes: 1. $\overline{WE}$ is high for Read Cycle.

2. Device is continuously enabled $\overline{CS_1}$ = V_{IL}, or CS_2 = V_{IH}, $\overline{HB}$ = V_{IL} and, or $\overline{LB}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS_1}$ and ($\overline{HB}$ and, or $\overline{LB}$) transition low or CS_2 transition High.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

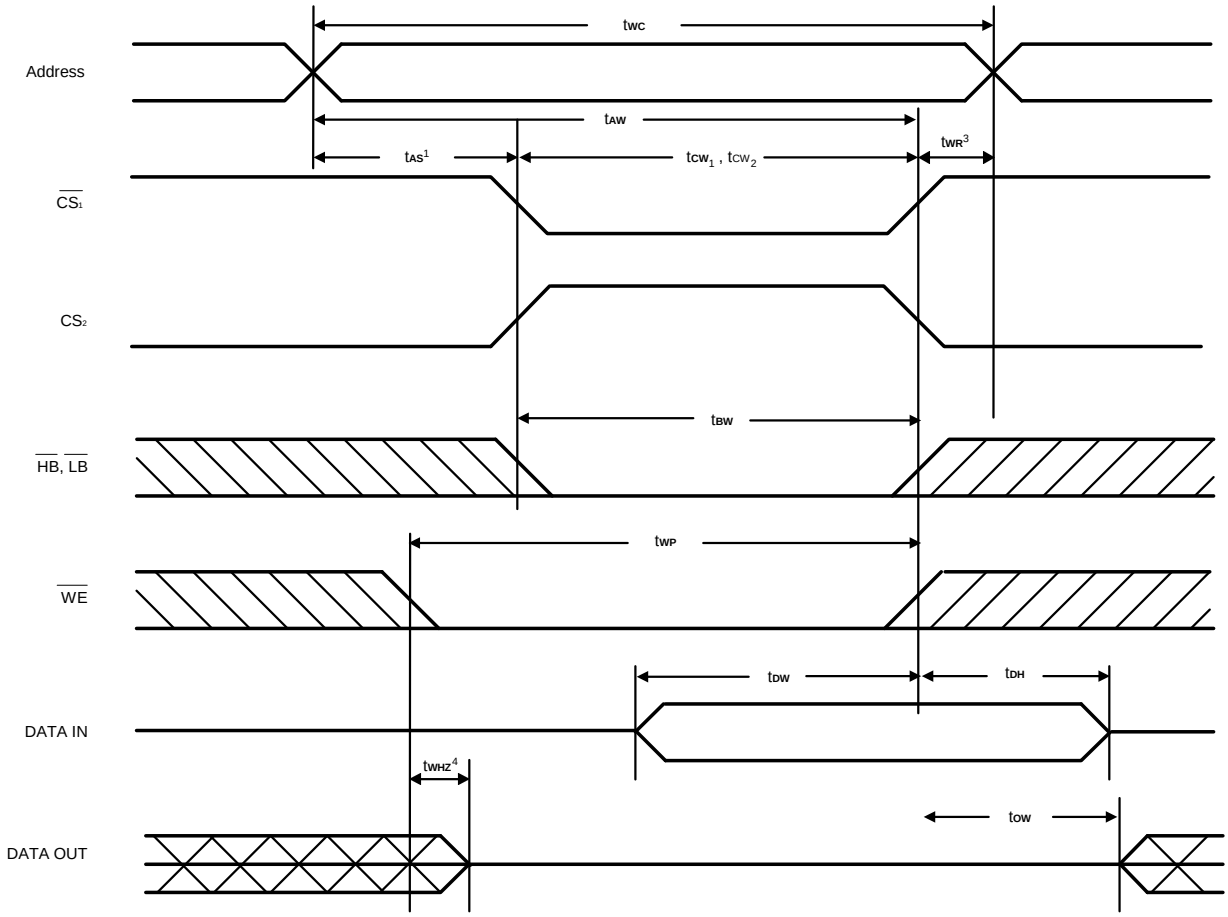
Timing Waveforms (continued)

Write Cycle 1
(Write Enable Controlled)



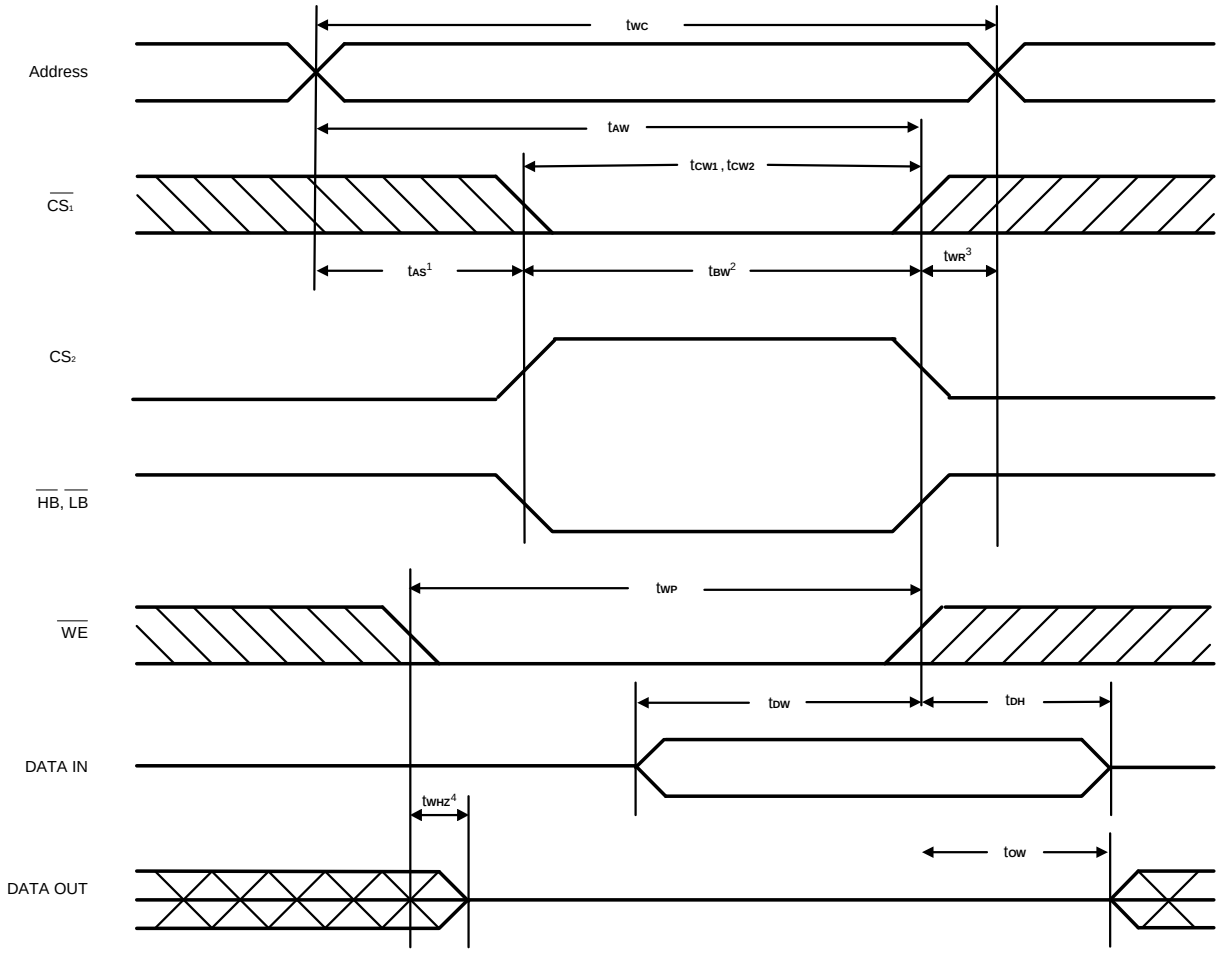
Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Timing Waveforms (continued)

Write Cycle 3
(Byte Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.

2. A Write occurs during the overlap (t_{WP}, t_{BW}) of a low $\overline{CS1}$, $\overline{WE}$ and ($\overline{HB}$ and , or $\overline{LB}$) or a high CS_2.
3. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ or ($\overline{HB}$ and , or $\overline{LB}$) going high or CS_2 going Low to the end of the Write cycle.
4. $\overline{OE}$ level is high or low.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise And Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

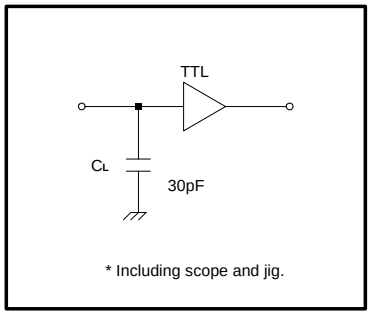


Figure 1. Output Load

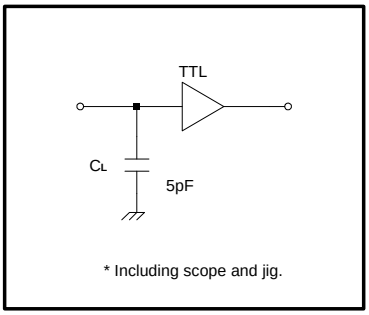


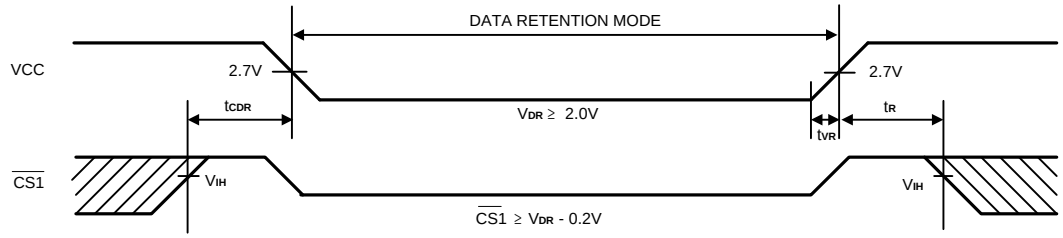
Figure 2. Output Load for t_{CLZ1}, t_{CLZ2} , t_{BHZ} , t_{BLZ} , t_{OLZ}, t_{CHZ1}, t_{CHZ2} , t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = -25°C to 85°C)

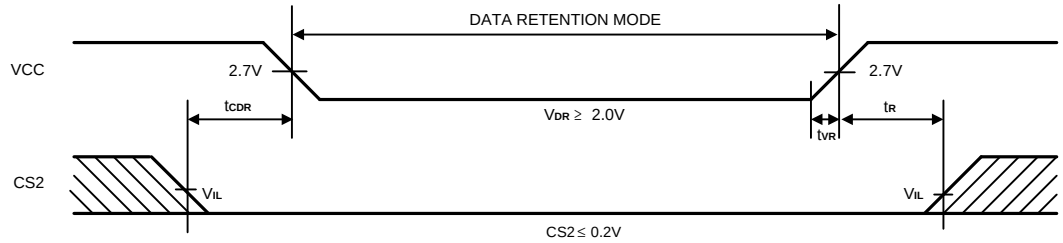
Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	2.0	3.6	V	$\overline{CS_1} \geq$ VCC - 0.2V or $CS_2 \leq$ 0.2V or $\overline{LB}$ = $\overline{HB}$ ≥ VCC-0.2V
I_{CCDR}	Data Retention Current	-	6*	µA	VCC = 2.0V, $\overline{CS_1} \geq$ VCC - 0.2V or $CS_2 \leq$ 0.2V or $\overline{LB}$ = $\overline{HB}$ ≥ VCC-0.2V $V_{IN} \geq$ VCC-0.2V or $V_{IN} \leq$ 0.2V
t_{CDR}	Chip Disable to Data Retention Time	0	-	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}	-	ns	
t_{VR}	VCC Rising Time from Data Retention Voltage to Operating Voltage	5	-	ms	

* LP62S16512-55/70LLT I_{CCDR}: max. 1µA at T_A = 25°C
(3µA at T_A = 0°C to + 40°C)

Low VCC Data Retention Waveform (1) ($\overline{CS1}$ Controlled)



Low VCC Data Retention Waveform (2) (CS2 Controlled)



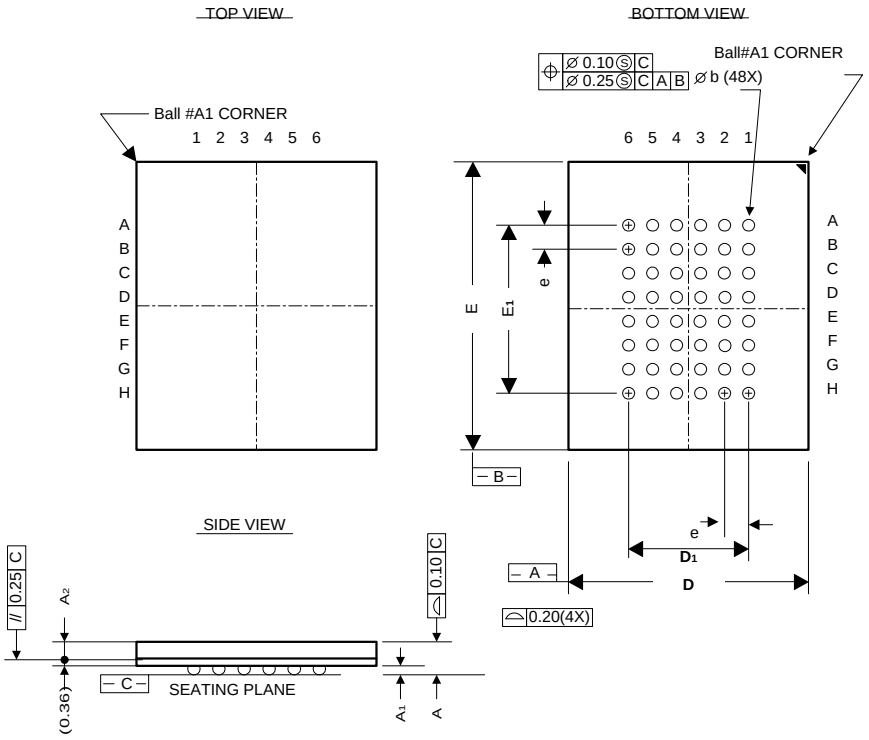
Ordering Information

Part No.	Access Time(ns)	Operating Current Max.(mA)	Standby Current Max.(uA)	Package
LP62S16512U-55LLT	55	50	20	48L CSP
LP62S16512U-70LLT	70	50	20	48L CSP

Package Information

48LD CSP (8 x 10 mm) Outline Dimensions (48TFBGA)

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	1.04	1.14	1.24
A_1	0.20	0.25	0.30
A_2	0.48	0.53	0.58
D	7.90	8.00	8.10
E	9.90	10.00	10.10
D_1	---	3.75	---
E_1	---	5.25	---
e	---	0.75	---
b	0.30	0.35	0.40

Notes:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. BALL PAD OPENING OF SUBSTRATE IS Φ 0.3mm (SMD)
   SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.3mm (NSMD)