Low IF 2.4 GHz ISM Transceiver

ATR2406

Preliminary

Features

- Fully Integrated Low IF Receiver
- Fully Integrated GFSK Modulator for 72, 144, 288, 576 and 1152 kBit/s
- High Sensitivity of Typically -93 dBm Due to Integrated LNA
- High Output Power of Typically +4 dBm
- Multi-channel Operation
  - 95 Channels
  - Support Frequency Hopping (ETSI) and Digital Modulation (FCC)
- Supply-voltage Range 2.9 V to 3.6 V (Unregulated)
- Auxiliary-voltage Regulator on Chip (3.2 V to 4.6 V)
- Low Current Consumption
- Few Low Cost External Components
- Integrated Ramp-signal Generator and Power Control for an Additional Power Amplifier
- Low Profile Lead-free Plastic Package QFN32 (5 × 5 × 0.9 mm)

Lead Free

Applications

- Hightech Multi-user Toys
- Wireless Game Controllers
- Telemetry
- Wireless Audio/Video
- Electronic Point of Sales
- Wireless Head Set
- FCC CFR47, Part 15, ETSI EN 300 328 and ARIB STD-T-66 Compliant Radio Links

Electrostatic sensitive device.
Observe precautions for handling.

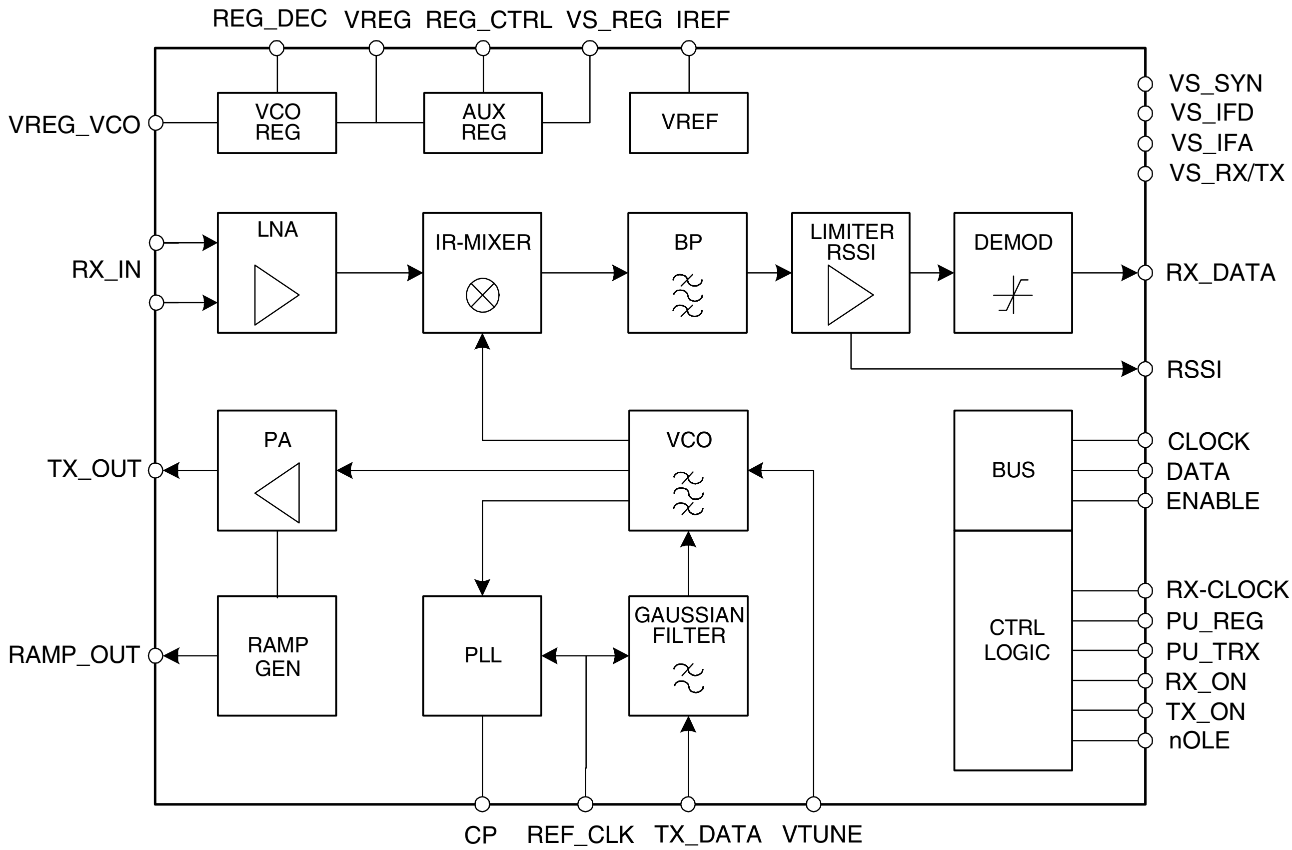
Description

The ATR2406 is a single chip RF-transceiver intended for applications in the 2.4 GHz ISM band. The QFN32 packaged IC is a complete transceiver including image rejection mixer, low IF filter, FM demodulator, RSSI, TX preamplifier, power-ramping generator for external power amplifier, integrated synthesizer, and a fully integrated VCO and TX filter. No mechanical adjustment is necessary in production.

The RF-transceiver offers a clock recovery function on-chip.

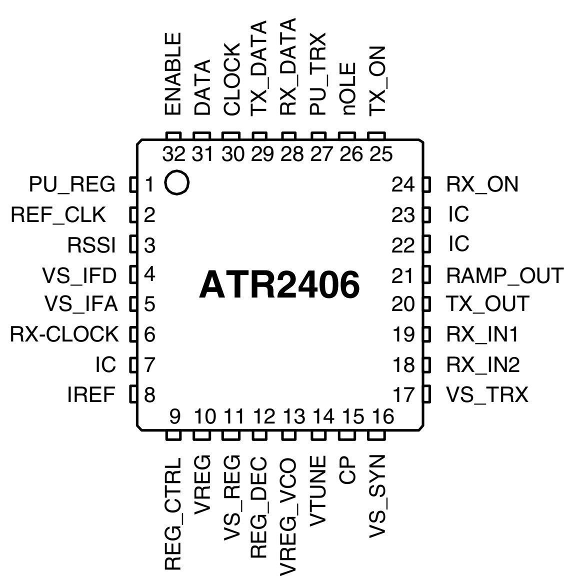
Rev. 4779F–ISM–09/04

Figure 1. Block Diagram



Pin Configuration

Figure 2. Pinning QFN32 - 5 × 5



Pin Description

Pin	Symbol	Function
1	PU_REG	Power-up input for auxiliary regulator
2	REF_CLK	Reference frequency input
3	RSSI	Received signal strength indicator output
4	VS_IFD	Digital supply voltage
5	VS_IFA	Analog supply voltage for IF circuits
6	RX-CLOCK	RX-CLOCK, if RX mode with clock recovery is active
7	IC	Internal connected, do not connect on PCB
8	IREF	External resistor for band-gap reference
9	REG_CTRL	Auxiliary voltage regulator control output
10	VREG	Auxiliary voltage regulator output
11	VS_REG	Auxiliary voltage regulator supply voltage
12	REG_DEC	Decoupling pin for VCO_REG
13	VREG_VCO	VCO voltage regulator
14	VTUNE	VCO tuning voltage input
15	CP	Charge-pump output
16	VS_SYN	Synchronous supply voltage
17	VS_TRX	Transmitter receiver supply voltage
18	RX_IN2	Differential receiver input 2
19	RX_IN1	Differential receiver input 1
20	TX_OUT	TX driver amplifier output
21	RAMP_OUT	Ramp generator output for PA power ramping
22	IC	Internal connected, do not connect on PCB
23	IC	Internal connected, do not connect on PCB
24	RX_ON	RX control input
25	TX_ON	TX control input
26	nOLE	Open loop enable input
27	PU_TRX	RX/TX/PLL/VCO power-up input
28	RX_DATA	RX data output
29	TX_DATA	TX data input
30	CLOCK	3-wire-bus: Clock input
31	DATA	3-wire-bus: Data input
32	ENABLE	3-wire-bus: Enable input
Paddle	GND	Ground

Functional Description

Receiver

The RF signal at RF_IN is differently fed through the LNA to the image rejection mixer IR_MIXER driving the integrated LowIF bandpass filter. The IF frequency is 864 kHz.The limiting IF_AMP with an integrated RSSI function feeds the signal to the digital demodulator DEMOD. No tuning is required. Datasling is handled internally.

Clock Recovery

For 1152 kBit/s data rate the receiver has a clock recovery function on-chip.

The receiver includes a clock recovery circuit which regenerates the clock out of the received data. The advantage is that this recovered clock is synchronous to the clock of the transmitting device (and thus to the transmitted data) which allows to reduce the load of the processing microcontroller significantly.

The falling edge of the clock gives the optimal sampling position for the RX_Data signal so at this event the data must be sampled by the microcontroller. The recovered clock is available at pin 6.

Transmitter

The transmit data at TX_DATA is filtered by an integrated Gaussian Filter GF and fed to the fully integrated VCO operating at twice the output frequency. After modulation the signal is frequency-divided by 2 and fed to the internal preamplifier PA. This preamplifier supplies typically +4 dBm output power at TX_OUT.

A ramp-signal generator RAMP_GEN, providing a ramp signal at RAMP_OUT for the external power amplifier, is integrated. The slope of the ramp signal is controlled internally so that spurious requirements are fulfilled.

Synthesizer

The IR_MIXER, the PA and the programmable counter PC are driven by the fully integrated VCO, using on-chip inductors and varactors. The output signal is frequency divided to supply the desired frequency to the TX_DRIVER, 0/90 degree phase shifter for the IR_MIXER and to be used by the PC for the phase detector PD (f_{PD} = 1.728 MHz). Open loop modulation is supported.

Power Supply

An integrated bandgap-stabilized voltage regulator for use with an external low-cost PNP transistor is implemented. Multiple power-down and current saving modes are provided.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min.	Max.	Unit
Supply voltage auxiliary regulator	V_S	-0.3	+4.7	V
Supply voltage	V_S	-0.3	+3.6	V
Control voltages	V_{contr}	-0.3	V_S	V
Storage temperature	T_{stg}	-40	+125	°C
Input RF level	P_{RF}		+10	dBm
ESD protection	V_{ESD_anal}		TBD	V
	V_{ESD_dig}		TBD	V

Operating Range

Parameters	Symbol	Min.	Max.	Unit
Supply voltage	V_S	2.9	3.6	V
Auxiliary regulator supply voltage	V_{S_BATT}	3.2	4.6	V
Temperature ambient	T_{amb}	-10	+60	°C
Input frequency range	f_{RX}	2400	2483	MHz

Electrical Characteristics

V_S = 3.6 V with AUX regulator, T_{amb} = 25°C, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
1	**Supply**						
1.1	Supply voltage	With AUX regulator	V_S	3.2	3.6	4.6	V
1.2	Supply voltage	w/o AUX regulator	V_S	2.9	3.0	3.6	V
1.3	RX supply current	CW-mode	I_S		31		mA
1.4	TX supply current	CW-mode	I_S		16		mA
1.5	Synthesizer supply current		I_S		26		mA
1.6	Supply current in power-down mode	With AUX regulator PU_TRX = 0; PU_REG = 0	I_S		< 1		µA
1.7	Supply current in power-down mode	w/o AUX regulator PU_TRX = 0; PU_REG = 0	I_S		< 1		µA
2	**Voltage Regulator**						
2.1	AUX regulator		VREG		3.0		V
2.2	VCO regulator		VREG_VCO		2.7		V
3	**Transmitter Part**						
3.1	TX data rate			72/144/288/576/1152			kBit/s
3.2	Output power	Over full temperature range, from 2400 MHz to 2483 MHz(1)	PTX	0		4	dBm

Notes: 1. Measured and guaranteed only on the Atmel evaluation board, including PCB and balun filter.
2. Timing is determined by external loop filter characteristics. Faster timing can be achieved by modification of loop filter. For further information refer to Application Note.

Electrical Characteristics (Continued)

V_S = 3.6 V with AUX regulator, T_{amb} = 25°C, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
3.3	TX data filter clock	6 taps in filter	f_{TXFCLK}		6.912		MHz
3.4	Frequency deviation		GFFM_nom		±400		kHz
3.5	Frequency deviation scaling	GFFM = GFFM_nom × GFCS (see bus protocol D9 to D11)	GFCS	60		130	%
3.6	Frequency drift during a slot		Δfo (drift)			±10	kHz
3.7	Harmonics 2nd Harmonic 3rd Harmonic	BW = 100 kHz(1)				 -40.5 -46	 dBc dBc
3.8	Spurious Emission 30 - 1000 MHz 1 - 12.75 GHz 1.8 - 1.9 GHz 5.15 - 5.3 GHz	BW = 100 kHz(1)				 -40.5 -48 -70 -70	 dBm dBm dBm dBm
4	**Receiver Part**						
4.1	Sensitivity	At input for BER ≤10^{-3} at 1152 kBit/s(1)			-93		dBm
4.2	Third order input intercept point		IIP3		-15		dBm
4.3	Intermodulation rejection	BER < 10^{-3}, wanted at -83 dBm, level of interferers in channels N + 2 and N + 4(1)	IM_3	32			dBc
4.4	Co-channel rejection	BER < 10^{-3}, wanted at -76 dBm(1)	R_{CO}	-11			dBc
4.5	Adjacent channel rejection	BER < 10^{-3}, wanted at -76 dBm, adjacent level referred to wanted channel level(1) ±1.728 MHz	$R_{i\ (N-1)}$	4			dBc
4.6	Bi-adjacent channel rejection	BER < 10^{-3}, wanted at -76 dBm, bi-adjacent level referred to wanted channel level(1) ±3.456 MHz	$R_{i\ (N-2)}$	30			dBc
4.7	Rejection with ≥ 3 channels separation	BER < 10^{-3}, wanted at -76 dBm, n ≥ 3 adjacent level referred to wanted channel level(1) ≥ ±5.128 MHz	$R_{i\ (n \geq 3)}$	40			dBc
4.8	Out of band rejection > 6 MHz	BER < 10^{-3}, wanted at -83 dBm at 2.45 GHz(1)	$Bl_{df>6MHz}$	38			dBc
4.9	Out of band rejection 2300 MHz to 2394 MHz 2506 MHz to 2600 GHz	BER < 10^{-3}, wanted at -83 dBm at 2.45 GHz(1)	Blnear	47			dBc
4.10	Out of band rejection 30 MHz to 2300 MHz 2600 MHz to 6 GHz	BER < 10^{-3}, wanted at -83 dBm at 2.45 GHz(1)	Blfar	57			dBc
5	**RSSI Part**						
5.1	Maximum RSSI output voltage	Under high RX input signal level	$V_{RSSImax}$		2.1		V

Notes: 1. Measured and guaranteed only on the Atmel evaluation board, including PCB and balun filter.
2. Timing is determined by external loop filter characteristics. Faster timing can be achieved by modification of loop filter. For further information refer to Application Note.

Electrical Characteristics (Continued)

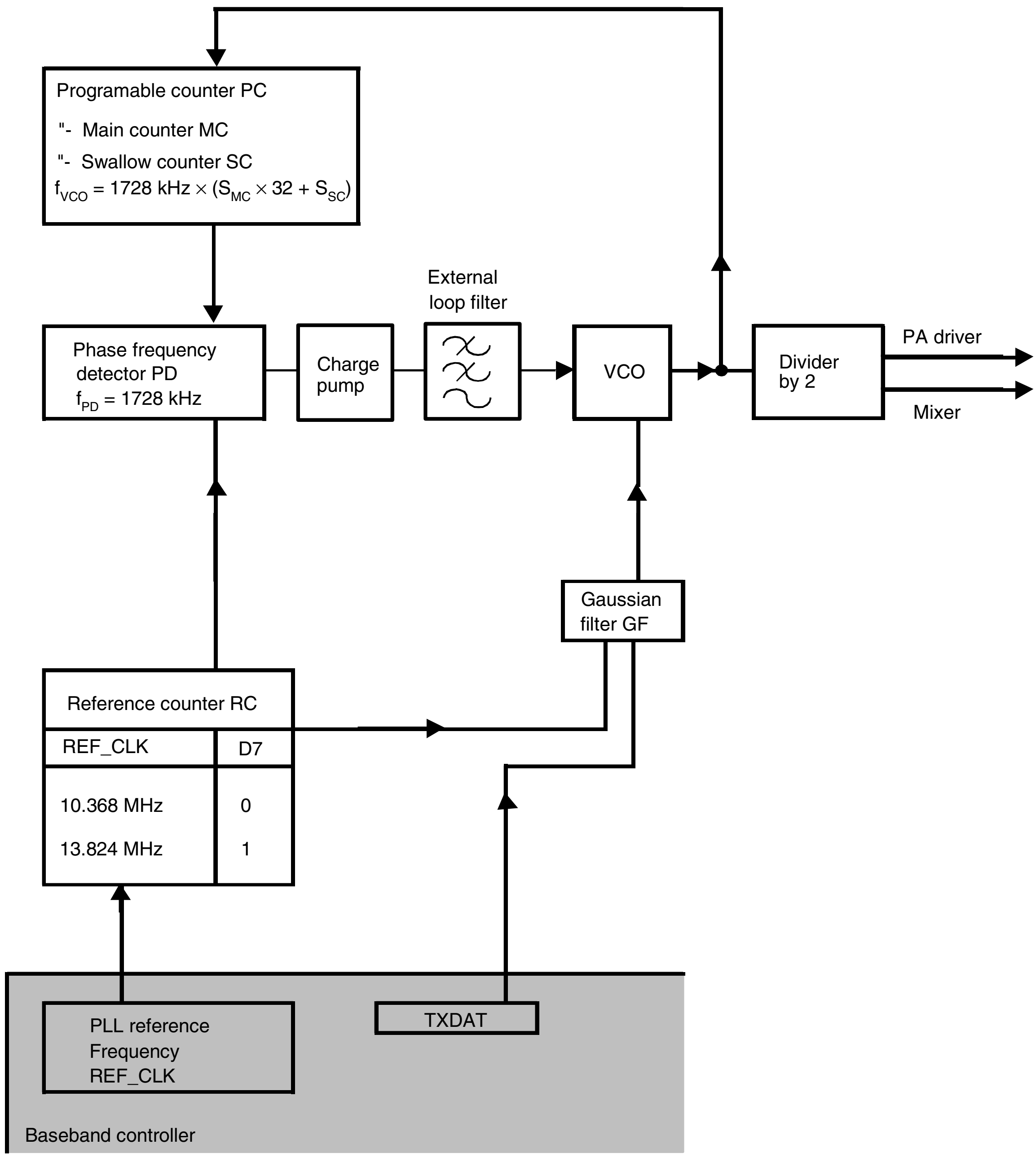
V_S = 3.6 V with AUX regulator, T_{amb} = 25°C, unless otherwise specified

No.	Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
5.2	RSSI output voltage, monotonic over range -96 dBm to -36 dBm	with -33 dBm at RF input with -96 dBm at RF input	V_{RSSI}		1.9 0.3		V V
5.3	Wake-up time from power-up signal to correct RSSI output		T_{on}			40	µs
6	**VCO**						
6.1	Oscillator frequency	Over full temperature range(1)		2400		2483	MHz
6.2	Frequency control voltage range		V_{VTUNE}	0.5		V_{CC} - 0.5	V
6.3	VCO tuning input gain		G_{VCO}		150		MHz/V
7	**Synthesizer**						
7.1	External reference input frequency	D7 = 0 D7 = 1	REF_CLK		10.368 13.824		MHz MHz
7.2	Sinusoidal input signal level (RMS value)	AC coupled sinewave	REF_CLK	250		500	mV_{RMS}
7.3	Scaling factor prescaler		S_{PSC}		32/33		
7.4	Scaling factor main counter		S_{MC}		86/87/88/89		
7.5	Scaling factor swallow counter		S_{SC}	0		31	
8	**Phase Detector**						
8.1	Phase detector comparison frequency		f_{PD}		1728		kHz
9	**Charge-pump Output**						
9.1	Charge-pump output current	V_{CP} = 1/2 V_{CC}	I_{CP}		±2		mA
9.2	Leakage current	V_{CP} = 1/2 V_{CC}	I_L		±100		pA
10	**Timing Conditions(1)(2)**						
10.1	Transmit to Receive time		TX →RX-time		100		µs
10.2	Receive to Transmit time		RX →TX-time		100		µs
10.3	Channel switch time		CS-time		350		µs
10.4	Power down to Transmit		PD →TR-time		450		µs
10.5	Power down to Receive		PD →RX-time		400		µs
10.6	Programming register		PRR-time		3		µs
10.7	PLL settling time		PLL set-time		350		µs
11	**Interface Logic Input and Output Signal Levels, Pin DATA, CLOCK, ENABLE**						
11.1	HIGH-level input voltage	Logic 1	V_{IH}	1.4		3.4	V
11.2	LOW-level input voltage	Logic 0	V_{IL}	-0.3		+0.4	V
11.3	HIGH-level output voltage	Logic 1	V_{OH}			3.4	V
11.4	LOW-level output voltage	Logic 0	V_{OL}	0			V
11.5	Input bias current	Logic 1 or logic 0	I_{bias}	-5		+5	µA
11.6	3-wire bus clock frequency		f_{CLKmax}			10	MHz

Notes: 1. Measured and guaranteed only on the Atmel evaluation board, including PCB and balun filter.
2. Timing is determined by external loop filter characteristics. Faster timing can be achieved by modification of loop filter. For further information refer to Application Note.

PLL Principle

Figure 3. PLL Principle



The following table shows the LO frequencies for RX and TX in the 2.4 GHz ISM band. There are 95 channels available. Since the ATR2406 supports wideband modulation with 400 kHz deviation, every second channel can be used without overlap in the spectrum.

Table 1. LO Frequencies

Mode	f_{IF}/kHz	Channel	f_{ANT}/MHz	f_{VCO}/MHz	S_{MC}	S_{SC}	N
TX		C0	2401.056	2401.056	86	27	2779
		C1	2401.920	2401.920	86	28	2780
		...	...	...	...	...	...
		C93	2481.408	2481.408	89	24	2872
		C94	2482.272	2482.272	89	25	2873
RX	864	C0	2401.056	2401.920	86	28	2780
		C1	2401.920	2402.784	86	29	2781
		...	...	...	...	...	...
		C93	2481.408	2482.272	89	25	2873
		C94	2482.272	2483.136	89	26	2874

TX Register Setting

The following 16-bit word has to be programmed for TX.

MSB															LSB
Data bits															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	PA		GFCS			1	RC	MC		SC				

Note: D12 and D13 are only relevant if ramping generator in conjunction with external PA is used, otherwise it can be programmed 0 or 1.

Table 2. Output Power Settings with Bits D12 - D13

PA (Output Power Settings)		
D13	**D12**	**RAMP_OUT (Pin 21)**
0	0	1.3 V
0	1	1.35 V
1	0	1.4 V
1	1	1.75 V

RX Register Setting

The are two RX settings possible. For a data rate of 1152 kBit/s an internal clock recovery function is implemented.

Register Setting without Clock Recovery

Must be used for data rates below 1.152 Mbit.

MSB															LSB
Data bits															
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	1	X	X	X	X	X	0	RC	MC		SC				

Note: X values are not relevant and can be set to 0 or 1.

RX Register Setting with Internal Clock Recovery

Recommended for 1.152 Mbit data rate.

The output pin of the recovered clock is pin 6. The falling edge of the recovered clock signal samples the data signal.

MSB								
Data bits								
D24	D23	D22	D21	D20	D19	D18	D17	D16
1	0	1	0	0	0	0	0	0

															LSB
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	X	X	X	X	X	0	RC	MC		SC				

Note: X values are not relevant and can be set to 0 or 1.

PLL Settings

RC, MC and SC bits are controlling the synthesizer frequency according to Table 3, Table 4 and Table 5.

Formula for calculating the frequency:

TX frequency: $f_{ANT} = 864\ \text{kHz} \times (32 \times S_{MC} + S_{SC})$
RX frequency: $f_{ANT} = 864\ \text{kHz} \times (32 \times S_{MC} + S_{SC} + 1)$

Table 3. PLL Settings with the Reference Counter Bit D7

RC (Reference Counter)	
D7	**CLK Reference**
0	10.368 MHz
1	13.824 MHz

Table 4. PLL Settings with the Main Counter Bits D5 - D6

MC (Main Counter)		
D6	**D5**	S_{MC}
0	0	86
0	1	87
1	0	88
1	1	89

Table 5. PLL Settings with the Swallow Counter Bits D0 - D4

SC (Swallow Counter)					
D4	**D3**	**D2**	**D1**	**D0**	S_{SC}
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
...	...	...	...	...	...
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

GFCS Adjustment

The Gaussian Filter Control Setting is used to compensate production tolerances by tuning the modulation deviation in production to the nominal value of 400 kHz. These bits are only relevant in TX mode.

Table 6. GFCS Adjustment with Bits D9 - D11

GFCS (Gaussian Filter Control Settings)			
D11	**D10**	**D9**	**GFCS**
0	0	0	60%
0	0	1	70%
0	1	0	80%
0	1	1	90%
1	0	0	100%
1	0	1	110%
1	1	0	120%
1	1	1	130%

The VRAMP voltage is used to control the output power of an external power amplifier. The voltage ramp is started with the TX_ON signal.

These bits are only relevant in TX mode.

Control Signals

The various transceiver functions are activated by the following control signals. A timing proposal is given in Figure 5 on page 13

Table 7. Control Signals – Functions

Signal	Functions
PU_REG	Activates AUX voltage regulator and the VCO voltage regulator supplying the complete transceiver
PU_TRX	Activates RX/TX blocks
RX_ON	Activates RX circuits: DEMOD, IF AMP, IR MIXER
TX_ON	Activates TX circuits: PA, RAMP GEN, Starts RAMP SIGNAL at RAMP_OUT
nOLE	Disables open loop mode of the PLL

Serial Programming Bus

The transceiver is programmed by the SPI (CLOCK, DATA and ENABLE).

After setting enable signal to low condition, on the rising edge of the clock signal, the data is transferred bit by bit into the shift register, starting with the MSB-bit. When the enable signal has returned to high condition, the programmed information is active. Additional leading bits are ignored and there is no check made how many clock pulses arrived during enable low condition.

The programming of the transceiver is done by a 16 bit or 25 bit data word (for the RX clock recovery mode).

3-wire BUS Timing

Figure 4. 3-wire Bus Protocol Timing Diagram

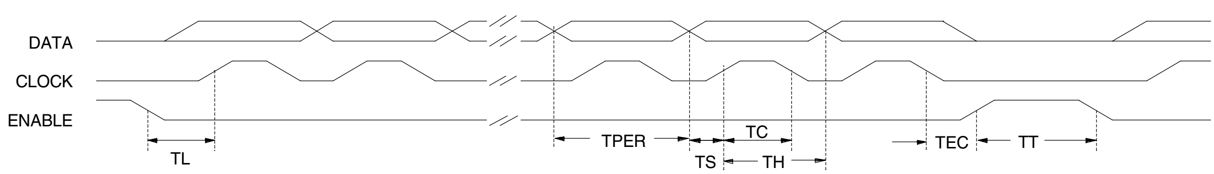


Table 8. 3-wire Bus Protocol Table

Description	Symbol	Minimum Value	Unit
Clock period	TPER	100	ns
Set time data to clock	TS	20	ns
Hold Time data to clock	TH	20	ns
Clock pulse width	TC	60	ns
Set time enable to clock	TL	100	ns
Hold time enable to data	TEC	0	ns
Time between two protocols	TT	250	ns

Figure 5. Complete TX and RX Timing Diagram

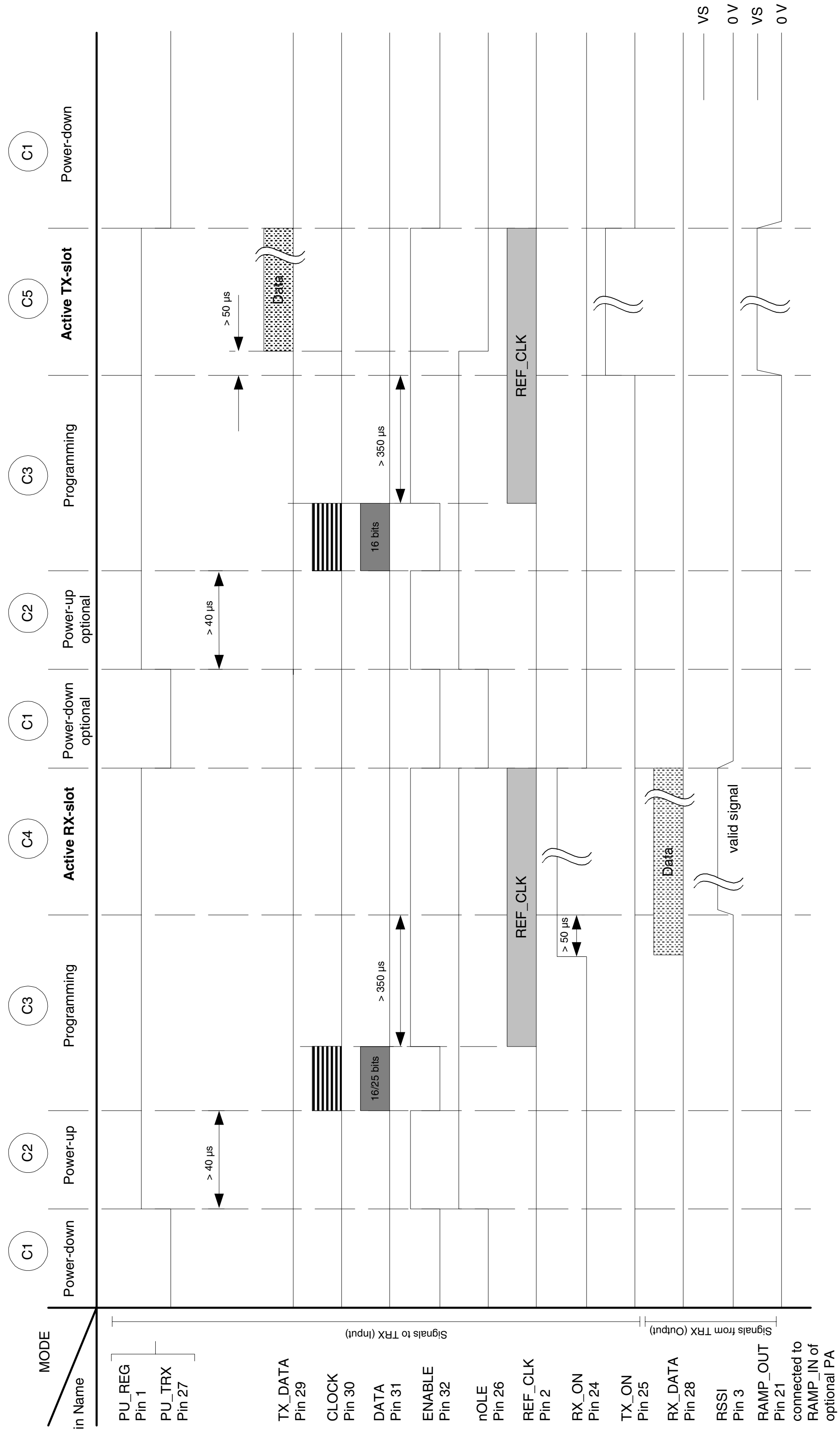


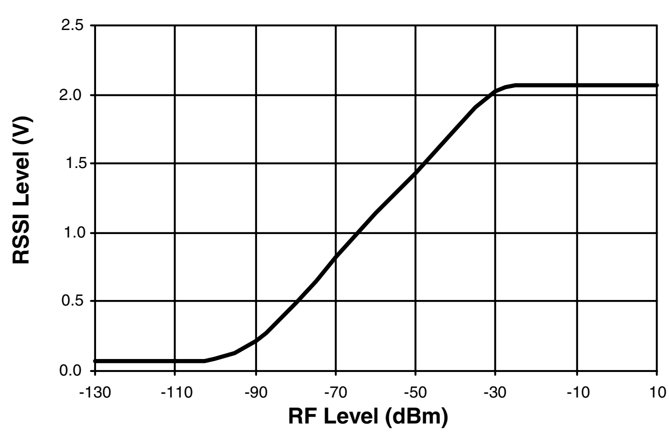
Table 9. Description of the Conditions/States

Conditiion	Description
C1	Power-down ATR2406 is switched off and the supply current is lower than 1 µA.
C2	Power-up ATR2406 is powered up by toggling PU_REG and PU_RTX to high. PU_REG enables the external AUX-Regulator transistor and PU_TRX enables the internal regulator like VCO_REG (VCO supply voltage regulator) as well as wakes up the PLL, the VCO, the demodulator, mixer, etc. It is necessary to wait at least 40 µs until the different supply voltage regulators have settled.
C3	Programming Via the tree-wire-interface the internal register of ATR2406 is programmed. At TX, this is just the PLL (transmit channel) and the deviation (gaussian filter). At RX, this is just the PLL (receive channel) and if the clock recovery is used also the bits to enable this option. At start of the three-wire-programming, the enable signal is toggled from high to low to enable clocking the data into the internal register. When the enable signals rises again to high, the programmed data is latched. This is the time point at which the settling of the PLL is starting. It is necessary to wait the settling time of 350 µs so that the VCO-Frequency is stable. The reference clock needs to be applied to ATR2406 at minimum the time when the PLL is in operation - which is the programming state (C3) and the active slot (C4, C5). Out of the reference clock, several internal signals are also derived, i.e., the gaussian filter circuitry and TX_DATA sampling.
C4	This is the receive slot where the transmit burst is received and data as well as recovered clock are available.
C5	This is the active transmit slot. As soon as TX_DATA is applied to ATR2406, the signal nOLE toggles to low which enables modulation in open-loop-mode.

Received Signal Strength Indication RSSI

The RSSI is given as an analog voltage at the RSSI pin. A typical plot of the RSSI value is shown in Figure 6.

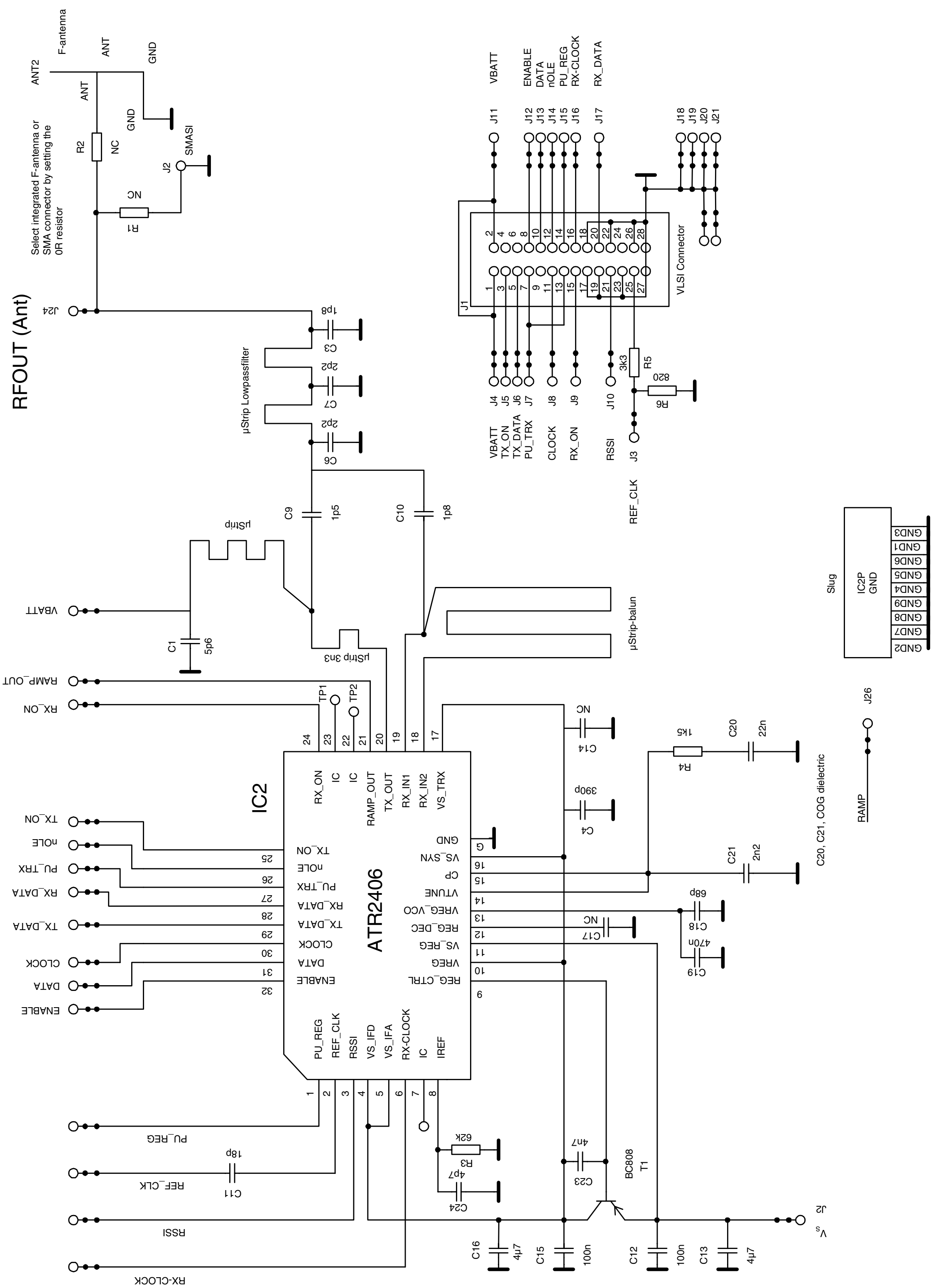
Figure 6. Typical RSSI Value versus Input Power



Application Circuit

The ATR2406 requires only few low cost external components for operation. A typical application is shown in Figure 7.

Figure 7. Application Circuit



PCB-layout Design

Figure 8. PCB-layout ATR2406-DEV-BOARD

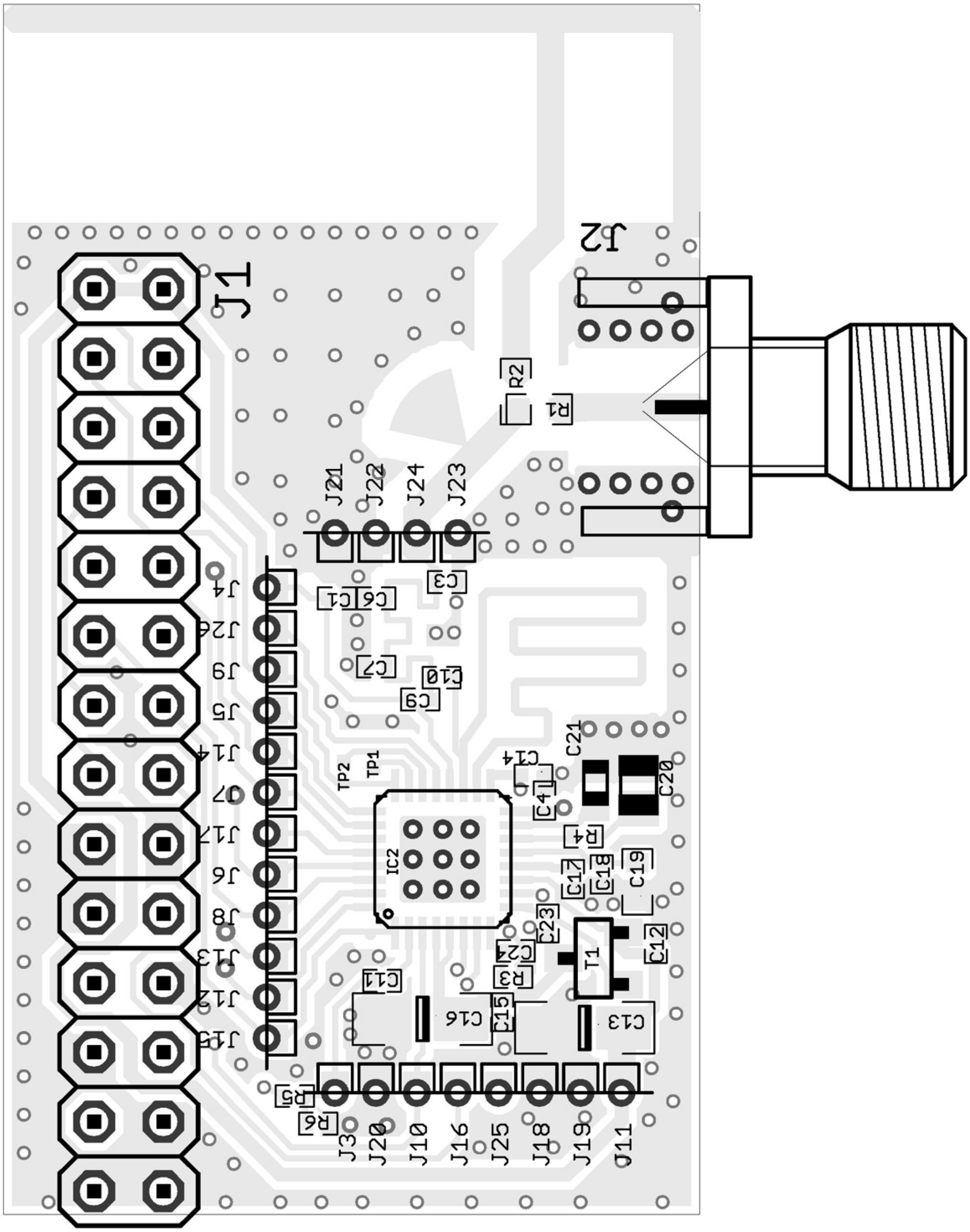


Table 10. Bill of Material

Part	Value	Part Number	Vendor	Package	Comment
C1	5p6	GJM1555C1H5R6CB01 or GRM1555C1H5R6DZ01	Murata®	0402	
C3	1p8	GJM1555C1H1R8CB01 or GRM1555C1H1R8CZ01	Murata	0402	
C4	390p	GRM1555C1H391JA01	Murata	0402	
C5	4p7	GJM1555C1H4R7CB01 or GRM1555C1H4R7CZ01	Murata	0402	NC
C6	2p2	GJM1555C1H2R2CB01 or GRM1555C1H2R2CZ01	Murata	0402	
C7	2p2	GJM1555C1H2R2CB01 or GRM1555C1H2R2CZ01	Murata	0402	
C9	1p5	GJM1555C1H1R5CB01 or GRM1555C1H1R5CZ01	Murata	0402	
C10	1p8	GJM1555C1H1R8CB01 or GRM1555C1H1R8CZ01	Murata	0402	
C11	18P	GRM1555C1H180JB01	Murata	0402	
C12	100n	GRM15F51H104ZB01	Murata	0402	
C13	4µ7	B45196H2475M109	Epcos®	3216	Optional[2]
C14	1n	GRM15R71H102KB01	Murata	0402	NC
C15	100n	GRM15F51H104ZB01	Murata	0402	
C16	4µ7	B45196H2475M109	Epcos	3216	Optional[2]
C17	3n3	GRM15R71H332KB01	Murata	0402	NC
C18	68p	GRM155C1H680JB01	Murata	0402	
C19	470n	GRM18F51H474ZB01 (0402) or 0603-Version	Murata	0402/0603	
C20	22n, COG	GRM21B5C1H223JA01	Murata	0805	
C21	2n2, COG	GRM1885C1H222JA01	Murata	0603	
C23	4n7	GRM15R71H472KB01	Murata	0402	
C24	4p7	GRM1555C1H4R7CB01	Murata	0402	
L6	8n2	WE-MK0402 744784082	Würth Electronic®	0402	NC, µStrip used
R3	62k	62k, ←5%	Vishay®	0402	
R4	1k5	1k5, ←5%	Vishay	0402	
R5	3k3	3k3, ←5%	Vishay	0402	Ref_Clk-Level, optional[1]
R6	820R	820R, ←5%	Vishay	0402	Ref_Clk-Level, optional[1]
IC2	ATR2406	ATR2406	Atmel	MLF32	
T1	BC808-40	BC808-40, any standard type can be used, important is "-40"	Vishay, Philips®, ...	SOT-23	Optional[2]
MSUB	FR4	FR4, e_r = 4.4 at 2.45 GHz, H = 500 µm, T = 35 µm, tand = 0.02, surface i.e. chem. tin or chem. gold			

Note: Option[1] = no necessary if supplied RefClk level is within specification range
Option[2] = if no AUX regulator is used, then T1 has to be bypassed
To use the integrated F-antenna, set jumper R2 (0R resistor 0603)

Table 11. Parts Count Bill of Material

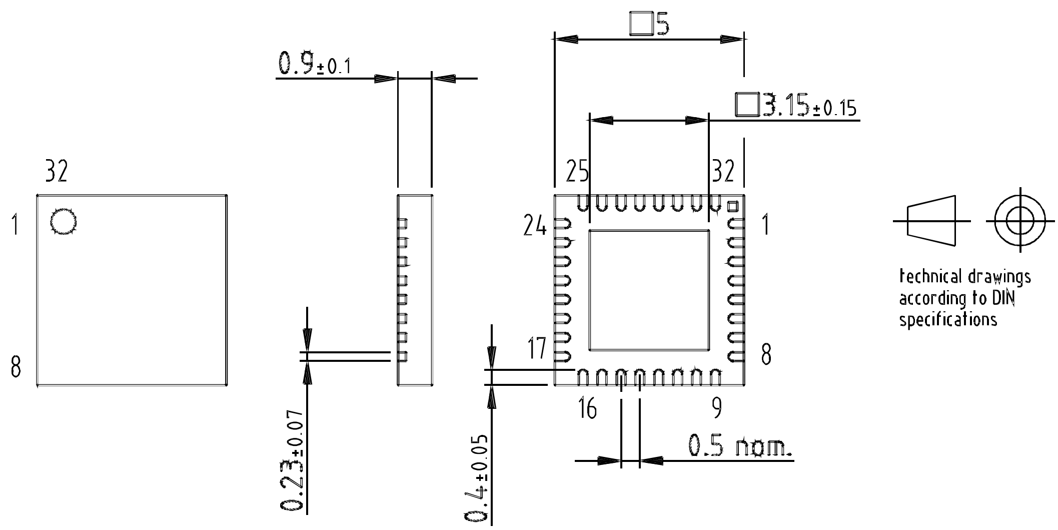
Parts Count	Required (Minimal BOM)	Optional (Depending on Application)
Capacitors 0402	14	-
Capacitors >0402	2	2
Resistors 0402	2	2
Inductors 0402	-	-
Semiconductors	1	1

Ordering Information

Extended Type Number	Package	Remarks	MOQ
ATR2406-PNSG	QFN32 - 5x5	Tube, Sampling; Pb-free	600
ATR2406-PNQG	QFN32 - 5x5	Taped and reeled; Pb-free	6000
ATR2406-DEV-BOARD	-	RF-module	1
ATR2406-DEV-KIT	-	Complete Evaluation-kit	1

Package Information

Package: QFN 32 - 5x5
Exposed pad 3.15x3.15
(acc. JEDEC OUTLINE No. MO-220)
Dimensions in mm



Drawing-No.: 6.543-5087.01-4
Issue: 2; 24.01.03

Recommended Footprint/Landing Pattern

Figure 9. Recommenced Footprint/Landing Pattern

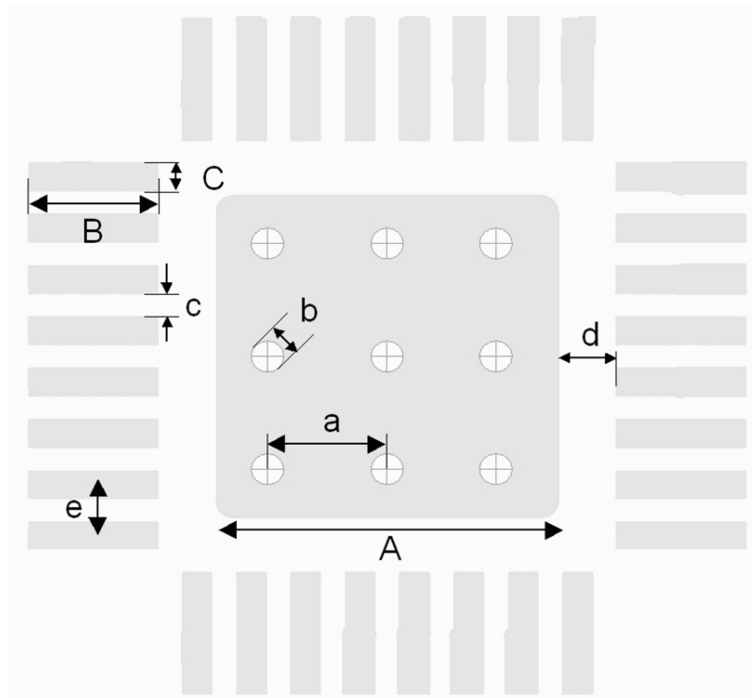


Table 1. Recommended Footprint/Landing Pattern Signs

Sign	Size
A	3.2 mm
B	1.2 mm
C	0.3 mm
a	1.1 mm
b	0.3 mm
c	0.2 mm
d	0.55 mm
e	0.5 mm

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4779F–ISM–09/04