Features

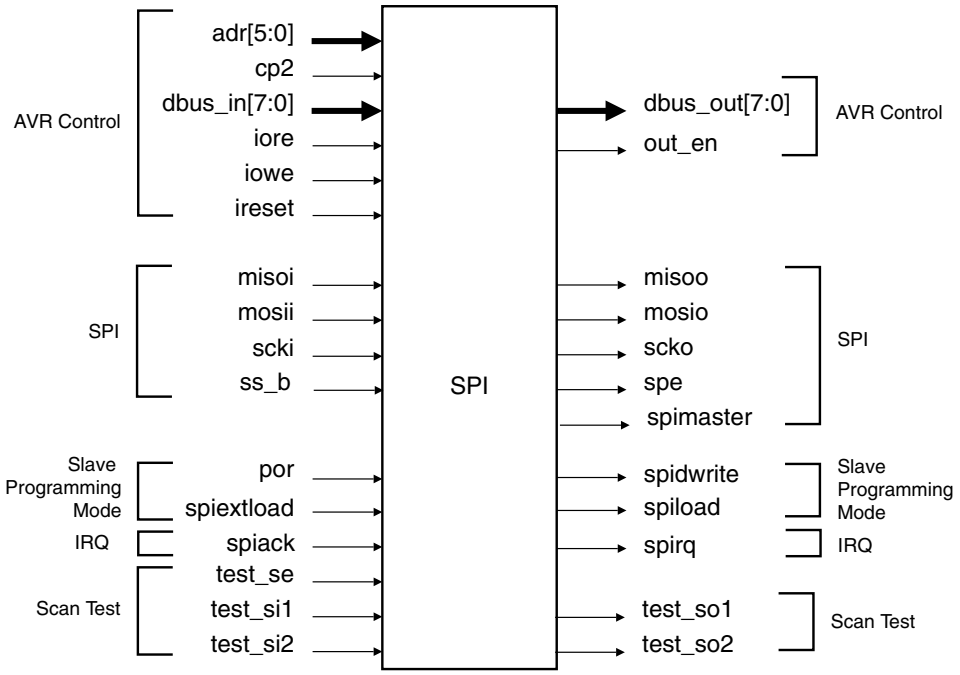
- **Full-duplex, 3-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **Maximum Bit Frequency of f_{CLOCK}/4 (in M-bits/second)**
- **LSB First or MSB First Data Transfer**
- **Four Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wakeup from Idle Mode (Slave Mode Only)**

Description

The AVR® embedded RISC microcontroller core is a low-power, CMOS 8-bit microprocessor based on the AVR enhanced RISC architecture. With this core, Atmel proposes a Serial Peripheral Interace (SPI).

The SPI allows high-speed synchronous data transfers between the AVR core and peripheral devices or between the AVR core and other cores.

Figure 1. SPI Pin Configuration



Serial Peripheral Interface (SPI)

AVR® Embedded RISC Microcontroller Core Peripheral

Rev. 1127A–10/99

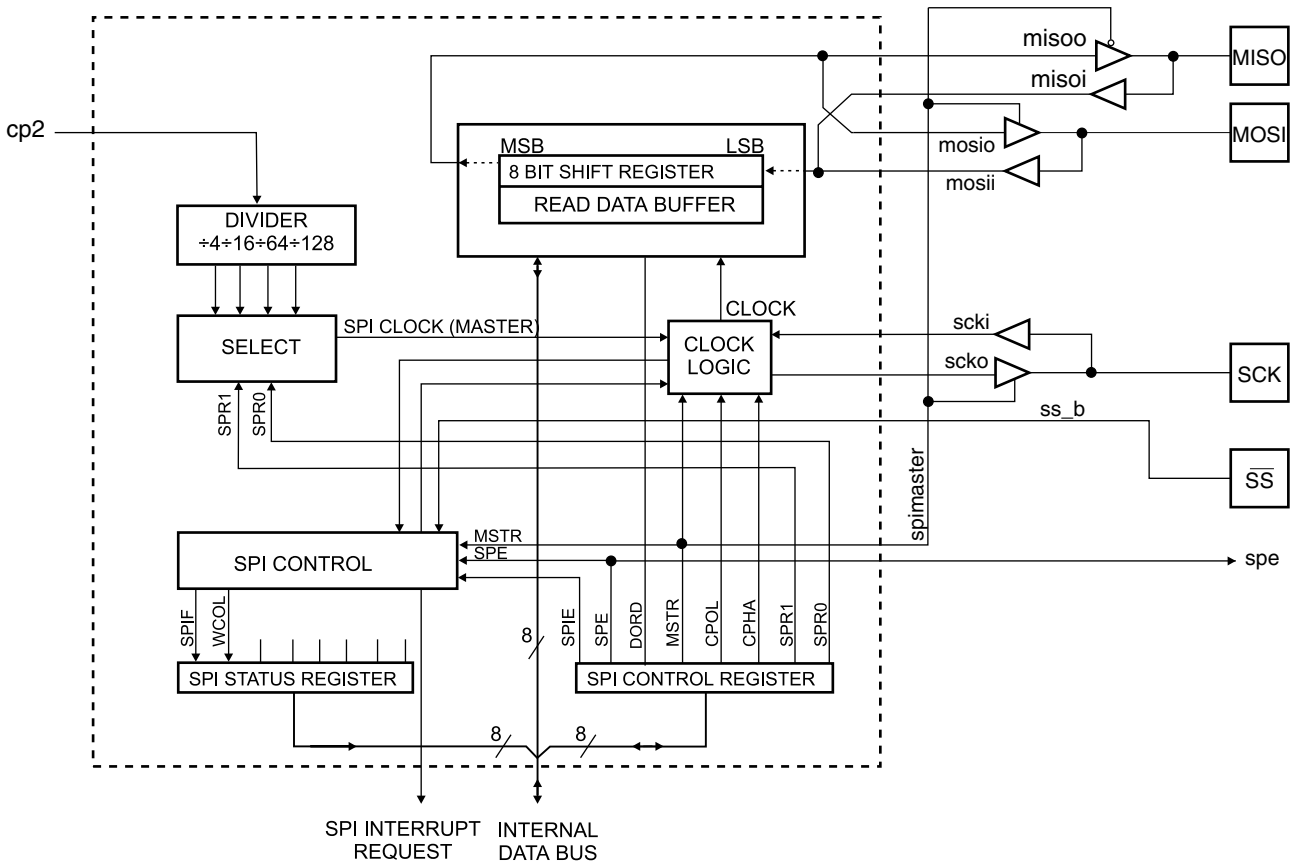
Table 1. Pin Description

Pin Name	Description	Direction	Comments
		AVR Control	
cp2	CPU clock	Input	Any register in the SPI will update its contents only on the positive edge of cp2
ireset	Synchronous reset	Input	When high, ireset will reset internal registers by reading the value on dbus_in which is forced to zero by the AVR Core
dbus_out[7:0]	Data bus output	Output	Valid only when accompanied by a strobe on out_en
dbus_in[7:0]	Data bus input	Input	
out_en	Output enable strobe	Output	When high, out_en indicates that the SPI requires control of the data bus
adr[5:0]	I/O address inputs	Input	Valid only when accompanied by a strobe on iore or iowe
iore	I/O read strobe	Input	Used to read the contents of the I/O location addressed by adr
iowe	I/O write strobe	Input	Used to update the contents of the I/O location addressed by adr
		SPI	
ss_b	SPI slave select	Input	Used to select SPI activity, slave or master. If active, turns off the SPI master flag (SPCR[4])
spe	SPI enable	Output	When high, spe indicates that the SPI peripheral is enabled. This mirrors the spi enable flag (SPCR[6])
spimaster	SPI is master	Output	When high, indicates that SPI peripheral is in master mode. This mirrors the SPI master flag (SPCR[4])
scko	SPI clock ouput	Output	Used to generate SPI clock in master mode
scki	SPI clock input	Input	Used to latch SPI data (MOSII and MISOO) in SPI slave mode
mosio	Master out, slave in output	Output	Used for data output in master mode
misoi	Master in, slave out input	Input	Used for data input in master mode
misoo	Master in, slave out output	Output	Used for data output in slave mode
mosii	Master out, slave in input	Input	Used for data input in slave mode
		IRQ	
spirq	SPI irq line	Output	When high, indicates that the SPI interrupt flag is set (SPSR[7]) and that SPI interrupt is enabled (SPCR[7])
spiack	SPI interrupt acknowledge	Input	Used to reset SPI interrupt flag
		Test Scan	
test_se	Scan enable input	Input	Active high. Enable scan shift.
test_mode	Test mode input	Input	Active high. Must be set during scan testing.
test_si1	Scan chain 1 input	Input	Scan chain 1 input.
test_si2	Scan chain 2 input	Input	Scan chain 2 input.
test_so1	Scan chain 1 output	Output	Scan chain 1 input.
test_so2	Scan chain 2 output	Output	Scan chain 2 output.

Table 1. Pin Description (Continued)

Pin Name	Description	Direction	Comments
Slave Programming Mode			
por	Power on reset	Input	Used to select SPI Flash/EEPROM programming slave mode. This mode is enabled with por low and ireset high.
spiextload	External data load enable	Input	Enable parallel load of transmit shift register from dbus_in during slave programming mode.
spiload	Active data load	Output	Indicates that the transmit shift register is updated on rising edge of cp2 with dbus_in value. This strobe will remain active until spiextload goes low.
spidwrite	Active data write	Output	Indicates that a byte has been sent and data on dbus_out is valid for reading.

Figure 2. SPI Block Diagram



Description

The SPI is a fully synchronous peripheral. It can run at a $F_{CP2}/4$ maximum baud rate which is controlled by SPCR[1:0].

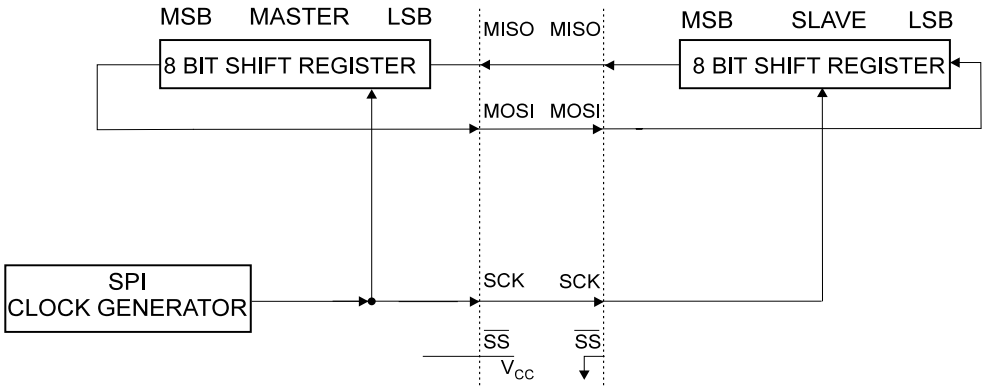
The SPI has one interrupt request output called **spirq**. This interrupt is controlled as follows:

- Cleared by ireset
- Set when receive FIFO is full
- Cleared by acknowledge (spiack high)
- Cleared by a read in the SPI Status Register (SPSR) followed by an access to SPI Data Register (SPDR), read or write

The interconnection between master and slave CPUs with SPI is shown in Figure 3. The SCK pin is the clock output in the master mode and is the clock input in the slave mode.

Writing to the SPI data register of the master CPU starts the SPI clock generator, and the data written shifts out of the MOSI pin and into the MOSI pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end of transmission flag (SPIF). If the SPI interrupt enable bit (SPIE) in the SPCR register becomes set, an interrupt is requested. The Slave Select input, $\overline{SS}$, is set low to select an individual SPI device as a slave. The two shift registers in the Master and the Slave can be considered as one distributed 16-bit circular shift register. This is shown in Figure 3. When data is shifted from the master to the slave, data is also shifted in the opposite direction simultaneously. This means that during one shift cycle, data in the master and the slave are interchanged.

Figure 3. SPI Master-Slave Interconnection



The system is single buffered in the transmit direction and double buffered in the receive direction. This means that characters to be transmitted cannot be written to the SPI Data Register before the entire shift cycle is completed. When receiving data, however, a received character must be read from the SPI Data Register before the next character has been completely shifted in. Otherwise, the first character is lost.

When the SPI is enabled, the data direction of the MOSI, MISO, SCK and $\overline{SS}$ pins is overriden according to the following table:

Table 2. SPI Pin Overrides

Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	Output	Input
MISO	Input	Output
SCK	Output	Input
$\overline{SS}$	–	Input

$\overline{SS}$ Pin Functionality

When the SPI is configured as a master (MSTR in SPCR is set), the user can determine the direction of the $\overline{SS}$ pin. If $\overline{SS}$ is configured as an output, the pin is a general output pin which does not affect the SPI system. If $\overline{SS}$ is configured as an input, it must be held high to ensure Master SPI operation. If, in master mode, the $\overline{SS}$ pin is input, and is driven low by peripheral circuitry, the SPI system interprets this as that another master selects the SPI as a slave and will start sending data to it. To avoid bus contention, the SPI system takes the following actions:

1. The MSTR bit in SPCR is cleared and the SPI system becomes a slave. As a result of the SPI becoming a slave, the MOSI and SCK pins become inputs.
2. The SPIF flag in SPSR is set, and if the SPI interrupt is enabled, the interrupt routine will be executed.

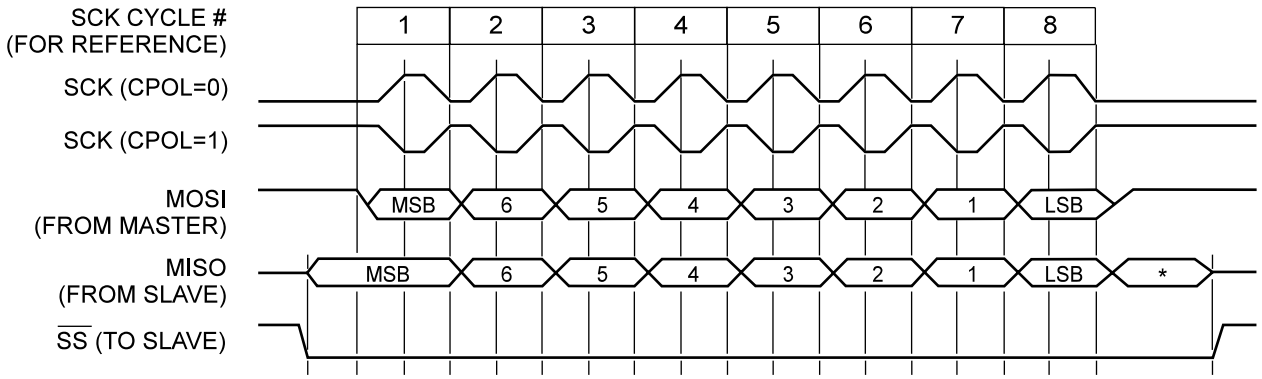
Thus, when interrupt-driven SPI transmision is used in master mode, and there is a possibility that $\overline{SS}$ is driven low, the interrupt should always check that the MSTR bit is still set. Once the MSTR bit has been cleared by a slave select, it must be set by the user.

When the SPI is configured as a slave, the $\overline{SS}$ is always input. When $\overline{SS}$ is held low, the SPI is activated and MISO becomes an output if configured so by the user. All other pins are inputs. When $\overline{SS}$ is driven low, all pins are inputs, and the SPI is passive, which means that it will not receive incoming data.

Data Modes

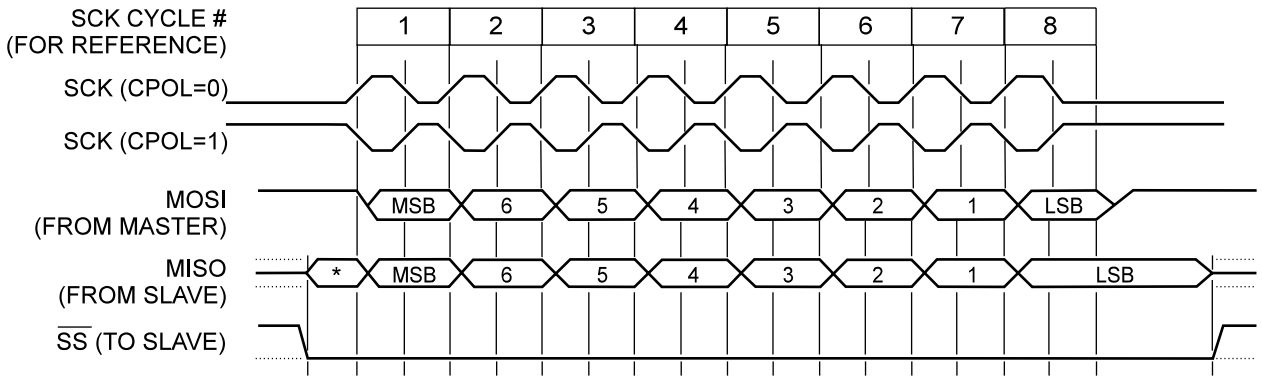
There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 4 and Figure 5.

Figure 4. SPI Transfer Format with CPHA = 0



* Not defined but normally MSB of character just received

Figure 5. SPI Transfer Format with CPHA = 1



* Not defined but normally LSB of previously transmitted character

The SPI Control Register - SPCR

Bit	7	6	5	4	3	2	1	0	
$0D ($2D)	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

Bit 7 - SPIE : SPI Interrupt Enable:
This bit causes setting of the SPIF bit in the SPSR register to execute the SPI interrupt provided that global interrupts are enabled.

Bit 6 - SPE : SPI Enable:
When the SPE bit is set (one), the SPI is enabled. This bit must be set to enable any SPI operations.

Bit 5 - DORD : Data ORDer:
When the DORD bit is set (one), the LSB of the data word is transmitted first.

When the DORD bit is cleared (zero), the MSB of the data word is transmitted first.

Bit 4 - MSTR : Master/Slave Select:
This bit selects Master SPI mode when set (one), and Slave SPI mode when cleared (zero). If $\overline{SS}$ is configured as an input and is driven low while MSTR is set, MSTR will be cleared, and SPIF in SPSR will become set. The user will then have to set MSTR to re-enable SPI master mode.

Bit 3 - CPOL : Clock POLarity:
When this bit is set (one), SCK is high when idle. When CPOL is cleared (zero), SCK is low when idle. Refer to Figure 4 and Figure 5 for additional information.

Bit 2 - CPHA : Clock PHAse:
Refer to Figure 4 or Figure 5 for the functionality of this bit.

Bits 1,0 - SPR1, SPR0 : SPI Clock Rate Select 1 and 0:
These two bits control the SCK rate of the device configured as a master. SPR1 and SPR2 have no effect on the slave. The relationship between SCK and the Oscillator Clock frequency f_{CP2} is shown in the following table:

Table 3. Relationship Between SCK and the Oscillator Frequency

SPR1	SPR0	SCK Frequency
0	0	f_{CP2}/ 4
0	1	f_{CP2} / 16
1	0	f_{CP2} / 64
1	1	f_{CP2}/ 128

The SPI Status Register - SPSR

Bit	7	6	5	4	3	2	1	0	
$0E ($2E)	SPIF	WCOL	-	-	-	-	-	-	SPSR
Read/Write	R	R	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	

Bit 7 - SPIF : SPI Interrupt Flag:
When a serial transfer is complete, the SPIF bit is set (one) and an interrupt is generated if SPIE in SPCR is set (one) and global interrupts are enabled. If $\overline{SS}$ is an input and is driven low when the SPI is in master mode, this will also set the SPIF flag. SPIF is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, the SPIF bit is cleared by first reading the SPI status register with SPIF set (one), then accessing the SPI Data Register (SPDR).

Bit 6 - WCOL : Write COLlision flag:

The WCOL bit is set if the SPI data register (SPDR) is written during a data transfer. During data transfer, the result of reading the SPDR register may be incorrect, and writing to it will have no effect. The WCOL bit (and the SPIF bit) are cleared (zero) by first reading the SPI Status Register with WCOL set (one), and then accessing the SPI Data Register.

Bit 5..0 - Res : Reserved bits:

These bits are reserved bits and will always read as zero.

The SPI interface may also be used for program memory and EEPROM downloading or uploading controlled by por, spiextload, spidload and spidwrite signals.

The SPI Data Register - SPDR

Bit	7	6	5	4	3	2	1	0	
$0F ($2F)	**MSB**							**LSB**	**SPDR**
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	–	–	–	–	–	–	–	–	Undefined

The SPI Data Register is a read/write register used for data transfer between the register file and the SPI Shift register. Writing to the register initiates data transmission. Reading the register causes the Shift Register Receive buffer to be read.

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