Features

- **High performance ULC family suitable for large-sized CPLDs and FPGAs**
- **Conversions to over 2,000,000 FPGA gates**
- **Pin counts to over 976 pins**
- **Any pin–out matched due to limited number of dedicated pads**
- **Full range of packages: LCC/PLCC, PQFP/TQFP, fine pitch BGA, PGA/PPGA**
- **2.5V I/O and 3.3V tolerant/compliant**
- **Low quiescent current: <0.3 nA/gate**
- **Available in commercial and industrial grades**
- **0.25 mm Drawn CMOS, 5 Metal Layers**
- **Library Optimised for Synthesis, Static Timing Analysis & Automatic Test Pattern Generation (ATPG)**
- **High Speed Performance:**
  - **100 ps Typical Gate Delay @2.5V**
  - **Typical 280 MHz Flip-Flop Toggle Frequency @2.5V**
- **High System Frequency Skew Control:**
  - **Clock Tree Synthesis Software**
- **2.5Volts & 3.3Volts Operation; Single or Dual Supply Modes**
- **Low Power Consumption:**
  - **<0.18 µW/Gate/MHz @2.5V**
- **Power on Reset**
- **Standard 2, 4, 6, 8,10, 12 and 18 mA I/Os**
- **CMOS/TTL/PCI Interface, LVCMOS, LVTTL, PECL, PCI (33/66 MHz) levels, GTL/GTL+, HSTL, SSTL2, SSTL3, CCT, AGP, LVDS**
- **ESD (2 kV) and Latch-up Protected I/O**
- **High Noise & EMC Immunity:**
  - **I/O with Slew Rate Control**
  - **Internal Decoupling**
  - **Signal Filtering between Periphery & Core**

Description

The UA2 series of ULCs is well suited for conversion of large sized CPLDs and FPGAs. Devices are implemented in high–performance CMOS technology with 0.25–µm (drawn) channel lengths, and are capable of supporting flip–flop toggle rates of 280 MHz at 2.5V, and input to output delay cells as fast as 100ps at 2.5V. The architecture of the UA2 series allows for efficient conversion of many PLD architecture and FPGA device types with higher IO count. A compact RAM cell, along with the large number of available gates allows the implementation of RAM in FPGA architectures that support this feature, as well as JTAG boundary–scan and scan–path testing.

Conversion to the UA2 series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100mA or more even when not being clocked. The UA2 series has a very low standby consumption of less than 0.3 nA/gate typically commercial temp, which would yield a standby current of 0.3 nA/gate, 0.42µA on a 144,000 gates design. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

The UA2 series provides several options for output buffers, including a variety of drive levels up to 18mA. Schmitt trigger inputs are also an option. A number of techniques are used for improved noise immunity and reduced EMC emissions, including: several independent power supply busses and internal decoupling for isolation; slew rate limited outputs are also available if required.

WIRELESS & µC

0.25 µm ULC Series

UA2

Preliminary

Rev. A – 29-Oct-01

The UA2 series is designed to allow conversion of high performance 2.5V devices. Support of mixed supply conversions (2.5V core, 3.3V periphery) is also possible, allowing optimal trade–offs between speed and power consumption.

Array Organization

Device Number	4LM Routable Gates	5LM Routable Gates	Full Programmable usable pads
UA2044	9,535	10,727	36
UA2/68	30,096	33,858	60
UA2084	50,410	56,712	76
UA2100	75,472	84,906	92
UA2120	106,278	120,449	112
UA2132	131,670	149,226	124
UA2144	159,778	181,081	136
UA2160	200,998	227,797	152
UA2184	270,663	306,751	176
UA2208	329,281	376,321	200
UA2228	401,010	458,298	220
UA2256	512,398	585,598	248
UA2304	733,635	838,440	296
UA2352	925,815	1,068,248	344
UA2388	1,133,594	1,307,994	380
UA2432	1,417,125	1,635,145	424
UA2484	1,651,406	1,926,640	476
UA2540	2,069,052	2,413,894	532
UA2600	2,567,790	2,995,755	592
UA2700	3,520,954	4,107,780	692
UA2800	4,231,979	5,001,430	792
UA2900	5,378,257	6,356,122	892
UA2976	5,765,320	6,918,384	968

Architecture

The basic element of the UA2 family is called a cell. One cell can typically implement between one to four FPGA gates. Cells are located contiguously through out the core of the device, with routing resources provided in three to four metal layers above the cells. Some cell blockage does occur due to routing, and utilization will be significantly greater with three metal routing than two. The sizes listed in the Product Outline are estimated usable amounts using three metal layers. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required to match any FPGA or PLD pinout.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O buffer interfacing

I/O Flexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator could be located close to each buffer.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull up or pull down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 2 to 18mA at 3.3V according to the chosen option. 36mA achievable, using 2 pads.

Slew Rate Controlled Output Buffer

In this mode, the p– and n–output transistors commands are delayed, so that they are never set “ON” simultaneously, resulting in a low switching current and low noise. These buffers are dedicated to very high load drive.

2.5V Compatibility

The UA2 series of ULC’s is fully capable of supporting high–performance operation at 2.5V for core or 3.3V for periphery. The performance specifications of any given ULC design however, must be explicitly specified as 2.5V, 3.3V or both.

Power Supply and Noise Protection

The speed and density of the UA2 technology cause large switching current spikes, for example, when:

- 16 high current output buffers switch simultaneously, or
- 10% of the 700 000 gates are switching within a window of 1ns.

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the setting time of the current and causes voltage drops on the power supply lines. These drops can affect the behavior of the circuit itself or disturb the external application (ground bounce).

In order to improve the noise immunity of the UA2 core matrix, several mechanisms have been implemented inside the UA2 arrays. Two types of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

I/O buffers switching protection

Three features are implemented to limit the noise generated by the switching current:

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix switching current protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added:

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.
- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial VDD and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the VDD supply of the matrix to the external world via the output buffers.

Electrical Characteristics

Absolute Maximum Ratings

Max Supply Voltage (V_{DD})	2.7V
Max Supply Voltage (V_{DD5})	3.6V
Input Voltage (V_{IN})V_{DD} V_{DD}	+ 0.5V
3.3V Tolerant/CompliantV_{DD5}	+ 0.5V
Storage Temperature	-65° to 150°C
Operating Ambient Temperature	-40° to 85°C

Recommended Operating Range

V_{DD}	2.5V ± 5% or 3.3V ± 5%
Operating Temperature:	
Commercial	0° to 70°C
Industrial	-40° to 85°C

DC Characteristics

2.5V Specified at V_{DD} = +2.5V +/- 5%

Symbol	Parameter	Buffer	Min.	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-40		+85	°C	
VDD	Supply Voltage	All	2.3	2.5	2.7	V	
I_{IH}	High level input current	CMOS			10	µA	$V_{IN}=V_{DD}$,$V_{DD}=V_{DD}$(max)
		PCI			10		
I_{IL}	Low Level input current	CMOS	-10			µA	$V_{IN}=V_{SS}$,$V_{DD}=V_{DD}$ (max)
		PCI					
I_{OZ}	High-Impedance State Output Current	All	-10		10	µA	V_{IN} = V_{DD} or V_{SS}, V_{DD} = V_{DD} (max), No Pull-up
I_{OS}	Output short-circuit current	PO11		9		mA	V_{OUT} = V_{DD}, V_{DD} = V_{DD} (max) V_{OUT} = V_{SS}, V_{DD}= V_{DD} (max)
		PO11		6			
V_{IH}	High-level Input Voltage	CMOS	0.7V_{DD}			V	
		PCI	0.475V_{DD}				
		CMOS Schmitt	0.7V_{DD}	1.5			
V_{IL}	Low-Level Input Voltage	CMOS			0.3V_{DD}	V	
		PCI			0.325V_{DD}		
		CMOS Schmitt		1.0	0.3V_{DD}		
V_{hys}	Hysteresis	CMOS Schmitt		0.5		V	
V_{OH}	High-Level output voltage	PO11	0.7V_{DD}			V	I_{OH} = 1.4mA, V_{DD} = V_{DD} (min) I_{OH} = -500 µA
		PCI	0.9V_{DD}				
V_{OL}	Low-Level output voltage	PO11			0.4	V	I_{OL} = 1.4 mA, V_{DD} = V_{DD} (min) I_{OL} = 1.5 mA
		PCI			0.1V_{DD}		

3.3V Specified at VDD = +3.3V +/- 5%

Symbol	Parameter	Buffer	Min	Typ	Max	Unit	Conditions
TA	Operating Temperature	All	-40		+85	°C	
VDD	Supply Voltage	All	3.0	3.3	3.6	V	
I_{IH}	High level input current	CMOS			10	µA	$V_{IN}=V_{DD}, V_{DD}=V_{DD}$(max)
		PCI			10		
I_{IL}	Low Level input current	CMOS	-10			µA	$V_{IN}=V_{SS}, V_{DD}=V_{DD}$ (max)
		PCI					
I_{OZ}	High-Impedance State Output Current	All	-10		10	µA	$V_{IN} = V_{DD}$ or V_{SS}, $V_{DD} = V_{DD}$ (max), No Pull-up
I_{OS}	Output short-circuit current	PO11		14		mA	$V_{OUT} = V_{DD}$, $V_{DD} = V_{DD}$ (max)
		PO11		-9			$V_{OUT} = V_{SS}$, $V_{DD} = V_{DD}$ (max)
V_{IH}	High-level Input Voltage	CMOS,LVTTL	2.0			V	
		PCI	0.475V_{DD}				
		CMOS Schmitt	2.0	1.7			
V_{IL}	Low-Level Input Voltage	CMOS			0.8	V	
		PCI			0.325V_{DD}		
		CMOS/TTL-level Schmitt		1.1	0.8		
V_{hys}	Hysteresis	TTL-level Schmitt		0.6		V	
V_{OH}	High-Level output voltage	PO11	0.7V_{DD}			V	I_{OH} = 2mA, $V_{DD} = V_{DD}$ (min) I_{OH} = -500 µA
		PCI	0.9V_{DD}				
V_{OL}	Low-Level output voltage	PO11			0.4	V	I_{OL} = 2 mA, $V_{DD} = V_{DD}$ (min) I_{OL} = 1.5 mA
		PCI			0.1V_{DD}		

I/O Buffer

Symbol	Parameter	Typ	Unit	Conditions
C_{IN}	Capacitance, Input Buffer (Die)	2.4	pF	3.3V
C_{OUT}	Capacitance, Output Buffer (Die)	5.6	pF	3.3V
$C_{I/O}$	Capacitance, Bidirectional	6.6	pF	3.3V

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