PROCESS CP195

Small Signal Transistor

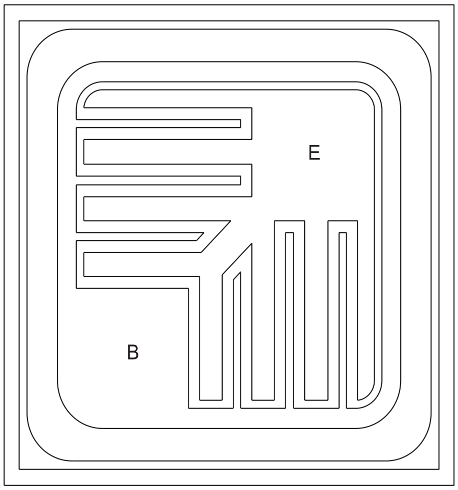
NPN - Amp/Switch Transistor Chip

Central™
Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	30 x 30 MILS
Die Thickness	7.0 MILS
Base Bonding Pad Area	8.0 x 8.0 MILS
Emitter Bonding Pad Area	7.6 x 7.6 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 10,000Å

GEOMETRY



BACKSIDE COLLECTOR

R1

GROSS DIE PER 4 INCH WAFER

12,550

PRINCIPAL DEVICE TYPES

2N5682
2N3501

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

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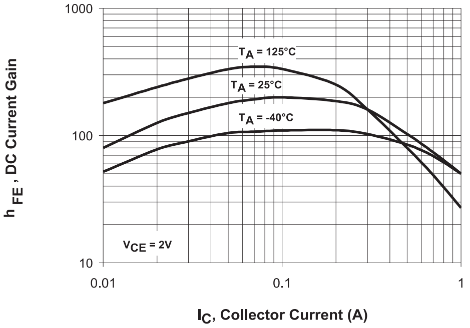
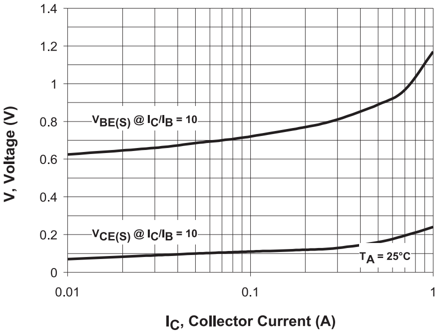
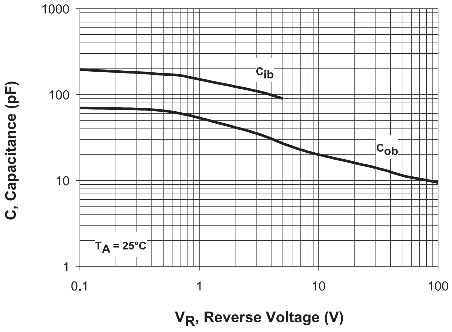
PROCESS CP195
Typical Electrical Characteristics



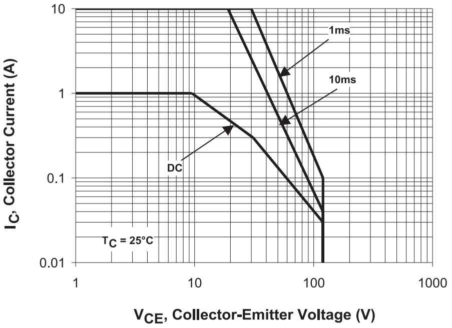
DC Current Gain



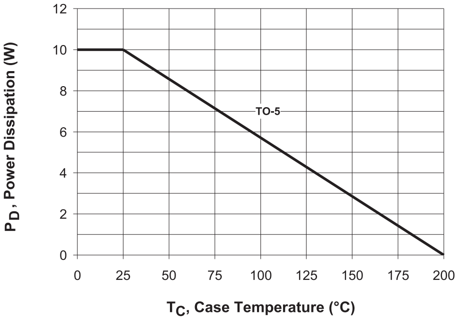
"ON" Voltage



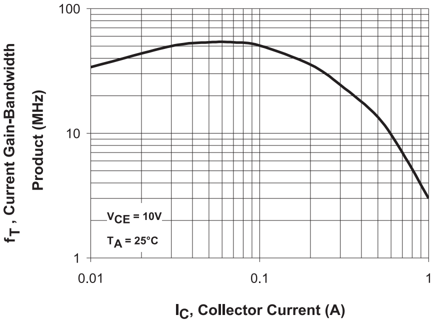
Capacitance



Safe Operating Area



Power Derating



Current Gain-Bandwidth Product

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