

**CTLT3410-M521 (NPN)
CTLT7410-M521 (PNP)
SURFACE MOUNT
COMPLEMENTARY SILICON
LOW $V_{CE(SAT)}$ TRANSISTORS**



Top View Bottom View

TLM521

CTLT3410-M521 (NPN) Marking Code: CB
CTLT7410-M521 (PNP) Marking Code: CD

MAXIMUM RATINGS: ($T_A=25^{\circ}\text{C}$)

	SYMBOL		UNITS
Collector-Base Voltage	V_{CB0}	40	V
Collector-Emitter Voltage	V_{CEO}	25	V
Emitter-Base Voltage	V_{EBO}	6.0	V
Collector Current	I_C	1.0	A
Collector Current (Peak)	I_{CM}	1.5	A
Power Dissipation	P_D	0.9	W *
Operating and Storage			
Junction Temperature	T_J, T_{stg}	-65 to +150	$^{\circ}\text{C}$
Thermal Resistance	Θ_{JA}	139	$^{\circ}\text{C/W} *$

ELECTRICAL CHARACTERISTICS: ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	TYP			UNITS
		MIN	NPN	PNP	
I_{CBO}	$V_{CB}=40\text{V}$				nA
I_{EBO}	$V_{EB}=6.0\text{V}$				nA
BV_{CB0}	$I_C=100\mu\text{A}$	40			V
BV_{CEO}	$I_C=10\text{mA}$	25			V
BV_{EBO}	$I_E=100\mu\text{A}$	6.0			V
$V_{CE(SAT)}$	$I_C=50\text{mA}, I_B=5.0\text{mA}$		20	25	mV
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=10\text{mA}$		35	40	mV
$V_{CE(SAT)}$	$I_C=200\text{mA}, I_B=20\text{mA}$		75	80	mV
$V_{CE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$		130	150	mV
$V_{CE(SAT)}$	$I_C=800\text{mA}, I_B=80\text{mA}$		200	220	mV
$V_{CE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		250	275	mV
$V_{BE(SAT)}$	$I_C=800\text{mA}, I_B=80\text{mA}$				1.1 V
$V_{BE(ON)}$	$V_{CE}=1.0\text{V}, I_C=10\text{mA}$				0.9 V
h_{FE}	$V_{CE}=1.0\text{V}, I_C=10\text{mA}$	100			
h_{FE}	$V_{CE}=1.0\text{V}, I_C=100\text{mA}$	100			300
h_{FE}	$V_{CE}=1.0\text{V}, I_C=500\text{mA}$	100			
h_{FE}	$V_{CE}=1.0\text{V}, I_C=1.0\text{A}$	50			

* FR-4 Epoxy PCB with copper mounting pad area of 33mm^2

continued on next page

CentralTM

Semiconductor Corp.

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTLT3410-M521 and CTLT7410-M521 are Low $V_{CE(SAT)}$ transistors in a very small leadless 1x2mm surface mount package, designed for applications where small size, operational efficiency, and low energy consumption are prime requirements. Due to the leadless package design these devices are capable of dissipating up to 3 times the power of similar devices in comparable sized surface mount packages.

FEATURES:

- High Operational Efficiency
- High Collector Current
- High Power to Footprint Ratio
- Small TLM 1x2mm case
- $V_{CE(SAT)}$ @ 1.0A = 250mV (Typ)

APPLICATIONS:

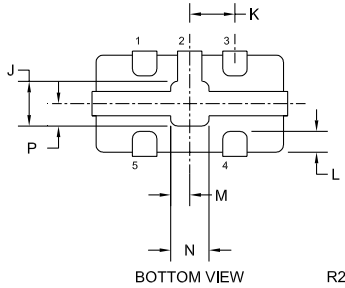
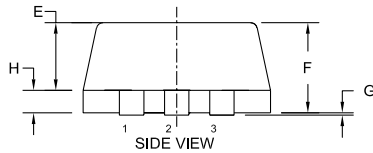
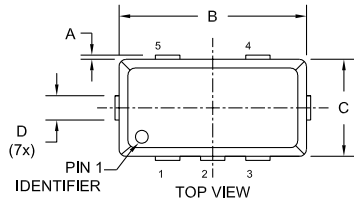
- DC/DC Converters
- Switching Circuits
- LCD Backlighting
- Battery Powered Portable Equipment

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ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_T	$V_{CE}=10\text{V}$, $I_C=50\text{mA}$, $f=100\text{MHz}$	100			MHz
C_{ob}	$V_{CB}=10\text{V}$, $I_E=0$, $f=1.0\text{MHz}$ (CTLT3410-M521)			10	pF
C_{ob}	$V_{CB}=10\text{V}$, $I_E=0$, $f=1.0\text{MHz}$ (CTLT7410-M521)			15	pF

TLM521 CASE - MECHANICAL OUTLINE



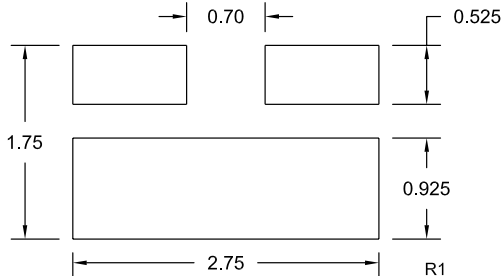
SYMBOL	DIMENSIONS		DIMENSIONS	
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.005	—	0.125
B	0.075	0.083	1.900	2.100
C	0.035	0.043	0.900	1.100
D	0.007	0.012	0.170	0.300
E	0.026	0.030	0.650	0.750
F	0.031	0.039	0.800	1.000
G	0.000	0.002	0.000	0.050
H	0.006	0.010	0.150	0.250
J	0.013	0.021	0.330	0.530
K	—	0.020	—	0.500
L	0.004	0.014	0.100	0.350
M	0.002	0.010	0.060	0.260
N	0.009	0.017	0.220	0.420
P	0.005	0.013	0.120	0.320

TLM521 (REV: R2)

LEAD CODE:

- 1) COLLECTOR
- 2) COLLECTOR
- 3) COLLECTOR
- 4) BASE
- 5) EMITTER

Suggested mounting pad layout
for maximum power dissipation
(Dimensions in mm)

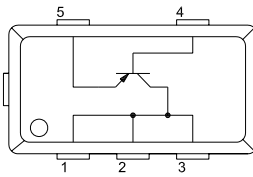
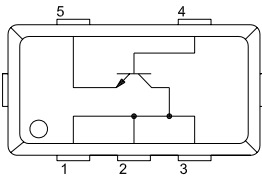


For standard mounting refer
to TLM521 Package Details

PIN CONFIGURATION

CTLT3410-M521 (NPN)

CTLT7410-M521 (PNP)



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