CH7015 SDTV / HDTV Encoder

Features

- VGA to SDTV conversion supporting graphics resolutions up to 1024x768
- Analog YPrPb output for HDTV
- HDTV support for 480p, 576p, 720p, 1080i and 1080p
- Macrovision™ 7.1.L1 copy protection support
- Programmable digital input interface supporting RGB and YCrCb input data formats
- True scale rendering engine supports under-scan in all TV output resolutions
- Text enhancement filter
- Adaptive flicker filter with up to 7 lines of filtering
- Interlaced to progressive scan conversion for DVD
- Support for NTSC, PAL and HDTV formats
- Support for SCART connector
- Outputs CVBS, S-Video, RGB and YPrPb
- Support for Wide Screen Signaling (WSS)
- TV / Monitor connection detect
- Programmable power management
- Four 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 48-pin LQFP package

1.0 General Description

The CH7015 is a Display Controller device which accepts a digital graphics input signal, and encodes and transmits data through a 10-bit high speed DAC. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL TV standards (SDTV), as well as analog HDTV interface standards and graphics standards up to UXGA. The device accepts data over one 12-bit wide variable voltage data port which supports 5 different data formats including RGB and YCrCb.

The TV-Out processor will perform non-interlace to interlace conversion with scaling and flicker filter, and encode data into any of the NTSC or PAL video standards. The scaling and flicker filter is adaptive and programmable to enable superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal under-scan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision™. ITU-R BT.656 interlaced video can also be input and scan converted to non-interlaced video.

In addition to TV encoder modes, bypass modes are included which perform color space conversion to HDTV standards and generate and insert HDTV sync signals, or output VGA style analog RGB for use as a CRT DAC.

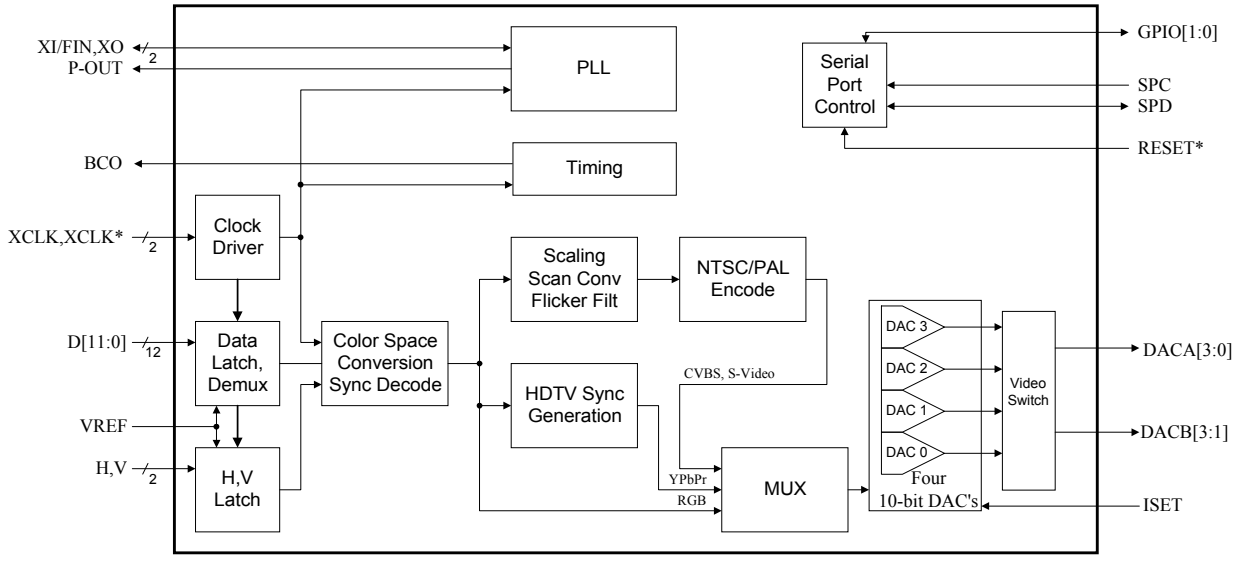

Figure 1: Functional Block Diagram

2.0 PIN-OUT

2.1 Package Diagram

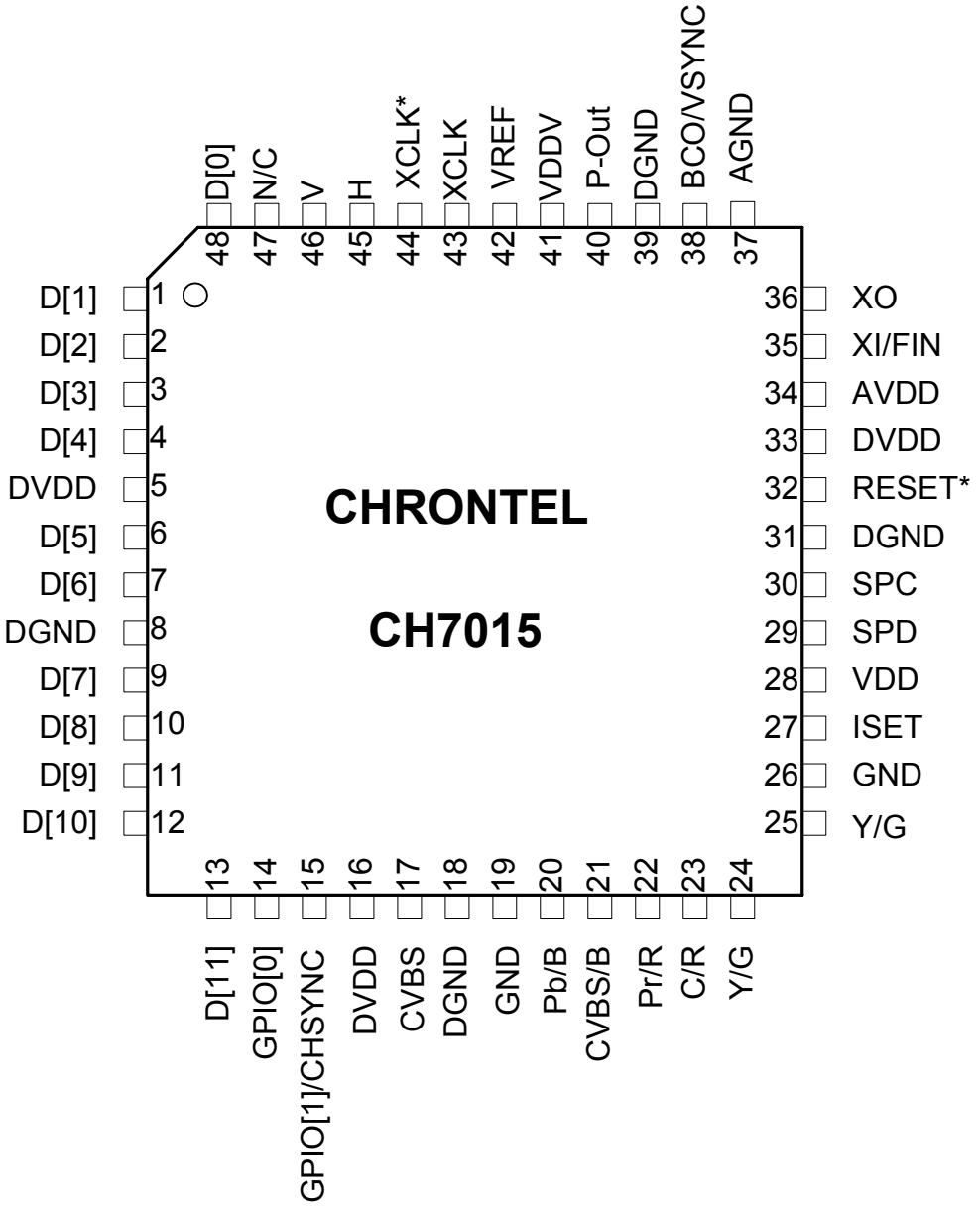

Figure 2: 48-Pin LQFP Package

2.2 Pin Description

Table 1: Pin Description

Pin #	Type	Symbol	Description
1-4, 6,7, 9-13, 48	In	D[11]-D[0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV, and the VREF signal is used as the threshold level.
14	In/Out	GPIO0	**General Purpose Input – Output0** (weak internal pull-up) This pin provides general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up. The internal pull-up will be to the DVDD supply.
15	In/Out	GPIO1 / CHSYNC	**General Purpose Input – Output1** (weak internal pull-up) This pin provides general purpose I/O controlled via the serial port. This allows an external switch to be used to select NTSC or PAL at power-up. The internal pull-up will be to the DVDD supply. It can also be configured to output composite or horizontal sync.
17	Out	CVBS (DAC3)	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load. During bypass modes this output is valid only if the data format is compatible with one of the TV-Out display modes.
20	Out	Pb/B (DACB0)	**Pb / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to the Pb component of YPrPb or blue (for VGA bypass).
21	Out	CVBS/B (DACA0)	**Composite Video / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be composite video or blue (for SCART type 1 connections).
22	Out	Pr/R (DACB2)	**Pr / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the Pr component of YPrPb or red (for VGA bypass)
23	Out	C/R (DACA2)	**Chroma / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video chrominance or red (for SCART type 1 connections).
24	Out	Y/G (DACB1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the luminance component of YPrPb or green (for VGA bypass)
25	Out	Y/G (DACA1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video luminance or green (for SCART type 1 connections).
27	In	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and GND (pin 24 or 26) using short and wide traces.
29	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to VDDV. Outputs are driven from 0 to VDDV. The serial port addresses for the CH7015 and CH7205 are 75h and 76h respectively.
30	In	SPC	**Serial Port Clock Input** This pin functions as the clock pin of the serial port and operates with inputs from 0 to VDDV.
32	In	RESET*	**Reset * Input** (Internal pull-up) When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port.
35	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.

Table 1: Pin Description ***(continued)***

Pin #	Type	Symbol	Description
36	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
38	Out	BCO	**Buffered Clock Output** This output pin provides selectable buffered clocks to be output, driven by the DVDD supply. The output clock can be selected using the BCO register. The levels are 0 to DVDD.
40	Out	P-Out	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
42	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
43, 44	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity used can be selected by the MCP control bit.
45	In/Out	H	**Horizontal Sync Input / Output** When the SYO control bit is low, this pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV, and the VREF signal is used as the threshold level. This pin must be used as an input in all bypass modes. When the SYO control bit is high, the device will output a horizontal sync pulse, 64 pixels wide. The output is driven from the DVDD supply. This output is valid with TV-Out operation.
46	In/Out	V	**Vertical Sync Input / Output** When the SYO control bit is low, this pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV, and the VREF signal is used as the threshold level. This pin must be used as an input in all bypass modes. When the SYO control bit is high, the device will output a vertical sync pulse one line wide. The output is driven from the DVDD supply. This output is valid with TV-Out operation.
5,16,33	Power	DVDD	**Digital Supply Voltage** (3.3V)
8,18,31,39	Power	DGND	**Digital Ground**
41	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
34	Power	AVDD	**PLL Supply Voltage** (3.3V)
37	Power	AGND	**PLL Ground**
28	Power	VDD	**DAC Supply Voltage** (3.3V)
19,26	Power	GND	**DAC Ground**

3.0 PACKAGE DIMENSIONS

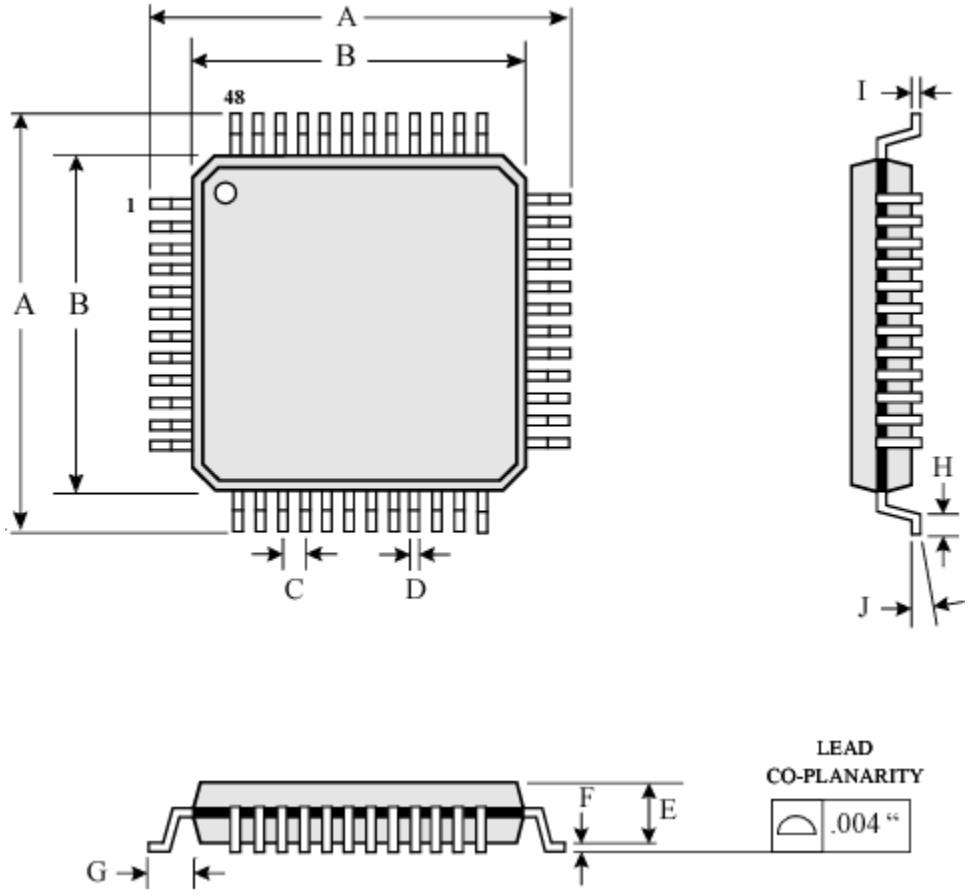

Table of Dimensions

No. of Leads		SYMBOL									
48 (7 X 7 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	9	7	0.5	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 3: 48 Pin LQFP Package

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ORDERING INFORMATION			
Part Number	Package Type	Number of Pins	Voltage Supply
CH7015A-T	LQFP	48	3.3V

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