CS4392

24-Bit, 192 kHz Stereo DAC with Volume Control

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 114 dB Dynamic Range
- 100 dB THD+N
- Up to 192kHz Sample Rates
- Direct Stream Digital Mode
- Low Clock Jitter Sensitivity
- Single +5 V Power Supply
- Selectable Digital Filters
  - Fast and Slow roll-off
- Volume Control with Soft Ramp
  - 1 dB Step Size
  - Zero Crossing Click-Free Transitions
- Direct Interface with 5 V to 1.8 V Logic
- ATAPI mixing functions
- Pin compatible with the CS4391

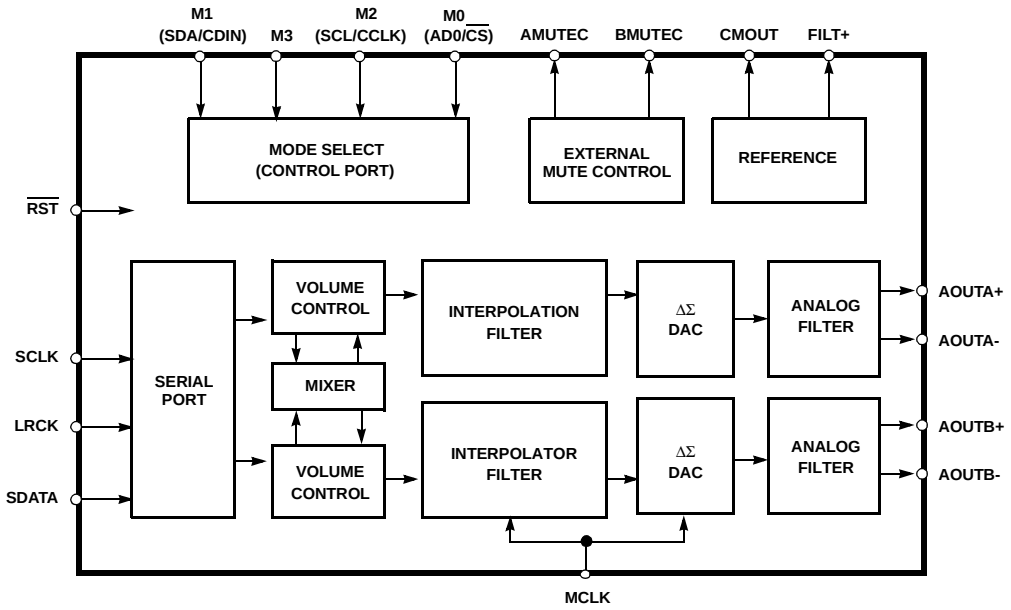
Description

The CS4392 is a complete stereo digital-to-analog system including digital interpolation, fifth-order delta-sigma digital-to-analog conversion, digital de-emphasis, volume control, channel mixing and analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, and a high tolerance to clock jitter.

The CS4392 accepts PCM data at sample rates from 4 kHz to 192 kHz, DSD audio data, has selectable digital filters, and consumes very little power. These features are ideal for DVD, SACD players, A/V receivers, CD and set-top box systems. The CS4392 is pin and register compatible with the CS4391, making easy performance upgrades possible.

ORDERING INFORMATION

CS4392-KS	-10 to 70 °C	20-pin SOIC
CS4392-KZ	-10 to 70 °C	20-pin TSSOP
CDB4392		Evaluation Board



Advance Product Information

This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

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1. CHARACTERISTICS/SPECIFICATIONS

ANALOG CHARACTERISTICS

(T_A = 25° C; Logic "1" = VL = VA; Logic "0" = AGND; Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; SCLK = 3.072 MHz, Sample Rate = 48, 96, or 192 kHz, 24-bit data, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified. Test load R_L = 3 kΩ, C_L = 10 pF)

Parameter		Symbol	VA = 5 V Min	Typ	Max	Unit
Dynamic Performance - Single Speed Mode (48kHz)						
Dynamic Range (Note 1)	unweighted		TBD	111	-	dB
	A-Weighted		TBD	114	-	dB
Total Harmonic Distortion + Noise (Note 1)	0 dB	THD+N	-	-100	TBD	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	TBD	dB
Idle Channel Noise / Signal-to-Noise Ratio			-	114	-	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB
Dynamic Performance - Double Speed Mode (96kHz)						
Dynamic Range (Note 1)	unweighted		TBD	111	-	dB
	A-Weighted		TBD	114	-	dB
Total Harmonic Distortion + Noise (Note 1)	0 dB	THD+N	-	-100	TBD	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	TBD	dB
Idle Channel Noise / Signal-to-Noise Ratio			-	114	-	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB
Dynamic Performance - Quad Speed Mode (192kHz)						
Dynamic Range (Note 1)	unweighted		TBD	111	-	dB
	A-Weighted		TBD	114	-	dB
Total Harmonic Distortion + Noise (Note 1)	0 dB	THD+N	-	-100	TBD	dB
	-20 dB		-	-91	-	dB
	-60 dB		-	-51	TBD	dB
Idle Channel Noise / Signal-to-Noise Ratio			-	114	-	dB
Interchannel Isolation	(1 kHz)		-	100	-	dB

Parameter	Symbol	Min	Typ	Max	Units
Analog Output					
Full Scale Differential Output Voltage		TBD	1.0xVA	TBD	Vpp
Common Mode Voltage	CMOUT	-	0.5xVA	-	VDC
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
AC-Load Resistance	R_L	3	-	-	kΩ
Load Capacitance	C_L	-	-	100	pF

ANALOG CHARACTERISTICS (continued)

Parameter	Symbol	Fast Roll-Off			Slow Roll-Off			Unit
		Min	Typ	Max	Min	Typ	Max	
Combined Digital and On-chip Analog Filter Response - Single Speed Mode (Note2)								
Passband (Note 3) to -0.01 dB corner		0	-	.4535	0	-	0.4166	Fs
to -3 dB corner		0	-	.4998	0	-	0.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	-0.01	-	+0.01	dB
StopBand		.5465	-	-	.5834	-	-	Fs
StopBand Attenuation (Note 5)		90	-	-	64	-	-	dB
Group Delay	tgd	-	TBD	-	-	TBD	-	s
Passband Group Delay Deviation 0 - 20 kHz		-	-	TBD		-	TBD	s
De-emphasis Error Fs = 32 kHz		-	-	±0.23	-	-	±0.23	dB
(Relative to 1kHz) Fs = 44.1 kHz		-	-	±0.14	-	-	±0.14	dB
Fs = 48 kHz		-	-	±0.09	-	-	±0.09	dB
Combined Digital and On-chip Analog Filter Response - Double Speed Mode - 96kHz (Note 2)								
Passband (Note 4) to -0.01 dB corner		0	-	.4166	0	-	.2083	Fs
to -3 dB corner		0	-	.4998	0	-	.4998	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.5834	-	-	.7917	-	-	Fs
StopBand Attenuation (Note 5)		80	-	-	70	-	-	dB
Group Delay	tgd	-	TBD	-	-	TBD	-	s
Passband Group Delay Deviation 0 - 20 kHz		-	-	TBD	-	-	TBD	s
Combined Digital and On-chip Analog Filter Response - Quad Speed Mode - 192kHz (Note 2)								
Passband (Note 4) to -0.01 dB corner		0	-	.1046	0	-	.1042	Fs
to -3 dB corner		0	-	.4897	0	-	.4813	Fs
Frequency Response 10 Hz to 20 kHz		-0.01	-	0.01	-0.01	-	0.01	dB
StopBand		.6355	-	-	.8683	-	-	Fs
StopBand Attenuation (Note 5)		75	-	-	75	-	-	dB
Group Delay	tgd	-	TBD	-	-	TBD	-	s
Passband Group Delay Deviation 0 - 20 kHz		-	-	TBD	-	-	TBD	s
Combined Digital and On-chip Analog Filter Response - DSD Mode (Note 2)								
Passband (Note 4) to -3 dB corner		TBD	-	TBD	TBD	-	TBD	Fs
Frequency Response 10 Hz to 20 kHz		TBD	-	TBD	TBD	-	TBD	dB

Notes:
1. Triangular PDF dithered data.
2. Filter response is not tested but is guaranteed by design.
3. Valid with the recommended capacitor values on FILT+ and CMOUT as shown in Figure 5. Increasing the capacitance will also increase the PSRR.
4. Response is clock dependent and will scale with Fs.
5. For Single-Speed Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
   For Double-Speed Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.

POWER AND THERMAL CHARACTERISTICS

GND = 0 V (All voltages with respect to ground. All measurements taken with all zeros input and open outputs, unless otherwise specified.)

Parameters		Symbol	Base-rate Mode Min	Typ	Max	Units
Power Supplies						
Power Supply Current-	VA=5V	I_A	-	TBD	-	mA
Normal Operation	VL=3V	I_{D_L}	--	TBD	-	µA
Power Supply Current-	VA=5V	I_A	-	TBD	-	µA
Power Down Mode (Note 6)	VL=3V	I_{D_L}	-	TBD	-	µA
Power Supply Current-	VA=5V	I_A	-	25	-	mA
Normal Operation	VL=5V	I_{D_L}	-	TBD	-	µA
Power Supply Current-	VA=5V	I_A	-	60	-	µA
Power Down Mode (Note 6)	VL=5V	I_{D_L}	-	TBD	-	µA
Total Power Dissipation-	All Supplies=5V		-	125	-	mW
Normal Operation	VA=5V, VL=1.8V		-	TBD	-	mW
Package Thermal Resistance		θ_{JA}	-	TBD	-	°C/Watt
Power Supply Rejection Ratio (Note 7)	1 kHz	PSRR	-	60	-	dB
	60 Hz		-	40	-	dB

Notes: 6. GND = 0 V (All voltages with respect to ground. All measurements taken with all zeros input and open outputs, unless otherwise specified.) Power Down Mode is defined as $\overline{RST}$ = LO with all clocks and data lines held static.

7. Valid with the recommended capacitor values on FILT+ as shown in Figure 5. Increasing the capacitance will also increase the PSRR. NOTE: Care should be taken when selecting capacitor type, as any leakage current in excess of 1.0 µA will cause degradation in analog performance.

DIGITAL CHARACTERISTICS (T_A = 25° C)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	70%	-	-	VL
Low-Level Input Voltage	V_{IL}		-	20%	VL
Input Leakage Current	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF
Maximum MUTEC Drive Current		-	3	-	mA

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA VL	-0.3 -0.3	6.0 VA	V V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VL+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VA VL	4.75 1.8	5.0 -	5.5 VA	V V

SWITCHING CHARACTERISTICS - PCM MODES (T_A = -10 to 70° C; VL = 5.5 to 1.8 Volts; Inputs: Logic 0 = 0 V, Logic 1 = VL, CL = 20 pF)

Parameters	Symbol	Min	Typ	Max	Units
Input Sample Rate	Fs	4	-	200	kHz
LRCK Duty Cycle		45	50	55	%
MCLK Duty Cycle		40	50	60	%
SCLK Frequency		-	-	MCLK/2	Hz
SCLK Frequency Note 8		-	-	MCLK/4	Hz
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time	t_{sdh}	20	-	-	ns

Notes: 8. This serial clock is available only in Control Port Mode when the MCLK Divide bit is enabled.

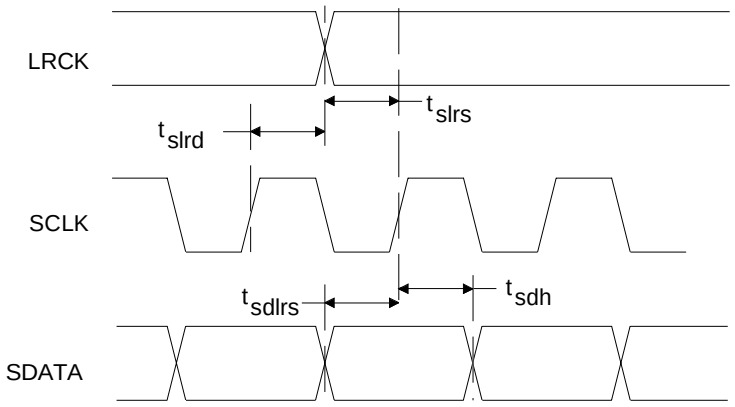


Figure 1. Serial Mode Input Timing

SWITCHING CHARACTERISTICS - DSD (T_A= -10 to 70° C; Logic 0 = AGND = DGND; Logic 1 = VL = 5.5 to 1.8 Volts; C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
MCLK Duty Cycle		40	50	60	%
DSD_SCLK Pulse Width Low	t_{sclkl}	TBD	-	-	ns
DSD_SCLK Pulse Width High	t_{sclkh}	TBD	-	-	ns
DSD_SCLK Period	t_{sclkw}	TBD	-	-	ns
DSD_L or DSD_R valid to DSD_SCLK rising setup time	t_{sdlrs}	TBD	-	-	ns
DSD_SCLK rising to DSD_L or DSD_R hold time	t_{sdh}	TBD	-	-	ns

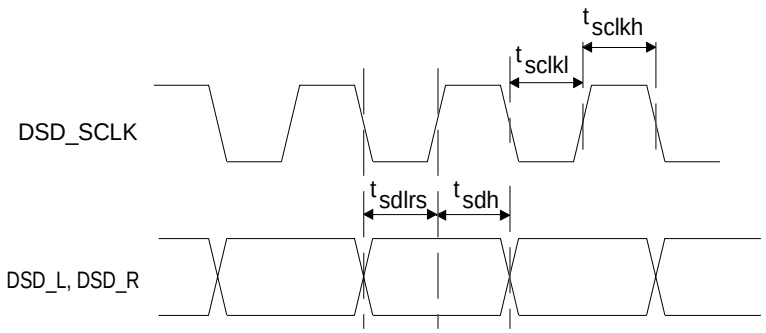


Figure 2. Direct Stream Digital - Serial Audio Input Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - TWO-WIRE MODE

(T_A = 25° C; VL = 5.5 to 1.8 Volts; Inputs: logic 0 = AGND, logic 1 = VL, C_L = 30 pF)

Parameter	Symbol	Min	Max	Unit
Two-Wire Mode				
SCL Clock Frequency	f_{scl}	-	100	KHz
RST Rising Edge to Start	t_{irs}	500	-	ns
Bus Free Time Between Transmissions	t_{buf}	4.7	-	µs
Start Condition Hold Time (prior to first clock pulse)	t_{hdst}	4.0	-	µs
Clock Low time	t_{low}	4.7	-	µs
Clock High Time	t_{high}	4.0	-	µs
Setup Time for Repeated Start Condition	t_{sust}	4.7	-	µs
SDA Hold Time from SCL Falling (Note 10)	t_{hdd}	0	-	µs
SDA Setup time to SCL Rising	t_{sud}	250	-	ns
Rise Time of Both SDA and SCL Lines	t_r	-	1	µs
Fall Time of Both SDA and SCL Lines	t_f	-	300	ns
Setup Time for Stop Condition	t_{susp}	4.7	-	µs

Notes: 9. The Two-Wire mode is compatible with the I^2C protocol.

10. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

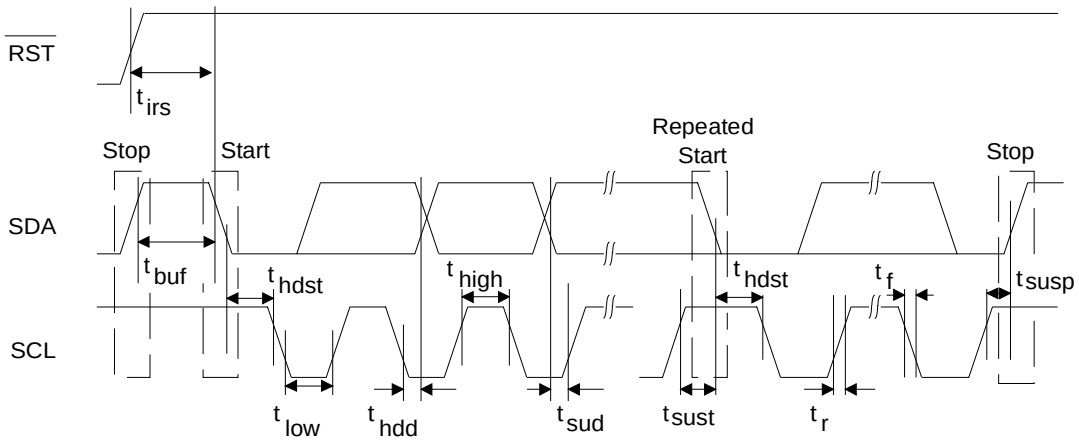


Figure 3. Two-Wire Mode Control Port Timing

SWITCHING CHARACTERISTICS - CONTROL PORT - SPI MODE

(T_A = 25° C; VL = 5.5 to 1.8 Volts; Inputs: logic 0 = AGND, logic 1 = VL, C_L = 30 pF)

Parameter		Symbol	Min	Max	Unit
SPI Mode					
CCLK Clock Frequency		f_{sclk}	-	6	MHz
RST Rising Edge to CS Falling		t_{srs}	500	-	ns
CCLK Edge to CS Falling	(Note 11)	t_{spi}	500	-	ns
$\overline{CS}$ High Time Between Transmissions		t_{csh}	1.0	-	µs
CS Falling to CCLK Edge		t_{css}	20	-	ns
CCLK Low Time		t_{scl}	66	-	ns
CCLK High Time		t_{sch}	66	-	ns
CDIN to CCLK Rising Setup Time		t_{dsu}	40	-	ns
CCLK Rising to DATA Hold Time	(Note 12)	t_{dh}	15	-	ns
Rise Time of CCLK and CDIN	(Note 13)	t_{r2}	-	100	ns
Fall Time of CCLK and CDIN	(Note 13)	t_{f2}	-	100	ns

Notes: 11. t_{spi} only needed before first falling edge of $\overline{CS}$ after $\overline{RST}$ rising edge. t_{spi} = 0 at all other times.

12. Data must be held for sufficient time to bridge the transition time of CCLK.

13. For F_{SCK} < 1 MHz

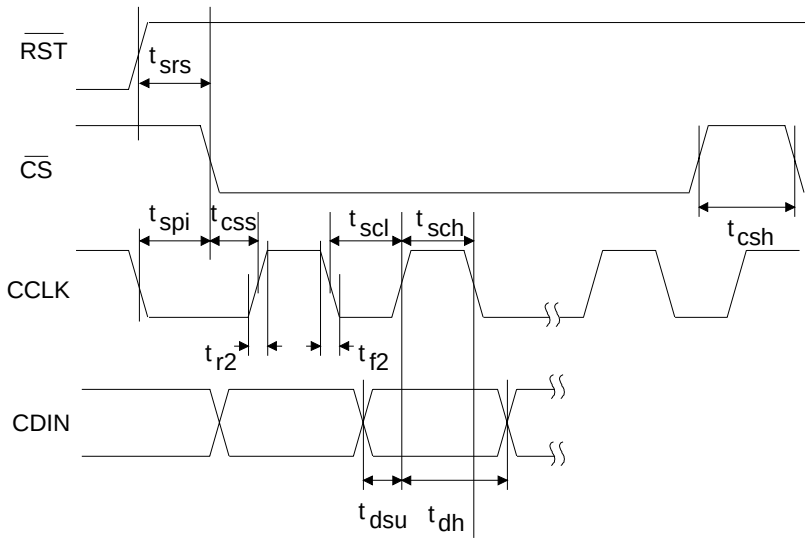


Figure 4. SPI Control Port Timing

2. TYPICAL CONNECTION DIAGRAMS

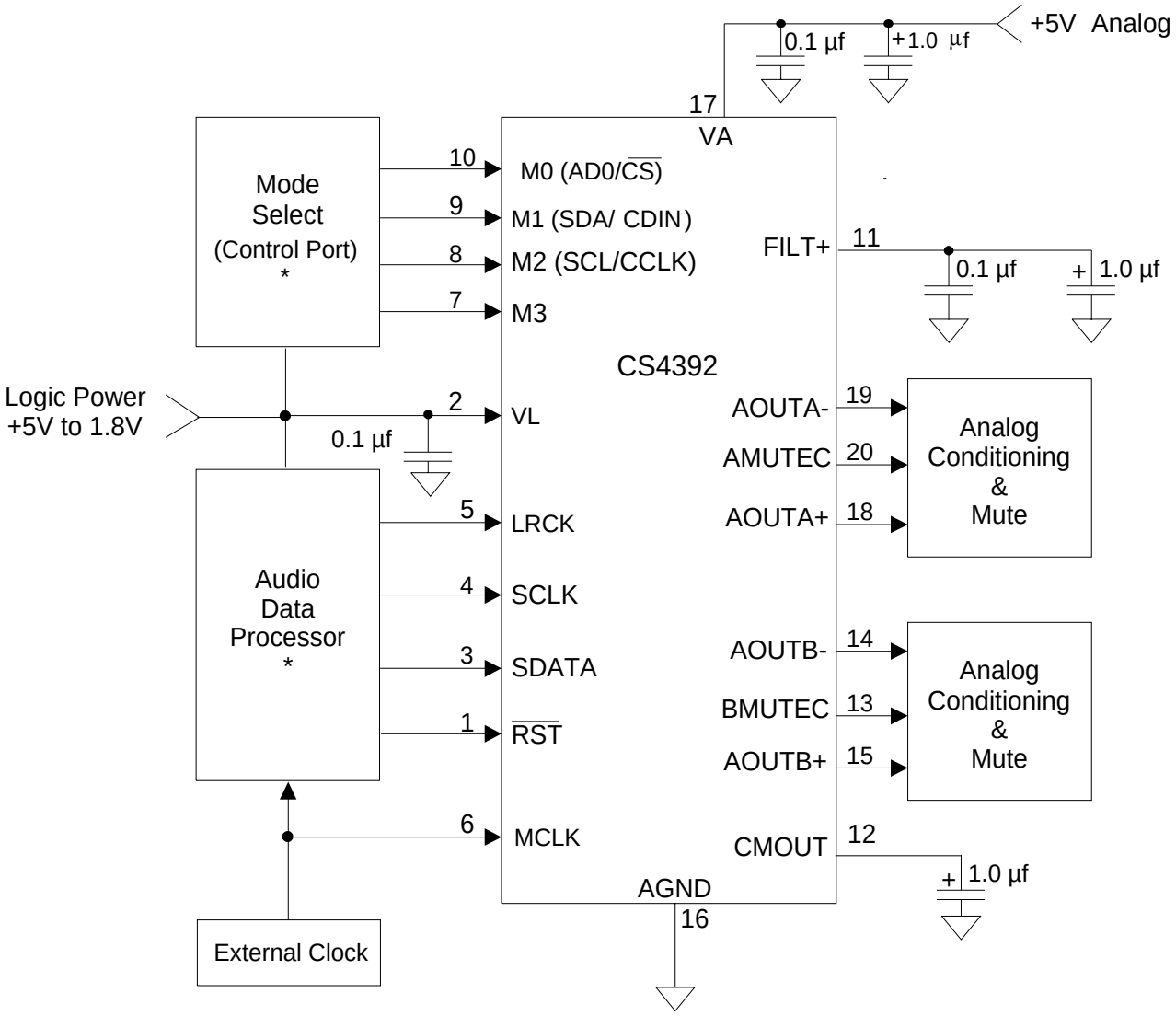


Figure 5. Typical Connection Diagram - PCM Mode

* A high logic level for all digital inputs should not exceed VL.

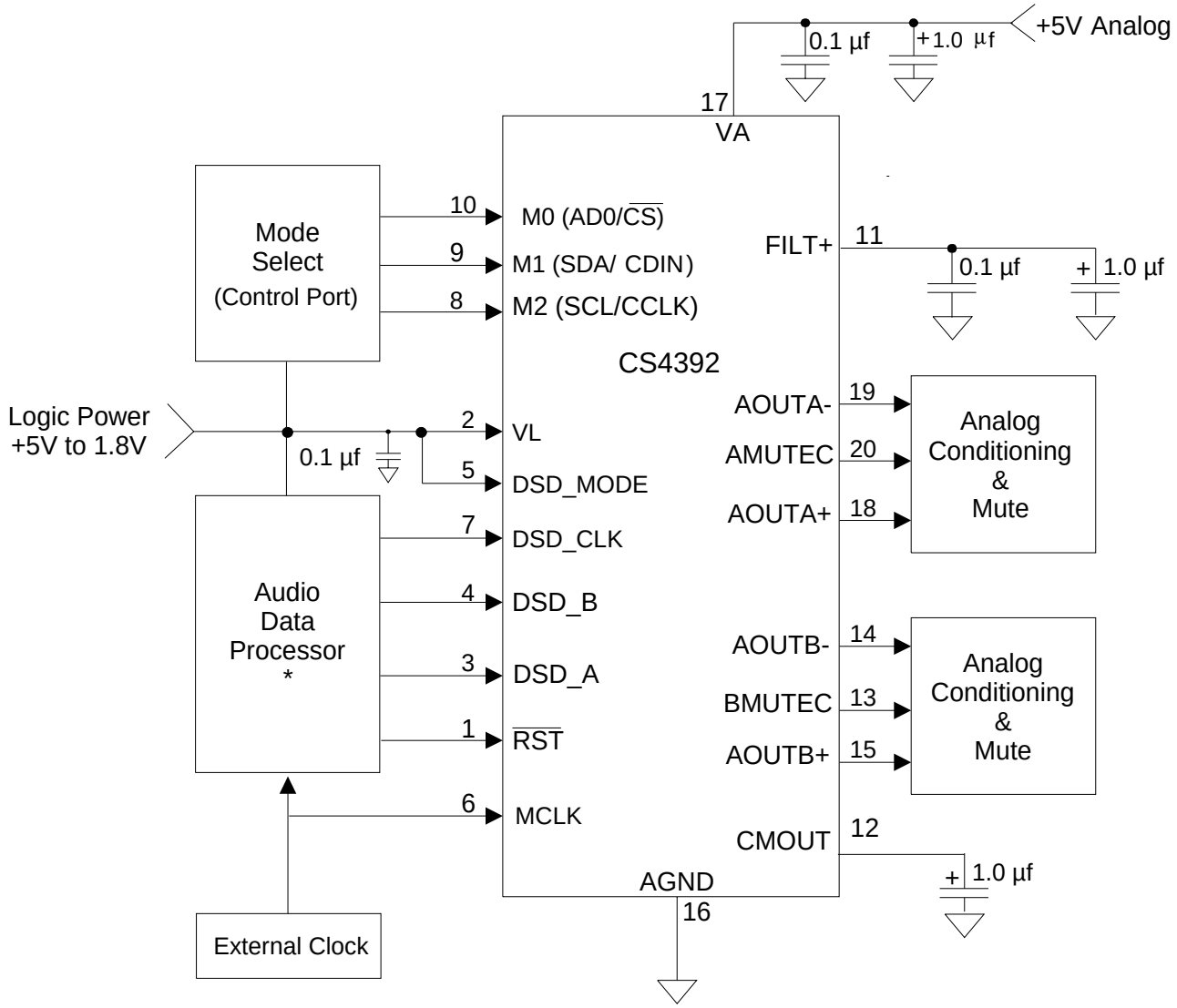


Figure 6. Typical Connection Diagram - DSD Mode

* A high logic level for all digital inputs should not exceed VL.

3. REGISTER QUICK REFERENCE

This table shows the register names and their associated default values.

Addr	Function	7	6	5	4	3	2	1	0
01h	Mode Control 1	AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0
		1	0	0	0	0	0	0	0
02h	Volume and MIxing Control	A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0
		0	1	0	0	1	0	0	1
03h	Channel A Volume Control	MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
		0	0	0	0	0	0	0	0
04h	Channel B Volume Control	MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0
		0	0	0	0	0	0	0	0
05h	Mode Control 2	INVERT_A	INVERT_B	CPEN	PDN	MUTEC A = B	FREEZE	MCLK Divide	Reserved
		0	0	0	1	0	0	0	0
06h	Mode Control 3	Reserved	Reserved	Reserved	Filt_rolloff	rst_rmp_up	rst_rmp_dwn	Reserved	Reserved
		0	0	0	0	0	0	0	0
07h	Chip ID	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
		1	0	0	0	-	-	-	-

4. REGISTER DESCRIPTION

** All registers are read/write in Two-Wire mode and write only in SPI mode, unless otherwise noted**

4.1 Mode Control 1 - Address 01h

7	6	5	4	3	2	1	0
AMUTE	DIF2	DIF1	DIF0	DEM1	DEM0	FM1	FM0

4.1.1 Auto-Mute (Bit 7)

Function:

The Digital-to-Analog converter output will mute following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. Detection and muting is done independently for each channel. (However, Auto-Mute detection and muting can become dependent on either channel if the Mute A = B function is enabled.) The common mode on the output will be retained and the Mute Control pin for that channel will go active during the mute period. The muting function is effected, similar to volume control changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register.

4.1.2 Digital Interface Formats (Bits 6:4)

Function:

PCM Mode - The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Table 1 and Figures 9-14.

DIF2	DIF1	DIFO	DESCRIPTION	Format	Figure
0	0	0	Left Justified, up to 24-bit data (default)	0	9
0	0	1	I^2S, up to 24-bit data	1	10
0	1	0	Right Justified, 16-bit Data	2	11
0	1	1	Right Justified, 24-bit Data	3	12
1	0	0	Right Justified, 20-bit Data	4	13
1	0	1	Right Justified, 18-bit Data	5	14
1	1	0	Reserved		
1	1	1	Reserved		

Table 1. Digital Interface Formats - PCM Modes

DSD Mode - The relationship between the oversampling ratio of the DSD audio data and the required Master clock to DSD data rate is defined by the Digital interface Format pins. Note that the Functional Mode registers must be set to DSD Mode. See Table 2 for register options.

DIF2	DIF1	DIFO	DESCRIPTION
0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate (default)
0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 2. Digital Interface Formats - DSD Mode

4.1.3 De-Emphasis Control (Bits 3:2)

Function:

Implementation of the standard 15 µs/50 µs digital de-emphasis filter response, Figure 7, requires re-configuration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. NOTE: De-emphasis is available only in Single-Speed Mode. See Table 3 below.

DEM1	DEMO	DESCRIPTION
0	0	Disabled (default)
0	1	44.1 kHz de-emphasis
1	0	48 kHz de-emphasis
1	1	32 kHz de-emphasis

Table 3. De-Emphasis Mode Selection

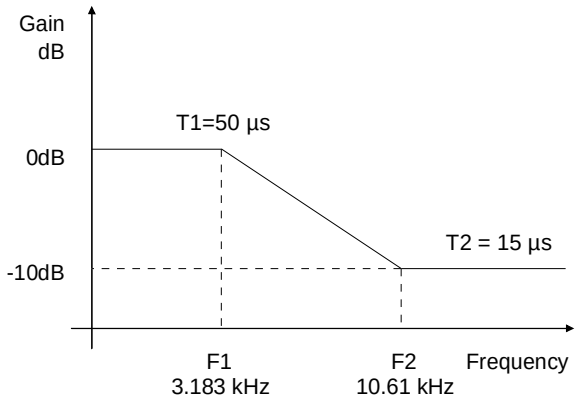


Figure 7. De-Emphasis Curve

4.1.4 Functional Mode (Bits 1:0)

Function:

Selects the required range of input sample rates or DSD Mode. See Table 4

FM1	FM0	MODE
0	0	Single-Speed Mode: 4 to 50 kHz sample rates (default)
0	1	Double-Speed Mode: 50 to 100 kHz sample rates
1	0	Quad-Speed Mode: 100 to 200 kHz sample rates
1	1	Direct Stream Digital Mode

Table 4. Functional Mode Selection

4.2 Volume and Mixing Control (Address 02h)

7	6	5	4	3	2	1	0
A = B	Soft	Zero Cross	ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0

4.2.1 Channel A Volume = Channel B Volume (Bit 7)

Function:

The AOUTA and AOUTB volume levels are independently controlled by the A and the B Channel Volume Control Bytes when this function is disabled. The volume on both AOUTA and AOUTB are determined by the A Channel Volume Control Byte and the B Channel Byte is ignored when this function is enabled.

4.2.2 Soft Ramp or Zero Cross Enable (Bits 6:5)

Function:

Soft Ramp Enable

Soft Ramp allows level changes, both muting and attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1dB per 8 left/right clock periods.

Zero Cross Enable

Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel.

Soft Ramp and Zero Cross Enable

Soft Ramp and Zero Cross Enable dictates that signal level changes, either by attenuation changes or muting, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period between 512 and 1024 sample periods (10.7 ms to 21.3 ms at 48 kHz sample rate) if the signal does not encounter a zero crossing. The zero cross function is independently monitored and implemented for each channel. See Table 5

SOFT	ZERO	Mode
0	0	Changes to affect immediately
0	1	Zero Cross enabled
1	0	Soft Ramp enabled (default)
1	1	Soft Ramp and Zero Cross enabled

Table 5. Soft Cross or Zero Cross Mode Selection

4.2.3 ATAPI Channel Mixing and Muting (Bits 4:0)

Function:

The CS4392 implements the channel mixing functions of the ATAPI CD-ROM specification. See Table 6 on page 19

ATAPI4	ATAPI3	ATAPI2	ATAPI1	ATAPI0	AOUTA	AOUTB
0	0	0	0	0	MUTE	MUTE
0	0	0	0	1	MUTE	bR
0	0	0	1	0	MUTE	bL
0	0	0	1	1	MUTE	b[(L+R)/2]
0	0	1	0	0	aR	MUTE
0	0	1	0	1	aR	bR
0	0	1	1	0	aR	bL
0	0	1	1	1	aR	b[(L+R)/2]
0	1	0	0	0	aL	MUTE
0	1	0	0	1	aL	bR
0	1	0	1	0	aL	bL
0	1	0	1	1	aL	b[(L+R)/2]
0	1	1	0	0	a[(L+R)/2]	MUTE
0	1	1	0	1	a[(L+R)/2]	bR
0	1	1	1	0	a[(L+R)/2]	bL
0	1	1	1	1	a[(L+R)/2]	b[(L+R)/2]
1	0	0	0	0	MUTE	MUTE
1	0	0	0	1	MUTE	bR
1	0	0	1	0	MUTE	bL
1	0	0	1	1	MUTE	[(bL+aR)/2]
1	0	1	0	0	aR	MUTE
1	0	1	0	1	aR	bR
1	0	1	1	0	aR	bL
1	0	1	1	1	aR	[(aL+bR)/2]
1	1	0	0	0	aL	MUTE
1	1	0	0	1	aL	bR
1	1	0	1	0	aL	bL
1	1	0	1	1	aL	[(aL+bR)/2]
1	1	1	0	0	[(aL+bR)/2]	MUTE
1	1	1	0	1	[(aL+bR)/2]	bR
1	1	1	1	0	[(bL+aR)/2]	bL
1	1	1	1	1	[(aL+bR)/2]	[(aL+bR)/2]

Table 6. ATAPI Decode

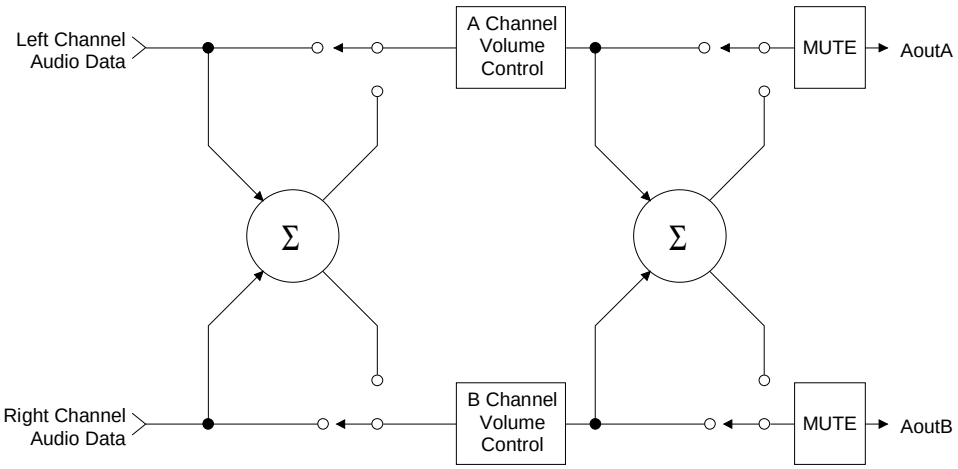


Figure 8. ATAPI Block Diagram

4.3 Channel A Volume Control - Address 03h

See 4.4 *Channel B Volume Control - Address 04h*

4.4 CHANNEL B VOLUME CONTROL - ADDRESS 04H

7	6	5	4	3	2	1	0
MUTE	VOL6	VOL5	VOL4	VOL3	VOL2	VOL1	VOL0

4.4.1 Mute (Bit 7)

Function:

The Digital-to-Analog converter output will mute when enabled. The common mode voltage on the output will be retained. The muting function is effected, similiar to attenuation changes, by the Soft and Zero Cross bits in the Volume and Mixing Control register. The MUTEC pin for that channel will go active during the mute period if the Mute function is enabled. Both the AMUTEC and BMUTEC will go active if either MUTE register is enabled and the MUTEC A = B bit (register 5) is enabled.

4.4.2 Volume Control (Bits 6:0)

Function:

The digital volume control allows the user to attenuate the signal in 1 dB increments from 0 to -127 dB. Volume settings are decoded as shown in Table 7. The volume changes are implemented as dictated by the Soft and Zero Cross bits in the Volume and Mixing Control register (see section 4.2.2).

Binary Code	Decimal Value	Volume Setting
0000000	0	0 dB
0010100	20	-20 dB
0101000	40	-40 dB
0111100	60	-60 dB
1011010	90	-90 dB

Table 7. Digital Volume Control Example Settings

4.5 Mode Control 2 - Address 05h

7	6	5	4	3	2	1	0
INVERT_A	INVERT_B	CPEN	PDN	MUTEC A = B	FREEZE	MCLK Divide	Reserved

4.5.1 Invert Signal Polarity (Bits 7:6)

Function:

When set to 1, this bit inverts the signal polarity for the appropriate channel. This is useful if a board layout error has occurred, or an other situations where a 180 degree phase shift is desirable. Default is 0.

4.5.2 Control Port Enable (Bit 5)

Function:

This bit defaults to 0, allowing the device to power-up in Stand-Alone mode. The Control port mode can be accessed by setting this bit to 1. This will allow the operation of the device to be controlled by the registers and the pin definitions will conform to Control Port Mode. To accomplish a clean power-up, the user should write 30h to register 5 within 10 ms following the release of Reset.

4.5.3 Power Down (Bit 4)

Function:

The device will enter a low-power state whenever this function is activated (set to 1). The power-down bit defaults to 'enabled' (1) on power-up and must be disabled before normal operation will begin. The contents of the control registers are retained when the device is in power-down.

4.5.4 AMUTEC = BMUTEC (Bit 3)

Function:

When this function is enabled, the individual controls for AMUTEC and BMUTEC are internally connected through a AND gate prior to the output pins. Therefore, the external AMUTEC and BMUTEC pins will go active only when the requirements for both AMUTEC and BMUTEC are valid.

4.5.5 Freeze (Bit 2)

Function:

This function allows modifications to the control port registers without the changes taking effect until Freeze is disabled. To make multiple changes in the Control port registers take effect simultaneously, set the Freeze Bit, make all register changes, then Disable the Freeze bit.

4.5.6 Master Clock Divide (Bit 1)

Function:

This function allows the user to select an internal divide by 2 of the Master Clock. This selection is required to access the higher Master Clock rates as shown in 8.

4.6 Mode Control 3 - Address 06h

B7	B6	B5	B4	B3	B2	B1	B0
Reserved	Reserved	Reserved	Filt_rolloff	rst_rmp_up	rst_rmp_dwn	Reserved	Reserved

4.6.1 Interpolation Filter Select (Bit 4)

Function:

This Function allows the user to select whether the Interpolation Filter has a fast (set to 0 - default) or slow (set to 1) roll off. The - 3dB corner is approximately the same for both filters, but the slope of the roll of is greater for the 'fast' roll off filter.

4.6.2 Soft Volume Ramp-up after Reset (Bit 3)

Function:

This function allows the user to control whether a soft ramp up in volume is applied when reset is released either by the reset pin or internal to the chip. The modes are as follows:

0 - An instantaneous change is made from max attenuation to the control port volume setting on release of reset (default setting).
1 - Volume is ramped up using the soft-ramp settings in Bits 6:5 of register 02h (see 4.2.2) from max attenuation to the control port volume setting on release of reset.

4.6.3 Soft Ramp-down before Reset (Bit 2)

Function:

This function allows the user to control if a soft ramp-down in volume is applied before a known reset condition. The modes are as follows:

0 - An instantaneous change is made from the control port volume setting to max attenuation when chip resets (default setting).
1 - Volume is ramped down using the soft-ramp settings in Bits 6:5 of register 02h (see 4.2.2) from the control port volume setting to max attenuation when chip resets.

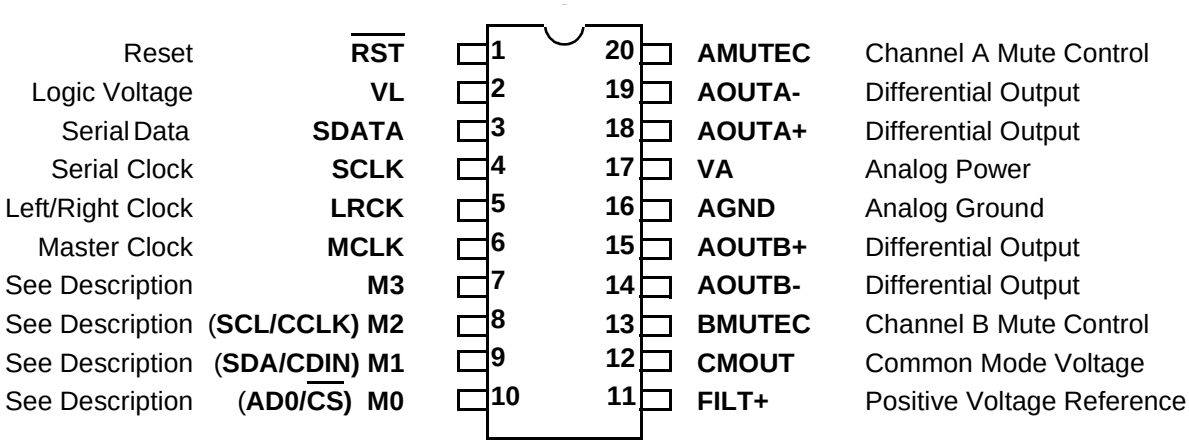
4.7 Chip ID - Register 07h

B7	B6	B5	B4	B3	B2	B1	B0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0

Function:

This register is Read-Only. Bits 7 through 4 are the part number ID which is 1000b (8h) and the remaining Bits (3 through 0) are for the chip revision.

5. PIN DESCRIPTION - PCM DATA MODE



RST	1	**Reset** (*Input*) - Hardware Mode: The device enters a low power mode and the internal state machine is reset to the default setting when low (0). When high (1), the device becomes operational. Control Port Mode: The device enters a low power mode and all internal registers are reset to the default settings, including the control port, when low. When high, the control port becomes operational and the PDN bit must be cleared before normal operation will occur. The control port can not be accessed when reset is low. The Control Port Enable Bit must also be enabled after a device reset. RST is required to remain low until the power supplies and clocks are applied and stable.
VL	2	**Interface Power** (*Input*) - Digital interface power supply. Typically 1.8 to 5.0 VDC. The voltage on this pin determines the logic level high threshold for the digital inputs. The voltage on VL is the maximum allowable input level for all digital inputs.
SDATA	3	**Serial Audio Data** (*Input*) - Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock.
SCLK	4	**Serial Clock** (*Input*) - Clocks the individual bits of the serial data into the SDATA pin.
LRCK	5	**Left / Right Clock** (*Input*) - The Left / Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference.

PCM Data Mode Pin Descriptions

MCLK	6	**Master Clock** (*Input*) - the master clock frequency must be either 256x, 384x, 512x, 768x or 1024x the input sample rate in Single Speed Mode; either 128x, 192x 256x, 384x or 512x the input sample rate in Double Speed Mode; or 64x, 96x 128x, 192x or 256 x the input sample rate in Quad Speed Mode. Table 8 illustrates the standard audio sample rates and the required master clock frequencies.

Mode (sample-rate range)	Sample Rate (kHz)	MCLK (MHz)				Control port only modes
MCLK Ratio		**256x**	**384x**	**512x**	**786x**	**1024x***
Single Speed (4 to 50 kHz)	32	8.1920	12.2880	16.3840	24.5760	32.7680
	44.1	11.2896	16.9344	22.5792	33.8688	45.1584
	48	12.2880	18.4320	24.5760	36.8640	49.1520
MCLK Ratio		**128x**	**192x**	**256x**	**384x**	**512x***
Double Speed (50 to 100 kHz)	64	8.1920	12.2880	16.3840	24.5760	32.7680
	88.2	11.2896	16.9344	22.5792	33.8688	45.1584
	96	12.2880	18.4320	24.5760	36.8640	49.1520
MCLK Ratio		**64x**	**96x**	**128x**	**192x**	**256x***
Quad Speed (100 to 200 kHz)	176.4	11.2896	16.9344	22.5792	33.8688	45.1584
	192	12.2880	18.4320	24.5760	36.8640	49.1520

Table 8. Common Clock Frequencies

14. *Note: these modes are only available in control port mode.

M3 (Control Port Mode)	7	Mode Select (*Inputs*) - The Mode Select Pin, M3, is not used in PCM Control Port mode and should be terminated to ground.
SDA/CDIN (Control Port Mode)	8	Serial Control Data I/O (*Input/Output*) - In Two-Wire mode, SDA is a data I/O line. CDIN is the input data line for the control port interface in SPI mode.
SCL/CCLK (Control Port Mode)	9	Serial Control Interface Clock (*Input*) - Clocks the serial control data into or from SDA/CDIN.
AD0 / $\overline{\text{CS}}$ (Control Port Mode)	10	Address Bit / Chip Select (*Input*) - In Two-Wire mode, AD0 is a chip address bit. $\overline{\text{CS}}$ is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain in SPI mode until either the part is reset or undergoes a power-down cycle.

PCM Data Mode Pin Descriptions

M3, M2, M1 and M0 (Stand-alone Mode)	7, 8, 9, and 10	Mode Select (*Inputs*) - The Mode Select Pins, M0-M3, select the operational mode of the device while in stand-alone mode.

M3	M1 (DIF1)	M0 (DIF0)	DESCRIPTION	FORMAT	FIGURE
0	0	0	Left Justified, up to 24-bit data	0	9
0	0	1	I^2S, up to 24-bit data	1	10
0	1	0	Right Justified, 16-bit Data	2	11
0	1	1	Right Justified, 24-bit Data	3	12

Table 9. Single Speed (4 to 50 kHz) Digital Interface Format, Stand-Alone Mode Options

M3	M2 (DEM)	DESCRIPTION	FIGURE
0	0	No De-Emphasis	7
0	1	De-Emphasis Enabled	7

Table 10. Single Speed Only (4 to 50 kHz) De-Emphasis, Stand-Alone Mode Options

M3	M2	M1	M0	DESCRIPTION	FORMAT	FIGURE
1	0	0	0	Left Justified up to 24-bit data	0	9
1	0	0	1	I^2S up to 24-bit data	1	10
1	0	1	0	Right Justified 16-bit data	2	11
1	0	1	1	Right Justified 24-bit data	3	12

Table 11. Double Speed (50 to 100 kHz) Digital Interface Format, Stand-Alone Mode Options

M3	M2	M1	M0	DESCRIPTION	FORMAT	FIGURE
1	1	0	0	Left Justified up to 24-bit data	0	9
1	1	0	1	I^2S up to 24-bit data	1	10
1	1	1	0	Right Justified 16-bit data	2	11
1	1	1	1	Right Justified 24-bit data	3	12

Table 12. Quad Speed (100 to 200 kHz) Digital Interface Format, Stand-Alone Mode Options

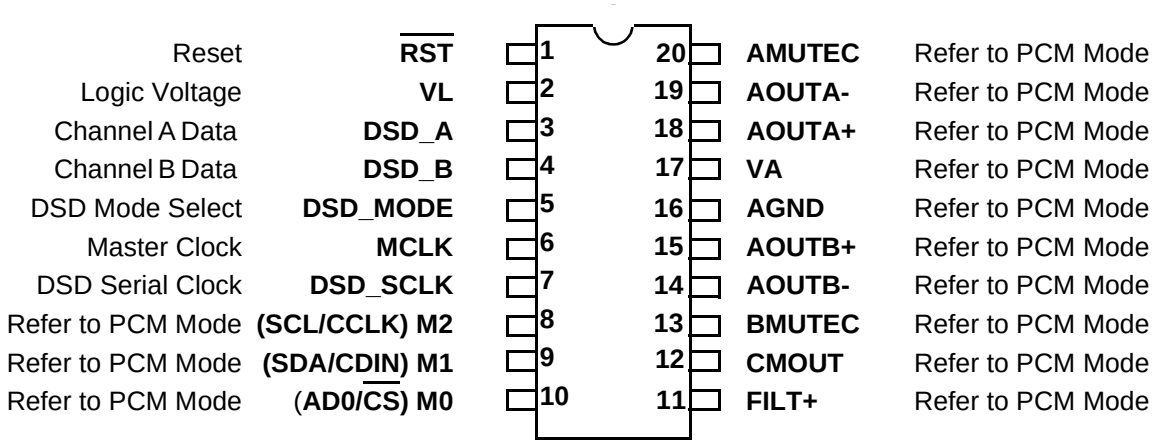
FILT+	11	Positive Voltage Reference (*Output*) - Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 5. The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.
CMOUT	12	Common Mode Voltage (*Output*) - Filter connection for internal common mode reference voltage, typically 50% of VA. Capacitors must be connected from CMOUT to analog ground, as shown in Figure 5. CMOUT is not intended to supply external current. CMOUT has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.

PCM Data Mode Pin Descriptions

AMUTEC and BMUTEC	13 and 20	Channel A and Channel B Mute Control (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down. These pins are intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.
AOUTB+, AOUTB- and AOUTA+, AOUTA	14, 15, 18, and 19	Differential Analog Audio Output (*Output*) - The fullscale differential output level is specified in the Analog Characteristics specification table.
AGND	16	Analog Ground (*Input*) Analog ground reference. Should be connected to analog ground.
VA	17	Analog Power (*Input*) - Analog power supply. Typically 5 VDC.

PCM Data Mode Pin Descriptions

6. PIN DESCRIPTION - DSD MODE



$\overline{\text{RST}}$	1	**Reset** (*Input*) - Hardware Mode: The device enters a low power mode and the internal state machine is reset to the default setting when low (0). When high (1), the device becomes operational. Control Port Mode: The device enters a low power mode and all internal registers are reset to the default settings, including the control port, when low. When high, the control port becomes operational and the PDN bit must be cleared before normal operation will occur. The control port can not be accessed when reset is low. The Control Port Enable Bit must also be enabled after a device reset. $\overline{\text{RST}}$ is required to remain low until the power supplies and clocks are applied and stable.
VL	2	**Interface Power** (*Input*) - Digital interface power supply. Typically 1.8 to 5.0 VDC. The voltage on this pin determines the logic level high threshold for the digital inputs. The voltage on VL is the maximum allowable input level for all digital inputs.
DSD_A and DSD_B	3 and 4	**DSD Audio Data** *(Inputs)* - Direct Stream Digital audio data is clocked into DSD_A and DSD_B via the DSD serial clock.
DSD_Mode	5	**DSD Mode** *(Input)* - This pin must be set to a logic '1' and M0-M2 must be properly set to access the DSD Mode in Stand-Alone Mode. Refer to Table 13.In Control Port Mode, this pin must be set to a logic '1' and the Control Registers must be properly set to access the DSD Mode. Refer to register descriptions in Section 4.
MCLK	6	**Master Clock** *(Input)* - The master clock frequency must be either 4x, 6x, 8x or 12x the DSD data rate for 64x oversampled DSD data or 2x, 3x, 4x or 6x the DSD data rate for 128x oversampled DSD data.
DSD_SCLK	7	**DSD Serial Clock** *(Input)* - Clocks the individual bits of the DSD audio data into the DSD_A and DSD_B pins.

DSD Mode Pin Descriptions

M2, M1 and M0 (Stand-alone Mode)	8, 9, and 10	Mode Select (*Inputs*) - The Mode Select Pins, M0-M2, select the operational mode of the device while in stand-alone mode.

DSD_Mode	M2	M1	M0	DESCRIPTION
1	0	0	0	64x oversampled DSD data with a 4x MCLK to DSD data rate
1	0	0	1	64x oversampled DSD data with a 6x MCLK to DSD data rate
1	0	1	0	64x oversampled DSD data with a 8x MCLK to DSD data rate
1	0	1	1	64x oversampled DSD data with a 12x MCLK to DSD data rate
1	1	0	0	128x oversampled DSD data with a 2x MCLK to DSD data rate
1	1	0	1	128x oversampled DSD data with a 3x MCLK to DSD data rate
1	1	1	0	128x oversampled DSD data with a 4x MCLK to DSD data rate
1	1	1	1	128x oversampled DSD data with a 6x MCLK to DSD data rate

Table 13. Direct Stream Digital (DSD), Stand-Alone Mode Options

SDA/CDIN (Control Port Mode)	8	Serial Control Data I/O (*Input/Output*) - In Two-Wire mode, SDA is a data I/O line. CDIN is the input data line for the control port interface in SPI mode.
SCL/CCLK (Control Port Mode)	9	Serial Control Interface Clock (*Input*) - Clocks the serial control data into or from SDA/CDIN.
AD0 / $\overline{\text{CS}}$ (Control Port Mode)	10	Address Bit / Chip Select (*Input*) - In Two-Wire mode, AD0 is a chip address bit. $\overline{\text{CS}}$ is used to enable the control port interface in SPI mode. The device will enter the SPI mode at anytime a high to low transition is detected on this pin. Once the device has entered the SPI mode, it will remain in SPI mode until either the part is reset or undergoes a power-down cycle.
FILT+	11	Positive Voltage Reference (*Output*) - Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 6. The recommended values will typically provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.
CMOUT	12	Common Mode Voltage (*Output*) - Filter connection for internal common mode reference voltage, typically 50% of VA. Capacitors must be connected from CMOUT to analog ground, as shown in Figure 6. CMOUT is not intended to supply external current. CMOUT has a typical source impedance of 250 kΩ and any current drawn from this pin will alter device performance.
AMUTEC and BMUTEC	13 and 20	Channel A and Channel B Mute Control (*Output*) - The Mute Control pins go high during power-up initialization, reset, muting, when master clock to left/right clock frequency ratio is incorrect, or power-down. These pins are intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.
AOUTB+, AOUTB- and AOUTA+, AOUTA	14, 15, 18, and 19	Differential Analog Audio Output (*Output*) - The fullscale differential output level is specified in the Analog Characteristics specification table.
AGND	16	Analog Ground (*Input*) Analog ground reference. Should be connected to analog ground.
VA	17	Analog Power (*Input*) - Analog power supply. Typically 5 VDC.

DSD Mode Pin Descriptions

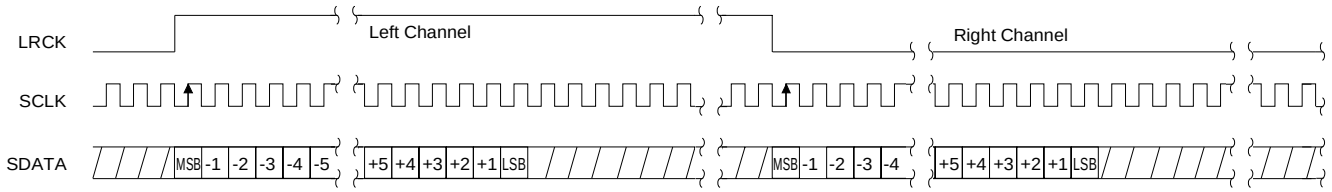


Figure 9. Format 0, Left Justified up to 24-Bit Data

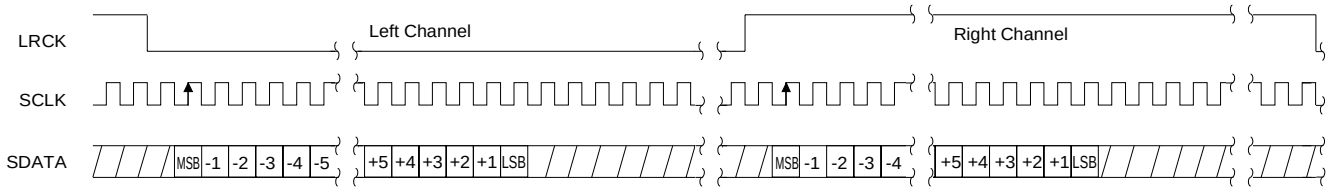


Figure 10. Format 1, I^2S up to 24-Bit Data

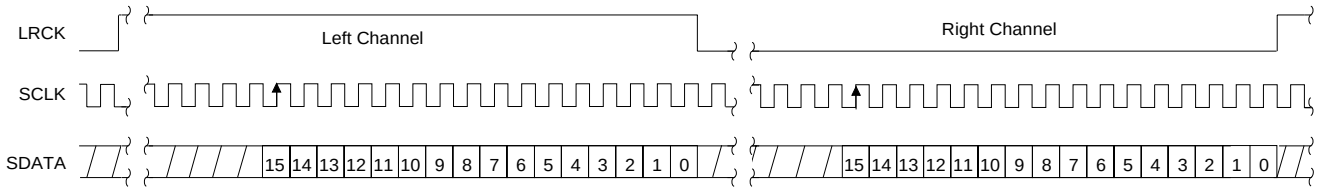


Figure 11. Format 2, Right Justified 16-Bit Data

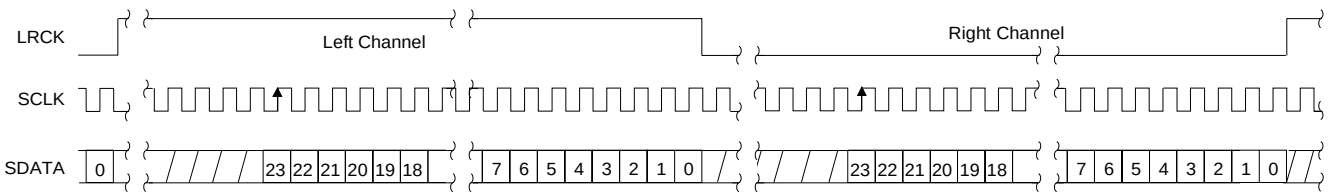


Figure 12. Format 3, Right Justified 24-Bit Data

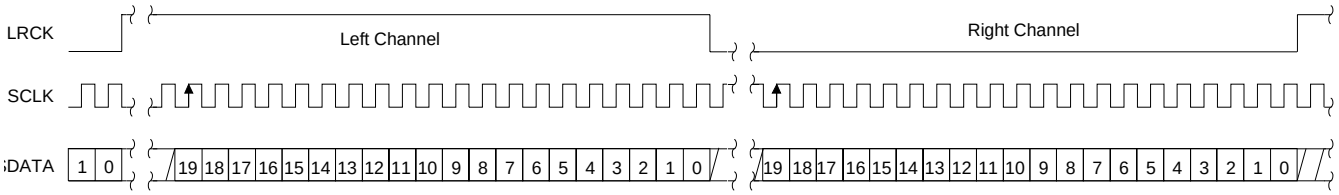


Figure 13. Format 4, Right Justified 20-Bit Data. (Available in Control Port Mode only)

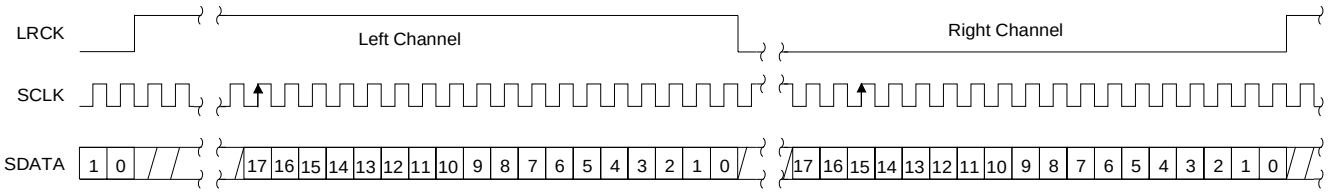


Figure 14. Format 5, Right Justified 18-Bit Data. (Available in Control Port Mode only)

7. APPLICATIONS

7.1 Recommended Power-up Sequence for Hardware Mode

1) Hold $\overline{\text{RST}}$ low until the power supplies, master, and left/right clocks are stable.
2) Bring $\overline{\text{RST}}$ high.

7.2 Recommended Power-up Sequence and Access to Control Port Mode

1) Hold $\overline{\text{RST}}$ low until the power supply, master, and left/right clocks are stable. In this state, the control port is reset to its default settings and CMOUT will remain low.
2) Bring $\overline{\text{RST}}$ high. The device will remain in a low power state with CMOUT low and the control port is accessible.
3) Write 30h to register 05h within 10 ms following the release of $\overline{\text{RST}}$.
4) The desired register settings can be loaded while keeping the PDN bit set to 1.
5) Set the PDN bit to 0 which will initiate the power-up sequence which requires approximately 10 µS.

7.3 Analog Output and Filtering

The application note “Design Notes for a 2-Pole Filter with Differential Input” discusses the second-order Butterworth filter and differential to single-ended converter which was implemented on the CS4392 evaluation board, CDB4392, as seen in Figure 15. The CS4392 filter is a linear phase design and does not include phase or amplitude compensation for an external filter. Therefore, the DAC system phase and amplitude response will be dependent on the external analog circuitry.

7.4 Interpolation Filter

To accommodate the increasingly complex requirements of digital audio systems, the CS4392 incorporates selectable interpolation filters for each mode of operation. A “fast” and a “slow” roll-off filter is available in each of Single, Double, and Quad Speed modes. These filters have been designed to accommodate a variety of musical tastes and styles. Bit 5 of the Mode Control 3 register (06h) is used to select which filter is used. When the part is used without the control port, the “fast” roll-off filter is selected.

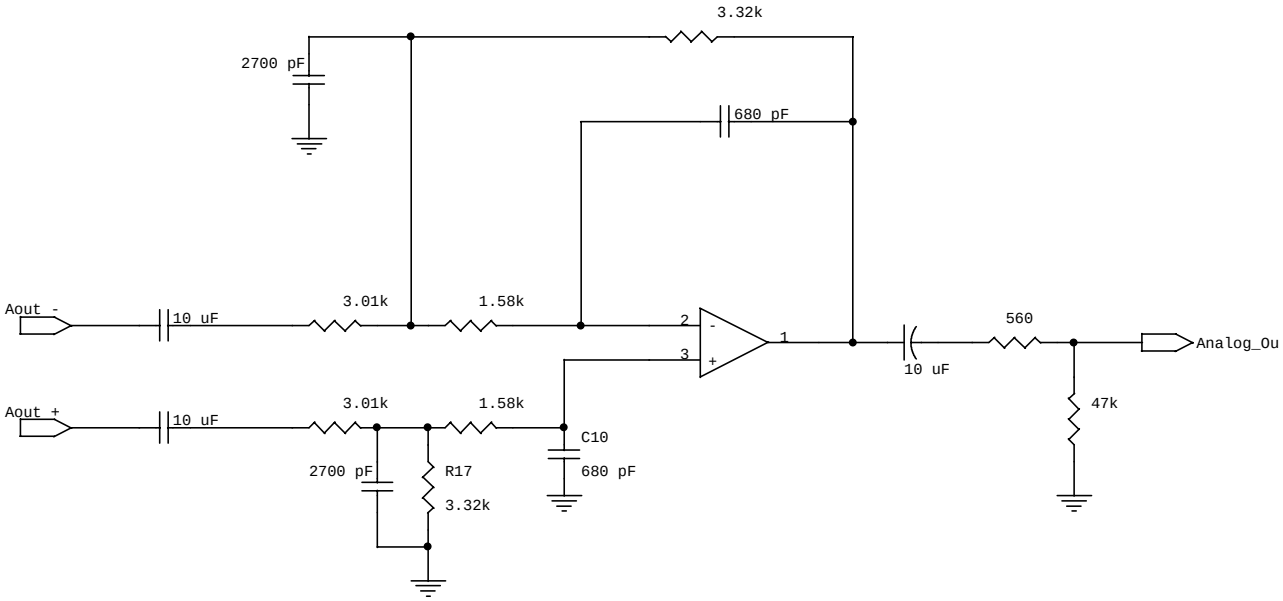


Figure 15. CS4392 Output Filter

8. CONTROL PORT INTERFACE

The control port is used to load all the internal settings of the CS4392. The operation of the control port may be completely asynchronous to the audio sample rate. However, to avoid potential interference problems, the control port pins should remain static if no operation is required.

The control port has 2 modes: SPI and Two-Wire, with the CS4392 operating as a slave device in both modes. If Two-Wire operation is desired, AD0/$\overline{CS}$ should be tied to VA or AGND. If the CS4392 ever detects a high to low transition on AD0/$\overline{CS}$ after power-up, SPI mode will be selected. The control port registers are write-only in SPI mode.

Upon release of the /RST pin, the CS4392 will wait approximately 100 ms before it begins its power-up sequence. The part defaults to Stand-Alone Mode, in which all operational modes are controlled as described in tables 9 through 12. The control port is active at all times, and if bit 5 of register 05h is set, the part enters Control-Port Mode and all operational modes are controlled by the control port registers. This bit can be set at any time, but to avoid unpredictable output noises, bit 5 and bit 4 of register 05h should be set before the end of the 100 ms power-up wait period. All registers can then be set as desired before releasing bit 4 of register 05h to begin the power-up sequence. If system requirements do not allow writing to the control port immediately following the release of /RST, the SDATA line should be held at logic "0" until the proper serial mode can be selected.

8.1 SPI Mode

In SPI mode, $\overline{CS}$ is the CS4392 chip select signal, CCLK is the control port bit clock, CDIN is the input data line from the microcontroller and the chip address is 0010000. All signals are inputs and data is clocked in on the rising edge of CCLK.

Figure 16 shows the operation of the control port in SPI mode. To write to a register, bring $\overline{CS}$ low. The first 7 bits on CDIN form the chip address, and must be 0010000. The eighth bit is a read/write indicator (R/$\overline{W}$), which must be low to write. The next 8 bits form the Memory Address Pointer (MAP), which is set to the address of the register that is to be updated. The next 8 bits are the data which will be placed into the register designated by the MAP. See Table 14 on page 34.

The CS4392 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

8.2 Two-Wire Mode

In Two-Wire mode, SDA is a bi-directional data line. Data is clocked into and out of the part by the clock, SCL, with the clock to data relationship as shown in Figure 3. There is no $\overline{CS}$ pin. Pin AD0 forms the partial chip address and should be tied to VA or AGND as required. The upper 6 bits of the 7-bit address field must be 001000. To communicate with the CS4392 the LSB of the chip address field, which is the first byte sent to the CS4392, should match the setting of the AD0 pin. The eighth bit of the address byte is the R/$\overline{W}$ bit (high for a read, low for a write). If the operation is a write, the next byte is the Memory Address Pointer, MAP, which selects the register to be read or written. The MAP is then followed by the data to be written. If the operation is a read, then the contents of the register pointed to by the MAP will be output after the chip address.

The CS4392 has MAP auto increment capability, enabled by the INCR bit in the MAP register. If INCR is 0, then the MAP will stay constant for successive writes. If INCR is set to 1, then MAP will auto increment after each byte is written, allowing block reads or writes of successive registers.

Two-Wire mode is compatible with I^2C. For more information on I^2C, please see "The I^2C-Bus Specification: Version 2.0", listed in the References section.

7	6	5	4	3	2	1	0
INCR	Reserved	Reserved	Reserved	Reserved	MAP2	MAP1	MAP0
0	0	0	0	0	0	0	0

INCR (Auto MAP Increment Enable)
Default = '0'.
0 - Disabled
1 - Enabled

MAP0-2 (Memory Address Pointer)
Default = '000'.

Table 14. Memory Address Pointer (MAP)

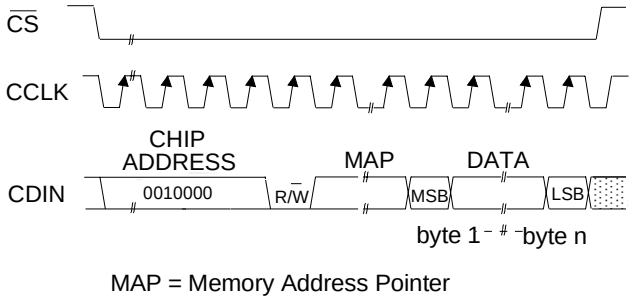
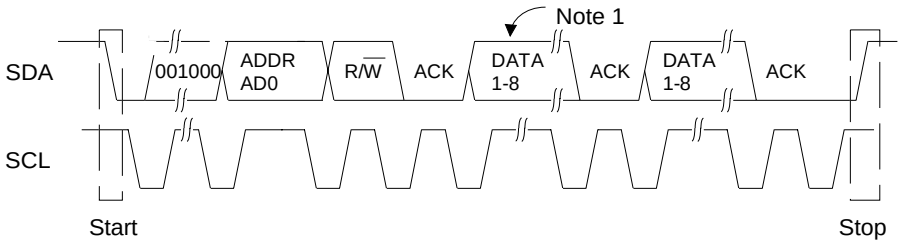


Figure 16. Control Port Timing, SPI mode



Note: If operation is a write, this byte contains the Memory Address Pointer, MAP.

Figure 17. Control Port Timing, Two-Wire Mode

9. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

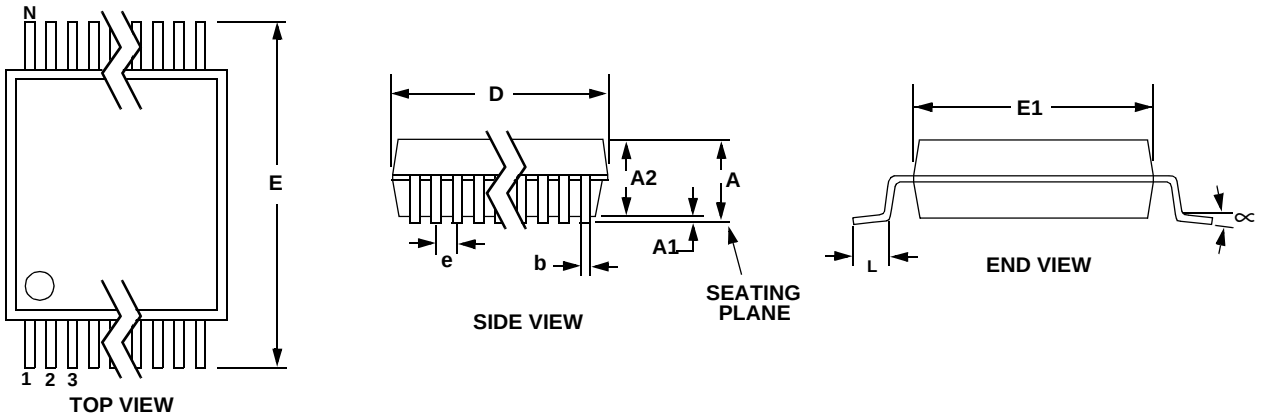
The change in gain value with temperature. Units in ppm/°C.

10. REFERENCES

1. "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.
2. CDB4392 Evaluation Board Datasheet
3. "The I^2C-Bus Specification: Version 2.0" Philips Semiconductors, December 1998. http://www.semiconductors.philips.com

11. PACKAGE DIMENSIONS

20L TSSOP (4.4 mm BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.043	--	--	1.10	
A1	0.002	0.004	0.006	0.05	--	0.15	
A2	0.03346	0.0354	0.037	0.85	0.90	0.95	
b	0.00748	0.0096	0.012	0.19	0.245	0.30	2,3
D	0.252	0.256	0.259	6.40	6.50	6.60	1
E	0.248	0.2519	0.256	6.30	6.40	6.50	
E1	0.169	0.1732	0.177	4.30	4.40	4.50	1
e	--	--	0.026	--	--	0.65	
L	0.020	0.024	0.028	0.50	0.60	0.70	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-153

Controlling Dimension is Millimeters.

Notes: 1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.

2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.

3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips

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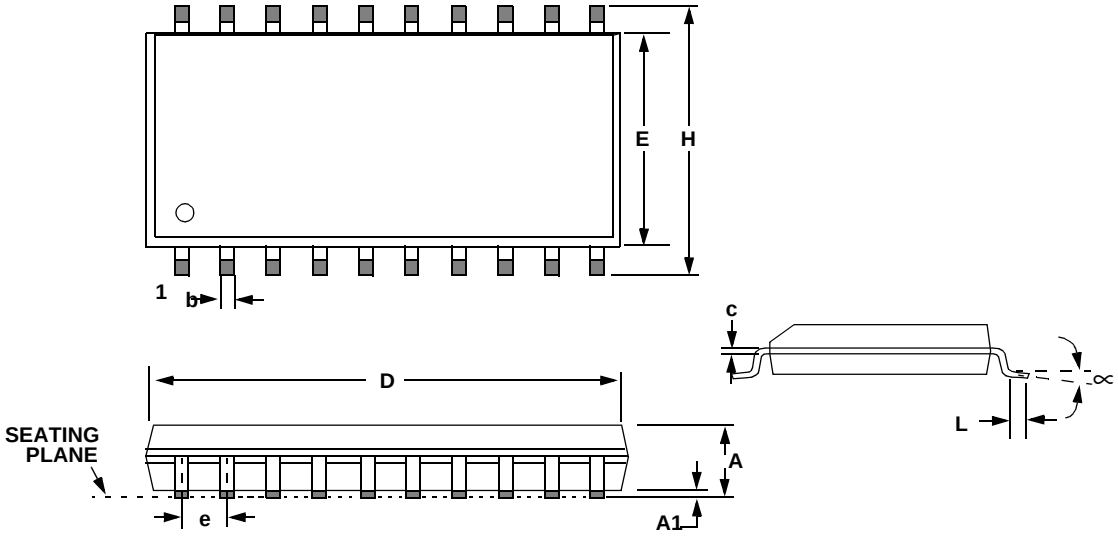
20L SOIC (300 MIL BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.093	0.098	0.104	2.35	2.50	2.65
A1	0.004	0.008	0.012	0.10	0.20	0.30
b	0.013	0.017	0.020	0.33	0.43	0.51
C	0.009	0.011	0.013	0.23	0.28	0.32
D	0.496	0.504	0.512	12.60	12.80	13.00
E	0.291	0.295	0.299	7.40	7.50	7.60
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.394	0.407	0.419	10.00	10.34	10.65
L	0.016	0.025	0.050	0.40	0.64	1.27
∝	0°	4°	8°	0°	4°	8°

JEDEC #: MS-013

Controlling Dimension is Millimeters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