CS5550

Two-channel, Low-cost A/D Converter

Features

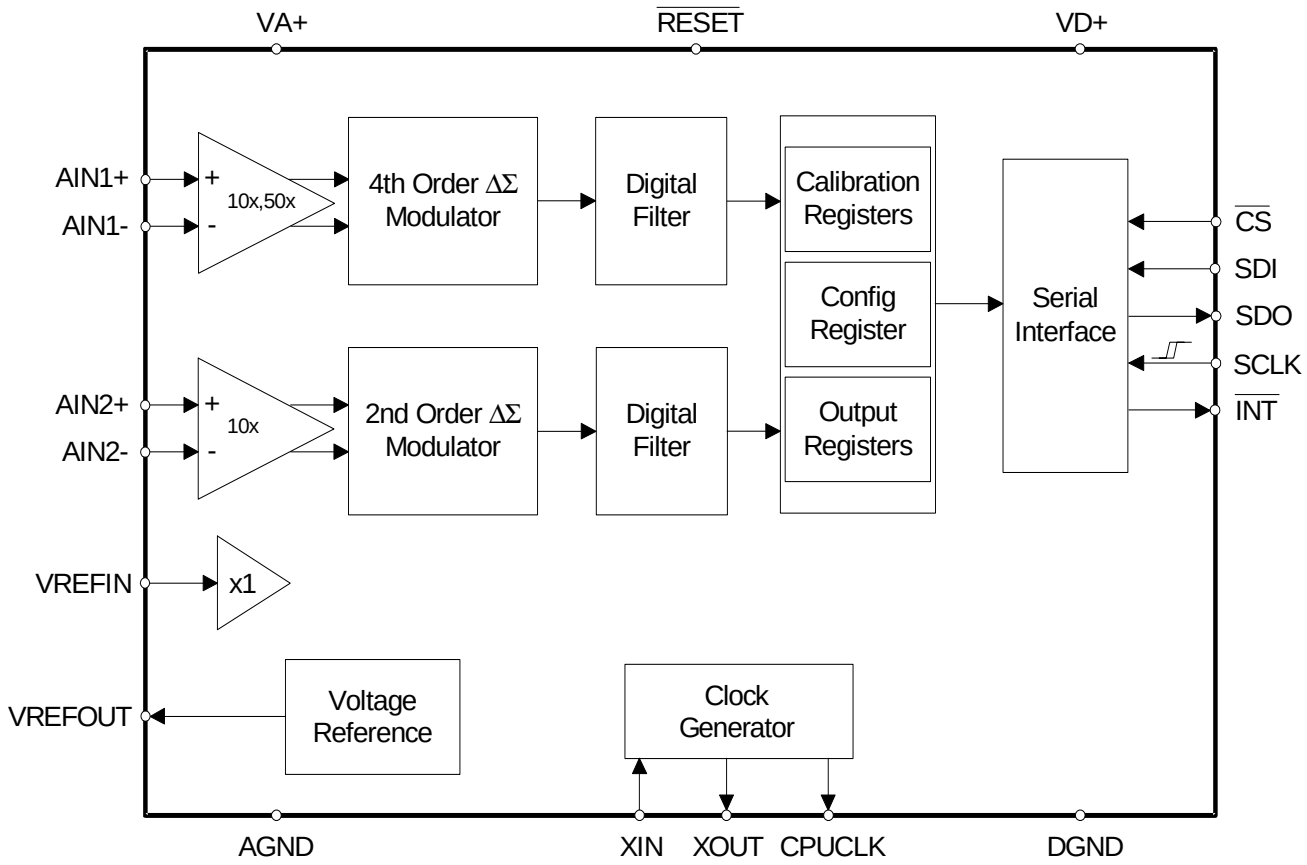
- Power Consumption <12 mW
  - with VD+ = 3.3 V
- Adjustable Input Range on AIN1±
- GND-referenced Signals with Single Supply
- On-chip 2.5 V Reference (25 ppm/°C typ)
- Simple Three-wire Digital Serial Interface
- Power Supply Configurations
  VA+ = +5 V; AGND = 0 V; VD+ = +3.3 V to +5 V

Description

The CS5550 combines two ΔΣ ADCs and a serial interface on a single chip. The CS5550 has on-chip functionality to facilitate offset and gain calibration. The CS5550 features a bi-directional serial interface for communication with a microcontroller.

ORDERING INFORMATION:

CS5550-IS	-40°C to +85°C	24-pin SSOP
CS5550-ISZ	-40°C to +85°C, Lead-free	24-pin SSOP



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Revision	Date	Changes
PP1	October 2003	Initial release
PP2	August 2004	Update THD on AIN1. Update Noise on AIN2. Update PSRR on AIN2. Delete AC Calibration references.
F1	March 2005	Added Lead-free Device Ordering Information

Contacting Cirrus Logic Support

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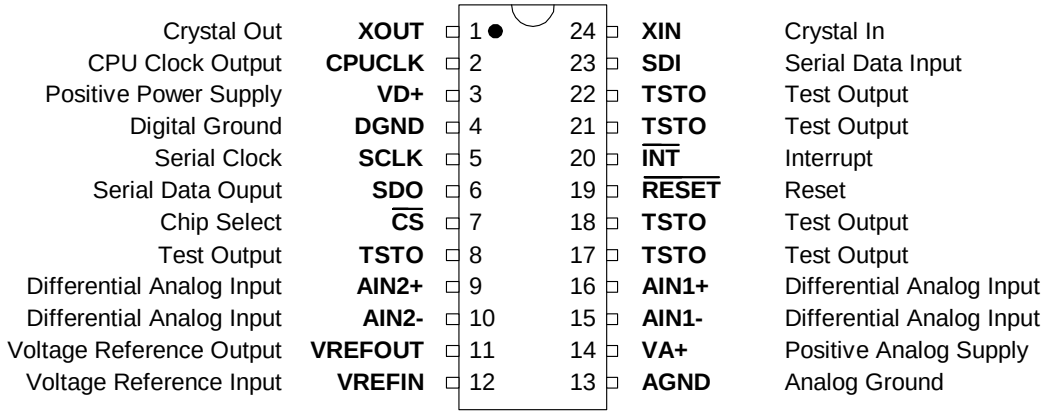
To find the one nearest to you go to **www.cirrus.com**

1. PIN DESCRIPTION



Clock Generator		
Crystal Out **Crystal In**	1,24	**XOUT, XIN** - A gate inside the chip is connected to these pins and can be used with a crystal to provide the system clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into XIN pin to provide the system clock for the device.
CPU Clock Output	2	**CPUCLK** - Output of on-chip oscillator which can drive one standard CMOS load.
Control Pins and Serial Data I/O		
Serial Clock Input	5	**SCLK** - A clock signal on this pin determines the input and output rate of the data for the SDI and SDO pins respectively. The SCLK pin will recognize clocks only when $\overline{CS}$ is low.
Serial Data Output	6	**SDO** -The serial data port output pin. Its output is in a high impedance state when $\overline{CS}$ is high.
Chip Select	7	**$\overline{CS}$** - When low, the port will recognize SCLK. An active high on this pin forces the SDO pin to a high impedance state. $\overline{CS}$ should be changed when SCLK is low.
Reset	19	**$\overline{RESET}$** - When reset is taken low, all internal registers are set to their default states.
Interrupt	20	**$\overline{INT}$** - When $\overline{INT}$ goes low it signals that an enabled event has occurred.
Serial Data Input	23	**SDI** - The serial data port input pin. Data will be input at a rate determined by SCLK.
Measurement and Reference Input		
Differential Analog Inputs	9,10,15,16	**AIN1+, AIN1-, AIN2+, AIN2-** - Differential analog input pins.
Voltage Reference Output	11	**VREFOUT** - The on-chip voltage reference output. The voltage reference has a nominal magnitude of 2.5 V and is referenced to the AGND pin on the converter.
Voltage Reference Input	12	**VREFIN** - The input establishes the voltage reference for the on-chip modulator.
Power Supply Connections		
Positive Digital Supply	3	**VD+** - The positive digital supply relative to DGND.
Digital Ground	4,9,10	**DGND** - The common-mode potential of digital ground must be equal to or above the common-mode potential of AGND.
Positive Analog Supply	14	**VA+** - The positive analog supply relative to AGND.
Analog Ground	13	**AGND** - The analog ground pin must be at the lowest potential.
Test Output	8,17,18,21,22	**TSTO** - These pins are used for factory testing and must be left floating.

2. CHARACTERISTICS/SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over all Operating Conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- DGND = 0 V. All voltages with respect to 0 V.

ANALOG CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Accuracy (Both Channels)						
Common Mode Rejection	(DC, 50, 60 Hz)	CMRR	80	-	-	dB
Offset Drift			-	5	-	nV/°C
Analog Inputs (AIN1±)						
Differential Input Voltage Range {(AIN1+) - (AIN1-)}	(Gain = 10) (Gain = 50)	AIN_1	0 0	- -	500 100	mV_{P-P} mV_{P-P}
Total Harmonic Distortion		THD_1	80	-	-	dB
Common Mode + Signal	Both Gain Ranges		-0.25	-	VA+	V
Crosstalk with AIN2± at Full Scale	(50, 60 Hz)		-	-	-115	dB
Input Capacitance	(Gain = 10) (Gain = 50)	IC_1	- -	25 25	- -	pF pF
Effective Input Impedance (Note 2)	(Gain = 10) (Gain = 50)	EII_1	30 30	- -	- -	kΩ kΩ
Noise (Referred to Input)	(Gain = 10) (Gain = 50)	N_1	- -	- -	22.5 4.5	μV_{rms} μV_{rms}
Accuracy						
Bipolar Offset Error	(Note 1)	VOS	-	-	±0.001	%F.S.
Full-Scale Error	(Note 1)	FSE	-	-	±0.001	%F.S.
Analog Inputs (AIN2±)						
Differential Input Voltage Range	{(AIN2+) - (AIN2-)}	AIN_2	0	-	500	mV_{P-P}
Total Harmonic Distortion		THD_2	65	-	-	dB
Common Mode + Signal			-0.25	-	VA+	V
Crosstalk with AIN1± at Full Scale	(50, 60 Hz)		-	-	-70	dB
Input Capacitance	(Gain = 10)	IC_2	-	0.2	-	pF
Effective Input Impedance (Note 2)	(Gain = 10)	EII_2	5	-	-	MΩ
Noise (Referred to Input)	(Gain = 10)	N_2	-	-	150	μV_{rms}
Accuracy						
Bipolar Offset Error	(Note 1)	VOS	-	-	±0.01	%F.S.
Full-Scale Error	(Note 1)	FSE	-	-	±0.01	%F.S.

Notes: 1. Applies after system calibration

2. Effective Input Impedance (EII) is determined by clock frequency (DCLK) and Input Capacitance (IC). EII = 1/(IC*DCLK/4). Note that DCLK = MCLK / K.

ANALOG CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Unit
Dynamic Characteristics						
High Rate Filter Output Word Rate		OWR	-	DCLK/1024	-	Hz
Input Sampling Rate	DCLK = MCLK/K		-	DCLK/8	-	Hz
Full Scale Calibration Range	(Note 3)	FSCR	25	-	100	%F.S.
High Pass Filter Pole Frequency	-3 dB		-	0.5	-	Hz
Power Supplies						
Power Supply Currents (Active State)	I_{A+}	PSCA	-	1.3	-	mA
	I_{D+} (VD+ = 5 V)	PSCD	-	2.9	-	mA
	I_{D+} (VD+ = 3.3 V)	PSCD	-	1.7	-	mA
Power Consumption (Note 4)	Active State (VD+ = 5 V)	PC	-	21	30	mW
	Active State (VD+ = 3.3 V)		-	11.6	-	mW
	Stand-by State		-	6.75	-	mW
	Sleep State		-	10	-	µW
Power Supply Rejection Ratio (AIN1±) (50, 60 Hz)(Note 5)	(Gain = 10)	$PSRR_1$	56	-	-	dB
	(Gain = 50)	$PSRR_1$	70	-	-	dB
Power Supply Rejection Ratio (AIN2±) (50, 60 Hz)(Note 5)	(Gain = 50)	$PSRR_2$	-	55	-	dB

Notes: 3. The minimum FSCR is limited by the maximum allowed gain register value.

4. All outputs unloaded. All inputs CMOS level.

5. Definition for PSRR: VREFIN tied to VREFOUT, VA+ = VD+ = 5 V, a 150 mV (zero-to-peak) (60 Hz) sinewave is imposed onto the +5 V DC supply voltage at VA+ and VD+ pins. The "+" and "-" input pins of both input channels are shorted to AGND. Then the CS5550 is commanded to continuous conversion acquisition mode, and digital output data is collected for the channel under test. The (zero-to-peak) value of the digital sinusoidal output signal is determined, and this value is converted into the (zero-to-peak) value of the sinusoidal voltage (measured in mV) that would need to be applied at the channel's inputs, in order to cause the same digital sinusoidal output. This voltage is then defined as V_{eq}. PSRR is then (in dB):

$$PSRR = 20 \cdot \log\left\{\frac{150}{V_{eq}}\right\}$$

VOLTAGE REFERENCE

Parameter		Symbol	Min	Typ	Max	Unit
Reference Output						
Output Voltage		REFOUT	2.4	-	2.6	V
Temperature Coefficient	(Note 6)	TC	-	25	60	ppm/°C
Load Regulation	(Output Current 1 µA Source or Sink)	ΔV_R	-	6	10	mV
Reference Input						
Input Voltage Range		VREFIN	2.4	2.5	2.6	V
Input Capacitance			-	4	-	pF
Input CVF Current			-	25	-	nA

Notes: 6. The voltage at VREFOUT is measured across the temperature range. From these measurements the following formula is used to calculate the VREFOUT Temperature Coefficient:.

$$TC_{VREF} = \left(\frac{(VREFOUT_{MAX} - VREFOUT_{MIN})}{VREFOUT_{AVG}}\right)\left(\frac{1}{T_{A}MAX - T_{A}MIN}\right)\left(1.0 \times 10^{6}\right)$$

5 V DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		-	-	0.8	V
XIN		-	-	1.5	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

3 V DIGITAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
High-Level Input Voltage	V_{IH}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		0.6 VD+	-	-	V
XIN		(VD+) - 0.5	-	-	V
SCLK and $\overline{\text{RESET}}$		0.8 VD+	-	-	V
Low-Level Input Voltage	V_{IL}				
All Pins Except XIN and SCLK and $\overline{\text{RESET}}$		-	-	0.48	V
XIN		-	-	0.3	V
SCLK and $\overline{\text{RESET}}$		-	-	0.2 VD+	V
High-Level Output Voltage I_{out} = +5 mA	V_{OH}	(VD+) - 1.0	-	-	V
Low-Level Output Voltage I_{out} = -5 mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	5	-	pF

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Positive Digital Power Supply	VD+	3.135	3.3	5.25	V
Positive Analog Power Supply	VA+	4.75	5	5.25	V
Negative Analog Power Supply	AGND	-0.25	0	0.25	V
Voltage Reference	VREF	-	2.5	-	V
Specified Temperature Range	T_A	-40	-	+85	°C

SWITCHING CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Gate Oscillator (Note 7)	MCLK	2.5	4.096	5	MHz
Master Clock Duty Cycle			40	-	60	%
CPUCLK Duty Cycle	(Note 8)		40		60	%
Rise Times	Any Digital Input Except SCLK	t_{rise}	-	-	1.0	µs
(Note 9)	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Fall Times	Any Digital Input Except SCLK	t_{fall}	-	-	1.0	µs
(Note 9)	SCLK		-	-	100	µs
	Any Digital Output		-	50	-	ns
Start-up						
Oscillator Start-Up Time	XTAL = 4.096 MHz (Note 10)	t_{ost}	-	60	-	ms
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2	MHz
Serial Clock	Pulse Width High	t_1	200	-	-	ns
	Pulse Width Low	t_2	200	-	-	ns
SDI Timing						
$\overline{CS}$ Falling to SCLK Rising		t_3	50	-	-	ns
Data Set-up Time Prior to SCLK Rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	100	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable		t_6	100	-	-	ns
SDO Timing						
$\overline{CS}$ Falling to SDI Driving		t_7	-	20	50	ns
SCLK Falling to New Data Bit (hold time)		t_8	-	20	50	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_9	-	20	50	ns

Notes:
7. Device parameters are specified with a 4.096 MHz clock. If a crystal is used, then XIN frequency must remain between 2.5 MHz - 5.0 MHz.
8. If external MCLK is used, then its duty cycle must be between 45% and 55% to maintain this spec.
9. Specified using 10% and 90% points on wave-form of interest. Output loaded with 50 pF.
10. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

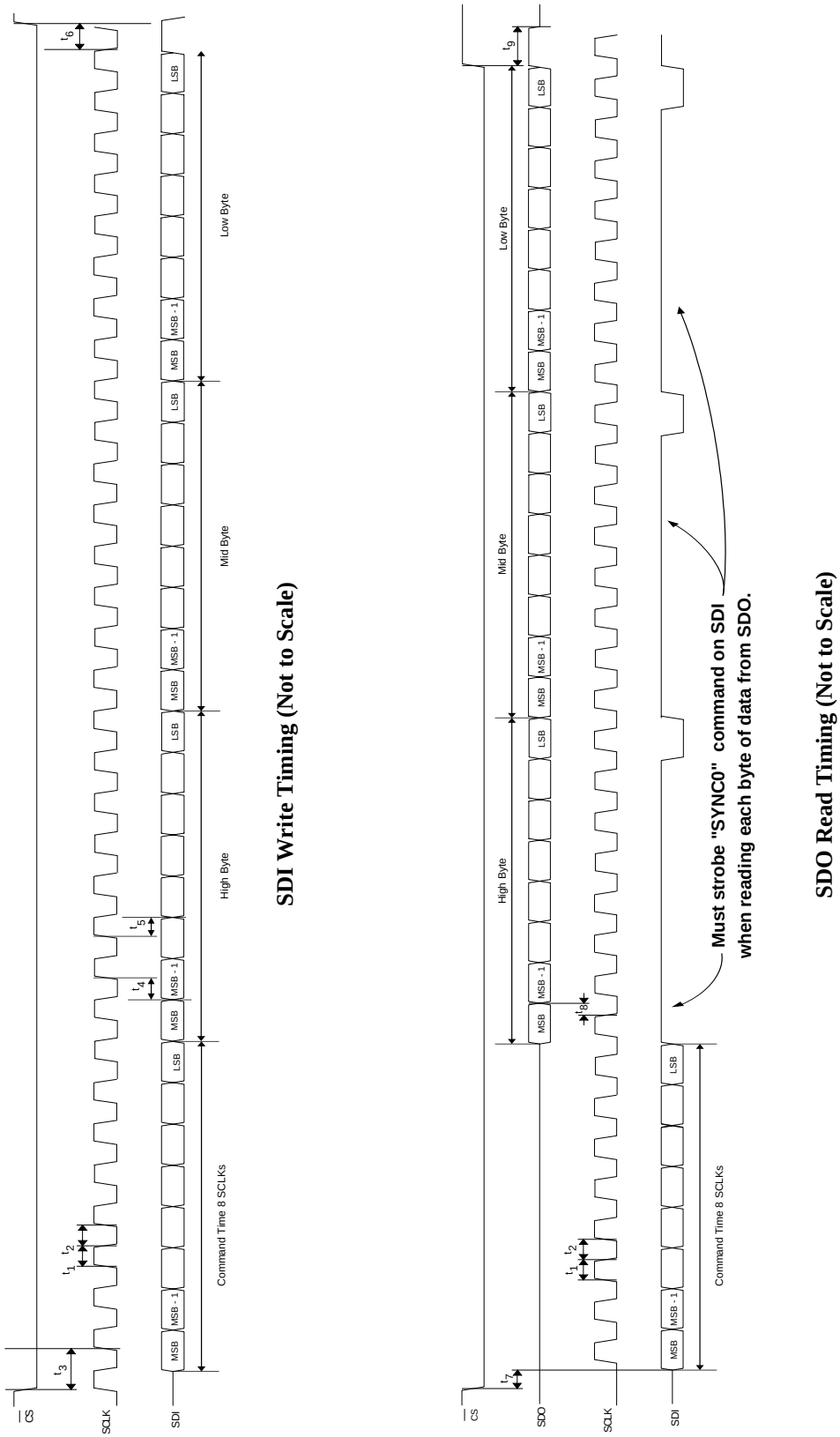


Figure 1. CS5550 Read and Write Timing Diagrams

2.1 Theory of Operation

The analog signals at the analog inputs are subject to the gains of the input PGAs. These signals are then sampled by the delta-sigma modulators at a rate of (MCLK/K) / 8.

2.1.1 High-Rate Digital Low-Pass Filters

The data is then low-pass filtered, to remove high-frequency noise from the modulator output. The high rate filters on both channels are implemented as fixed $Sinc^3$ filters.

2.1.2 Digital Compensation Filters

The data from both channels is then passed through two 4th-order IIR "compensation" filters, whose purpose is to correct (compensate) for the magnitude roll-off of the low-pass filtering operation. These filters "re-flatten" the magnitude response of the AIN1 and AIN2 channels over the relevant frequency range, by correcting for the magnitude roll-off effects that are induced by the $Sinc^3$ low-pass filter stages.

2.1.3 Gain and Offset Adjustment

After the filtering, the digital codes are subjected to value adjustments, based on the values in the DC Offset Registers (additive) and the Gain Registers (multiplicative). These registers are used for calibration of the device (see *Section 3.4, Calibration*). After offset and gain, the data is available to the user by reading the appropriate registers.

2.2 Performing Measurements

The CS5550 performs measurements at an output word rate (sampling rate) of (MCLK/K) / 1024. From these instantaneous samples, $FILT_1$ and $FILT_2$ are computed, using the most recent N instantaneous samples that were acquired. All of the measurements/results are available as a percentage of full scale. The *signed* output format is a two's complement format, and the output data words represent a normalized value between -1 and +1. The *unsigned* data in the CS5550 output registers represent normalized values between 0 and 1. A register value of 1 represents the maximum possible value. Note that a value of 1.0 is never actually obtained, the true maximum register value is [(2^23 - 1) / (2^23)] = 0.999999880791.

After each A/D conversion, the CRDY bit will be asserted in the Status Register, and the $\overline{INT}$ pin will also become active if the CRDY bit is unmasked (in the Mask Register). The assertion of the CRDY bit indicates that new instantaneous samples have been collected.

The unsigned $FILT_1$ and $FILT_2$ calculations are updated every N conversions (which is known as 1 "*computation cycle*") where N is the value in the Cycle Count Register. At the end of each computation cycle, the DRDY bit in the Mask Register will be set, and the $\overline{INT}$ pin will become active if the DRDY bit is unmasked.

DRDY is set only after each computation cycle has completed, whereas the CRDY bit is asserted after each individual A/D conversion. When these bits are asserted, they must be cleared before they can be asserted again. If the Cycle Count Register value (N) is set to 1, all output calculations are instantaneous, and DRDY will indicate when instantaneous calculations are finished, just like the CRDY bit. For the FILT results to be valid, the Cycle-Count Register must be set to a value greater than 10.

A computation cycle is derived from the master clock and its frequency is (MCLK/K)/(1024*N). Under default conditions with a 4.096 MHz clock at XIN, instantaneous A/D conversions are performed at a 4000 Hz rate, whereas FILT calculations are performed at a 1 Hz rate.

2.3 CS5550 Linearity Performance

	$FILT_1$	$FILT_2$
Range (% of FS)	0.2% - 100%	1% - 100%
Linearity	0.1% of reading	0.1% of reading

Table 2. Available range of ±0.1% output linearity, with default settings in the gain/offset registers.

Table 2 lists the range of input levels (as a percentage of full-scale registration in the FILT Registers) over which the output linearity of the FILT Register measurements are guaranteed to be within ±0.1%.

This linearity is guaranteed for all available full-scale input voltage ranges.

Note that until the CS5550 is calibrated (see Calibration) the *accuracy* of the CS5550 is not guaranteed to within ±0.1%. But the *linearity* of any given sample of CS5550, before calibration, will be within ±0.1% of reading over the ranges specified, with respect to the input voltage levels required to cause full-scale readings in the FILT Registers. Table 2 describes linearity + variation specs after the completion of each successive computation cycle.

3. FUNCTIONAL DESCRIPTION

3.1 Analog Inputs

The CS5550 has two available full-scale differential input voltage ranges for AIN1±.

The input ranges are the maximum sinusoidal signals that can be applied to the analog inputs, yet theses values will not result in full scale registration.

If the analog inputs are set to 500 mV_{P-P}, only a 250 mV_{RMS} signal will register full scale. Yet it would not be practical to inject a sinusoidal signal with a value of 250 mV_{RMS}. When such a sine wave enters the higher levels of its positive crest region (over each cycle), the voltage level of this signal exceeds the maximum differential input voltage range of the input channels. The largest sine wave voltage signal that can be placed across the inputs, with no saturation is:

$$\frac{500\text{mV}_{\text{P-P}}}{2\sqrt{2}} = \sim 176.78\text{mV}_{\text{RMS}}$$

which is ~70.7% of full-scale. So for sinusoidal inputs at the full scale peak-to-peak level the full scale registration is ~.707.

3.2 Voltage Reference

The CS5550 is specified for operation with a +2.5 V reference between the VREFIN and AGND pins. The converter includes an internal 2.5 V reference (25 ppm/°C drift) that can be used by connecting the VREFOUT pin to the VREFIN pin of the device. If higher accuracy/stability is required, an external reference can be used.

3.3 Oscillator Characteristics

XIN and XOUT are the input and output of an inverting amplifier to provide oscillation and can be configured as an on-chip oscillator, as shown in Figure 2. The oscillator circuit is designed to work with a quartz crystal or a ceramic resonator. To reduce circuit cost, two load capacitors C1 and C2 are integrated in the device. With these load capacitors, the oscillator circuit is capable of oscillation up to 20 MHz. To drive the device from an external clock source, XOUT should be left unconnected while XIN is driven by the external circuitry. There is an amplifier between XIN and the digital section which provides CMOS level signals. This amplifier works with sinusoidal inputs so there are no problems with slow edge times.

The CS5550 can be driven by an external oscillator ranging from 2.5 to 20 MHz, but the K divider value must be set such that the internal DCLK will run somewhere between 2.5 MHz and 5 MHz. The K divider value is set with the K[3:0] bits in the Configuration Register. As an example, if XIN = MCLK = 15 MHz, and K is set to 5, then DCLK is 3 MHz, which is a valid value for DCLK.

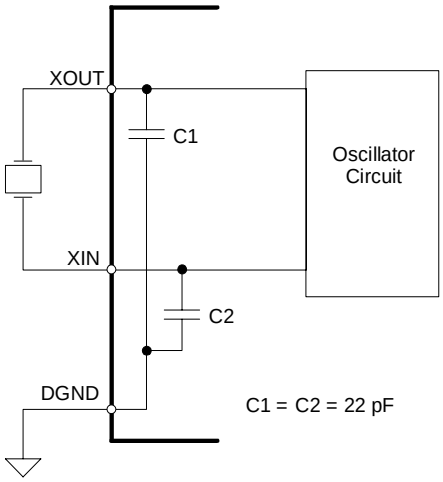


Figure 2. Oscillator Connection

3.4 Calibration

3.4.1 Overview of Calibration Process

The CS5550 offers digital calibration for offset and gain. Since both channels have separate offset and gain registers associated with them, system offset or system gain can be performed on either channel without the calibration results from one channel affecting the other.

3.4.2 Calibration Sequence

1. Before Calibration the CS5550 must be operating in its *active* state, and ready to accept valid commands. The 'DRDY' bit in the Status Register should also be cleared.

2. Apply appropriate calibration signals to the inputs of the AIN1 and AIN2 channels (discussed next in Sections 3.4.3 and 3.4.4.)

3. Send the 8-bit calibration command to the CS5550 serial interface. Various bits within this command specify the exact type of calibration. The calibration command should not be sent to the device while performing A/D conversions.

4. After the CS5550 finishes the desired internal calibration sequence, the DRDY bit is set in the Status Register to indicate that the calibration sequence is complete. The results of the calibration are now available in the appropriate gain/offset registers.

3.4.3 Calibration Signal Input Level

For gain calibrations, there is an absolute limit on the voltage levels that are selected for the gain calibration input signals. The maximum value that the gain register can attain is 4. Therefore, for either channel, if the voltage level of a gain calibration input signal is low enough that it causes the CS5550 to attempt to set either gain register higher than 4, the gain calibration result will be invalid and all CS5550 results obtained while performing A/D conversions will be invalid.

3.4.4 Input Configurations for Calibrations

Figure 3 shows the basic setup for gain calibration. When performing a gain calibration a *positive* DC voltage level must be applied at the inputs of the AIN1 and/or AIN2 channels. This voltage should be set to the level that represents the *absolute maximum* instantaneous voltage level that needs to be measured across the inputs (including the maximum over-range level that must be accurately measured).

For offset calibrations, the "+" and "-' pins of the AIN± channels should be connected to their ground reference level. (See Figure 4.)

Calibrating both offset and gain at the same time will cause undesirable calibration results.

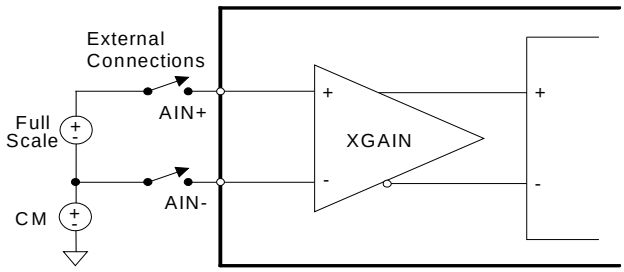


Figure 3. System Calibration of Gain.

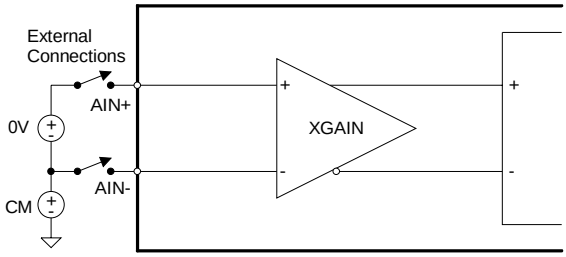


Figure 4. System Calibration of Offset.

3.4.5 Description of Calibration Algorithms

Note: For proper calibration, the value of the AIN1/AIN2 Gain Registers must be set to default (1.0) before running the *gain* calibration(s), and the value in the *Offset* Registers must be set to default (0) before running *offset* calibrations. This can be accomplished by a software or hardware reset of the device. The values in the calibration registers *do* affect the results of the calibration sequences.

3.4.5.1 Offset Calibration Sequence

The Offset Registers hold the negative of the simple average of N samples taken while the offset calibration was executed. The inputs should be grounded during offset calibration. The offset value

is added to the signal path to nullify the DC offset in the system.

3.4.5.2 Gain Calibration Sequence

Based on the level of the positive DC calibration voltage applied across the "+' and "-" inputs, the CS5550 determines the Gain Register value by averaging the Digital Output Register's output signal values over one computation cycle (N samples) and then dividing this average into 1. Therefore, after the gain calibration, the Instantaneous Register will read at full-scale whenever the DC level of the input signal is equal to the level of the calibration signal applied to the inputs during the gain calibration (see Figure 5).

3.4.6 Duration of Calibration Sequence

The value of the Cycle Count Register (N) determines the number of conversions performed by the CS5550 during a given calibration sequence. For offset/gain calibrations, the calibration sequence takes at least N + 30 conversion cycles to complete. As N is increased, the accuracy of calibration results will increase.

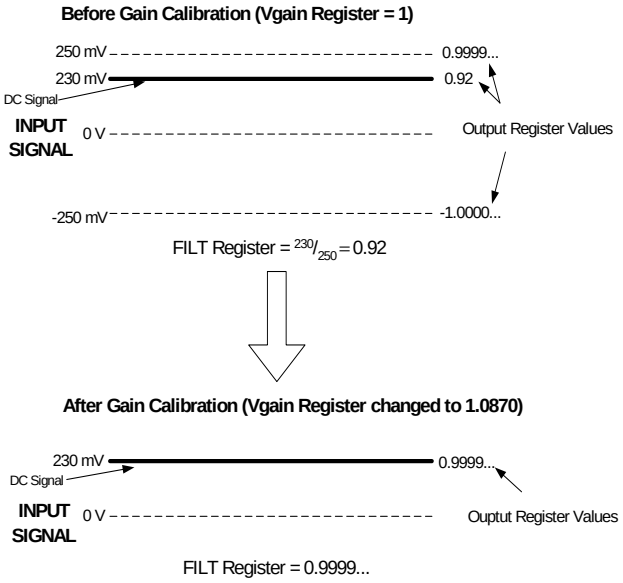


Figure 5. Example of Gain Calibration

3.5 Interrupt

The $\overline{\text{INT}}$ pin is used to indicate that an event has taken place in the converter that needs attention. These events inform the system about operation conditions and internal error conditions. The $\overline{\text{INT}}$ signal is created by combining the Status Register with the Mask Register. Whenever a bit in the Status Register becomes active, and the corresponding bit in the Mask Register is a logic 1, the $\overline{\text{INT}}$ signal becomes active. The interrupt condition is cleared when the bits of the Status Register are returned to their inactive state.

3.5.1 Typical use of the $\overline{\text{INT}}$ pin

The steps below show how interrupts can be handled.

- *Initialization*:

  Step I0 - All Status bits are cleared by writing FFFFFF (Hex) into the Status Register.

  Step I1 - The conditional bits which will be used to generate interrupts are then set to logic 1 in the Mask Register.

  Step I3 - Enable interrupts.

- *Interrupt Handler Routine*:

  Step H0 - Read the Status Register.

  Step H1 - Disable all interrupts.

  Step H2 - Branch to the proper interrupt service routine.

  Step H3 - Clear the Status Register by writing back the read value in step H0.

  Step H4 - Re-enable interrupts.

  Step H5 - Return from interrupt service routine.

  This handshaking procedure insures that any new interrupts activated between steps H0 and H3 are not lost (cleared) by step H3.

3.5.2 $\overline{\text{INT}}$ Active State

The behavior of the $\overline{\text{INT}}$ pin is controlled by the IMODE and IINV bits of the Configuration Register. The pin can be active low (default), active high, active on a return to logic 0 (pulse-low), or active on a return to logic 1 (pulse-high). If the interrupt output signal format is set for either pulse-high or

pulse-low, the duration of the $\overline{INT}$ pulse will be at least one DCLK cycle (DCLK = MCLK / K).

3.6 PCB Layout

The CS5550 should be placed entirely over an analog ground plane with both the AGND and DGND pins of the device connected to the analog plane. Place the analog-digital plane split immediately adjacent to the digital portion of the chip.

4. SERIAL PORT OVERVIEW

The CS5550's serial port incorporates a state machine with transmit/receive buffers. The state machine interprets 8-bit command words on the rising edge of SCLK. Upon decoding of the command word, the state machine performs the requested command or prepares for a data transfer of the addressed register. Request for a read requires an internal register transfer to the transmit buffer, while a write waits until the completion of 24 SCLKs before performing a transfer. The internal registers are used to control the ADC's functions. All registers are 24-bits in length.

The CS5550 is initialized and fully operational in its *active* state upon power-on. After a power-on, the device will wait to receive a valid command (the first 8-bits clocked into the serial port). Upon receiving and decoding a valid command word, the state machine instructs the converter to either perform a system operation, or transfer data to or from an internal register. The user should refer to the “Commands” section to decode all valid commands.

4.1 Commands

All command words are 1 byte in length. Any 8-bit word that is not listed in this section should be considered an illegal command word, and issuing any such illegal command word to the serial interface can result in unpredictable operation of the CS5550. Commands that write to a register must be followed by 3 bytes of register data. Commands that read data can be chained with other commands (e.g., while reading data, a new command can be sent to SDI which can execute before the original read is completed). This allows for “chaining” commands.

4.1.1 Start Conversions

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	C	0	0	0

This command indicates to the state machine to begin acquiring measurements and calculating results. The device has two modes of acquisition.

C = Modes of acquisition/measurement
0 = Perform a single computation cycle
1 = Perform continuous computation cycles

4.1.2 SYNC0 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	0

This command is the end of the serial port re-initialization sequence. The command can also be used as a NOP command. The serial port is resynchronized to byte boundaries by sending three or more consecutive SYNC1 commands followed by a SYNC0 command.

4.1.3 SYNC1 Command

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	1	1	1	1	1

This command is part of the serial port re-initialization sequence. The command also serves as a NOP command.

4.1.4 Power-Up/Halt

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	0	0	0	0

If the device is powered-down, this command will power-up the device. When powered-on, no computations will be running. If the part is already powered-on, all computations will be halted.

4.1.5 Power-Down and Software Reset

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	S1	S0	0	0	0

The device has two power-down states to conserve power. If the chip is put in stand-by state, all circuitry except the analog/digital clock generators is turned off. In the sleep state, all circuitry except the digital clock generator and the instruction decoder is turned off. Waking up the CS5550 out of sleep state requires more time than out of stand-by state, because of the extra time needed to re-start and re-stabilize the analog clock signal.

S1,S0 — Power-down state
00 = Software Reset
01 = Halt and enter stand-by power saving state. This state allows quick power-on time
10 = Halt and enter sleep power saving state. This state requires a slow power-on time
11 = Reserved

4.1.6 Calibration

B7	B6	B5	B4	B3	B2	B1	B0
1	1	0	A2	A1	0	G	O

The device has the capability of performing a system offset calibration and gain calibration. Offset and gain calibrations should NOT be performed at the same time (must do one after the other). Proper inputs must be supplied to the device before initiating calibration.

A2,A1 — Designates calibration channel
00 = Not allowed
01 = Calibrate the AIN1 channel
10 = Calibrate the AIN2 channel
11 = Calibrate AIN1 channel and AIN2 channel simultaneously

G — Designates gain calibration
0 = Normal operation
1 = Perform gain calibration

O — Designates offset calibration
0 = Normal operation
1 = Perform offset calibration

4.1.7 Register Read/Write

B7	B6	B5	B4	B3	B2	B1	B0
0	W/$\overline{R}$	RA4	RA3	RA2	RA1	RA0	0

The Read/Write command informs the state machine that a register access is required. During a *read* operation, the addressed register is loaded into the device's output buffer and clocked out by SCLK. During a *write* operation, the data is clocked into the input buffer and, and all 24 bits are transferred to the addressed register on the 24th SCLK.

W/$\overline{R}$ Write/Read control
0 = Read register
1 = Write register

RA[4:0] Register address bits (bits 1 through 5) of the read/write command.

Address	RA[4-0]	Abbreviation	Name/Description
0	00000	Config	Configuration Register
1	00001	$AIN1_{DCoff}$	AIN1 Offset Register
2	00010	$AIN1_{gn}$	AIN1 Gain Register
3	00011	$AIN2_{DCoff}$	AIN2 Offset Register
2	00100	$AIN2_{gn}$	AIN2 Gain Register
5	00101	Cycle Count	Number of A/D conversions used in one computation cycle (N)).
6	00110	Res	Reserved †
7	00111	OUT_1	AIN1 Output Register
8	01000	OUT_2	AIN2 Output Register
9	01001	Res	Reserved †
10	01010	Res	Reserved †
11	01011	$FILT_1$	Computed Filtered value for AIN1
12	01100	$FILT_2$	Computed Filtered value for AIN2
13	01101	Res	Reserved †
14	01110	Res	Reserved †
15	01111	Status	Status Register
16	10000	Res	Reserved
17	10001	Res	Reserved
18	10010	Res	Reserved †
19	10011	Res	Reserved
20	10100	Res	Reserved †
21	10101	Res	Reserved †
22	10110	Res	Reserved †
23	10111	Res	Reserved †
24	11000	Res	Reserved †
25	11001	Res	Reserved †
26	11010	Mask	Mask Register
27	11011	Res	Reserved †
28	11100	Ctrl	Control Register
29	11101	Res	Reserved †
30	11110	Res	Reserved †
31	11111	Res	Reserved †

† These registers are for internal use only. For proper device operation, the user must *not* attempt to write to these registers.

4.2 Serial Port Interface

The CS5550's serial interface consists of four control lines, which have the following pin-names: $\overline{CS}$, SDI, SDO, and SCLK.

$\overline{CS}$, Chip Select, is the control line which enables access to the serial port. If the $\overline{CS}$ pin is tied to logic 0, the port can function as a three wire interface. SDI, Serial Data In, is the data signal used to transfer data to the converters.

SDO, Serial Data Out, is the data signal used to transfer output data from the converters. The SDO output will be held at high impedance any time $\overline{CS}$ is at logic 1.

SCLK, Serial Clock, is the serial bit-clock which controls the shifting of data to or from the ADC's serial port. The $\overline{CS}$ pin must be held at logic 0 before SCLK transitions can be recognized by the port logic. To accommodate opto-isolators SCLK is designed with a Schmitt-trigger input to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 400 mV loss in the drive voltage when sinking or sourcing 5 mA.

4.3 Serial Read and Write

The state machine decodes the command word as it is received. Data is written to and read from the CS5550 by using the Register Read/Write command. Figure 1 illustrates the serial sequence necessary to write to, or read from the serial port's buffers. As shown in Figure 1, a transfer of data is always initiated by sending the appropriate 8-bit command (MSB first) to the serial port (SDI pin).

4.3.1 Register Write

When a command involves a write operation, the serial port will continue to clock in the data bits (MSB first) on the SDI pin for the next 24 SCLK cycles. Command words instructing a register write must be followed by 24 bits of data. To write the Configuration Register, the user would transmit the command (0x40) to initiate a write to the Configuration Register. The CS5550 will then acquire the serial data input from the (SDI) pin when the user pulses the serial clock (SCLK) 24 times. Once the data is received, the state machine writes the data to the Configuration Register and then waits to receive another valid command.

4.3.2 Register Read

When a read command is initiated, the serial port will start transferring register content bits serial (MSB first) on the SDO pin for the next 8, 16, or 24 SCLK cycles. Command words instructing a register read may be terminated at 8-bit boundaries (e.g., read transfers may be 8, 16, or 24 bits in length). Also data register reads allow "command chaining". This means that the micro-controller is allowed to send a new command while reading register data. The new command will be acted upon immediately and could possibly terminate the first register read. For example, if the user is only interested in acquiring the 16 most significant bits of data from the first read, then the user can begin to strobe a second read command on SDI after the first 8 data bits have been read from SDO.

During the read cycle, the SYNC0 command (NOP) should be strobed on the SDI port while clocking the data from the SDO port.

4.4 System Initialization

A software or hardware reset can be initiated at any time. The software reset is initiated by sending the command 0x80.

A hardware reset is initiated when the $\overline{RESET}$ pin is forced low with a minimum pulse width of 50 ns. The $\overline{RESET}$ signal is asynchronous, requiring no MCLKs for the part to detect and store a reset event. The $\overline{RESET}$ pin is a Schmitt Trigger input, which allows it to accept slow rise times and/or noisy control signals. Once the $\overline{RESET}$ pin is inactive, the internal reset circuitry remains active for 5 MCLK cycles to insure resetting the synchronous circuitry in the device. The modulators are held in reset for 12 MCLK cycles after $\overline{RESET}$ becomes inactive. After a hardware or software reset, the internal registers (some of which drive output pins) will be reset to their *default* values on the first MCLK received after detecting a reset event. The internal register values are also set to their default values after initial power-on of the device. The CS5550 will then assume its *active* state. (The term *active state*,

as well as the other defined power states of the CS5550, are described in Section 4.6).

Refer to Section 5 of the data sheet to see the default register values for any particular device register.

4.5 Serial Port Initialization

It is possible for the serial interface to become unsynchronized, with respect to the SCLK input. If this occurs, any attempt to clock valid CS5550 commands into the serial interface will result in either no operation or unexpected operation, because the CS5550 will not interpret the input command bits correctly. The CS5550's serial port must then be re-initialized. To initialize the serial port, any of the following actions can be performed:

1) Drive (assert) the $\overline{CS}$ pin low [or if $\overline{CS}$ pin is already low, drive the pin high, then back to low].
2) Hardware Reset (drive $\overline{RESET}$ pin low, for at least 10 µs, then drive back to high).
3) Issue the *Serial Port Initialization Sequence*, which is performed by clocking 3 (or more) SYNC1 command bytes (0xFF) followed by one SYNC0 command byte (0xFE).

4.6 CS5550 Power States

Active state denotes the operation of CS5550 when the device is fully powered on (not in *sleep* state or *stand-by* state). Performing either of the following actions will insure that the CS5550 is operating in the *active* state:

1) Power on the CS5550. (Or if the device is already powered on, recycle the power.)
2) Software Reset
3) Hardware Reset

In addition to the actions listed above, note that if the device is in *sleep* state or in *stand-by* state, the action of waking up the device out of *sleep* state or *stand-by* state (by issuing the Power-Up/Halt command) will also insure that the device is set into *active* state. In order to send the Power-Up/Halt command to the device, the serial port must be initialized. Therefore, after applying power to the CS5550, a hardware reset should always be performed.

5. REGISTER DESCRIPTION

1. “Default**” => bit status after power-on or reset
2. Any bit not labeled is Reserved. A zero should always be used when writing to one of these bits.

5.1 Configuration Register

Address: 0

23	22	21	20	19	18	17	16
							gain
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
			IMODE	IINV			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	2HPF	1HPF	iCPU	K3	K2	K1	K0

Default** = 0x000001

gain — Sets the gain of the AIN1 PGA
0 = gain is 10
1 = gain is 50

[IMODE IINV] — Soft interrupt configuration bits. Select the desired pin behavior for indication of an interrupt.
00 = active low level (default)
01 = active high level
10 = falling edge (INT is normally high)
11 = rising edge (INT is normally low)

1HPF — Control the use of the High Pass Filter on AIN1 Channel.
0 = HPF disabled
1 = HPF enabled

2HPF — Control the use of the High Pass Filter on AIN2 Channel.
0 = HPF disabled
1 = HPF enabled

iCPU — Inverts the CPUCLK clock. In order to reduce the level of noise present when analog signals are sampled, the logic driven by CPUCLK should not be active during the sample edge.
0 = normal operation (default)
1 = minimize noise when CPUCLK is driving rising edge logic

K[3:0] — Clock divider. A 4-bit binary number used to divide the value of MCLK to generate the internal clock DCLK. The internal clock frequency is DCLK = MCLK/K. The value of K can range between 1 and 16. Note that a value of “0000” will set K to 16 (not zero).

5.2 Offset Registers

Address: 1 (Offset Register - AIN1)
3 (Offset Register - AIN2)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

Default** = 0.000

The Offset Registers are initialized to zero on reset, allowing the device to function and perform measurements. The register is loaded after one computation cycle with the offset when the proper input is applied and the Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range ± full scale. The numeric format of this register is two's complement notation.

5.3 Gain Registers

Address: 2 (Gain Register - AIN1)
4 (Gain Register - AIN2)

MSB															LSB
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	.....	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}

Default** = 1.000

The Gain registers are initialized to 1.0 on reset, allowing the device to function and perform measurements. The Gain registers hold the result of the gain calibrations. If a calibration is performed, the register is loaded after one computation cycle with the system gain when the proper DC input is applied and the Calibration Command is received. DRDY will be asserted at the end of the calibration. The register may be read and stored so the register may be restored with the desired system offset compensation. The value is in the range $0.0 \leq \text{Gain} < 3.9999$.

5.4 Cycle Count Register

Address: 5

MSB															LSB
2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	.....	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Default** = 4000

The Cycle Count Register value (denoted as 'N') determines the length of one *computation cycle*. During continuous conversions, the computation cycle frequency is (MCLK/K)/(1024∗N) where MCLK is master clock input frequency (into XIN/XOUT pins), K is clock divider value (as specified in the Configuration Register), and N is Cycle Count Register Value.

5.5 OUT_1 and OUT_2 Output Registers

Address: *7* (*AIN1 Output Register*)
8 (AIN2 Output Register)

MSB															LSB
$-(2^0)$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	.....	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

These signed registers contain the last value of the measured results of AIN1 and AIN2. The results will be within the range of $-1.0 \le AIN1,AIN2 < 1.0$. The value is represented in two's complement notation, with the binary point place to the right of the MSB (MSB has a negative weighting). These values are 22 bits in length. The two least significant bits, (located at the far right-side) have no meaning, and will always have a value of "0".

5.6 $FILT_1$, $FILT_2$ Unsigned Output Register

Address: *11* (*AIN1 Filtered Output Register*)
12 (AIN2 Filtered Output Register)

MSB															LSB
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	.....	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}

These unsigned registers contain the last values of $FILT_1$ and $FILT_2$. The results are in the range of $0.0 \le FILT_1,FILT_2 < 1.0$. The value is represented in (unsigned) binary notation, with the binary point place to the left of the MSB. These results are updated after each computation cycle.

5.7 Status Register and Mask Register

Address: *15* (*Status [Clear] Register*)
Address: *26 (Mask Register)*

23	22	21	20	19	18	17	16
DRDY			CRDY			OR1	OR2
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
	FOR1	FOR2					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			OD2	OD1			$\overline{IC}$

Default** = 0x000000 (Status [Clear] Register

0x000000 (Mask Register)

The Status [Clear] Register indicates the condition of the chip. In normal operation writing a '1' to a bit will cause the bit to go to the '0' state. Writing a '0' to a bit will maintain the status bit in its current state. With this feature the user can simply write back to the Status [Clear] Register to clear the bits that have been seen, without concern of clearing any newly set bits. Even if a status bit is masked to prevent the interrupt (at the time that the status bit is asserted), the status bit will still be set in (both of) the Status Registers so the user can poll the status.

The Mask Register is used to control the activation of the $\overline{INT}$ pin. Placing a logic '1' in the Mask Register will allow the corresponding bit in the Status Register to activate the $\overline{INT}$ pin when the status bit becomes active.

DRDY — Data Ready. When running in single or continuous conversion acquisition mode, this bit will indicate the end of computation cycles. When running calibrations, this bit indicates that the calibration sequence has completed, and the results have been stored in the offset or gain

OR1, OR2 — AIN Output Out of Range. Set when the *magnitude* of the calibrated output is too large or too

small to fit in the AIN Output Register.

CRDY — Conversion Ready. Indicates a new conversion is ready.

OD1, OD2 — Modulator oscillation detect. Set when the modulator oscillates due to an input above Full Scale. Note that the level at which the modulator oscillates is significantly higher than the Input Voltage Range.

FOR1, FOR2 — FILT out of range. Set when the calibrated voltage value is too large for the FILT register.

$\overline{IC}$ — Invalid Command. Normally logic 1. Set to logic 0 if the host interface is strobed with an 8-bit word that is not recognized as one of the valid commands (see Section 4.1, *Commands*).

5.8 Control Register

Register Address: 28

23	22	21	20	19	18	17	16
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
			INTOD		NOCPU	NOOSC	

Default** = 0x000000

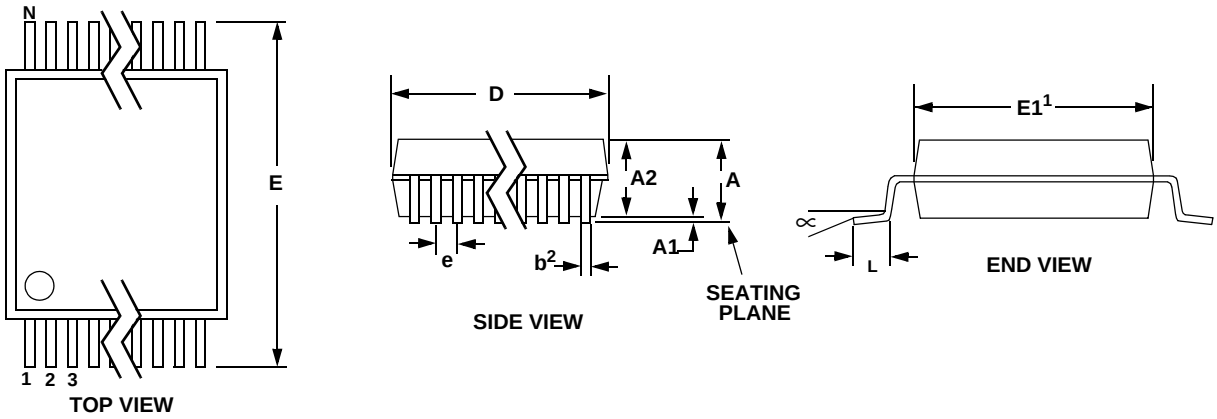
INTOD — 1 = Converts $\overline{INT}$ output to open drain configuration.

NOCPU — 1 = saves power by disabling the CPUCLK external drive pin.

NOOSC — 1 = saves power by disabling the crystal oscillator circuit.

6. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:
1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.