Description and Overview

Universality

CMI9739 is a 6CH AC97 CODEC, applicable for major MB chipsets of Intel, VIA, Ali, and SIS. CMI9739 is ideal for PC2001-compliant desktops, notebooks, and home entertainment PCs where high-quality audio is a must.

6CH Playback

The specially-designed 6CH hardware architecture of CMI9739 allows multi-channel south bridge to playback 6CH audio.

Cost-effectiveness

As to the cost concern, CMI9739 integrates the earphone buffer, analog CD differential interface, and analog switch for rear channel audio to Line-in. Besides, Mic-in can share same jack with center/bass output for traditional 3 jacks audio port to output 6 channels audio. CMI9739 also has built-in PLL to save additional crystal.

More Audio Option

Last but not least, CMI9739 provides HRTF 3D audio which interface compatible with EAX™/ A3D™/DirectSound3D™. In addition, it provides Sensaura™ 3D audio option. In that regard, the audio quality of CMI9739 is fabulous beyond general expectation.

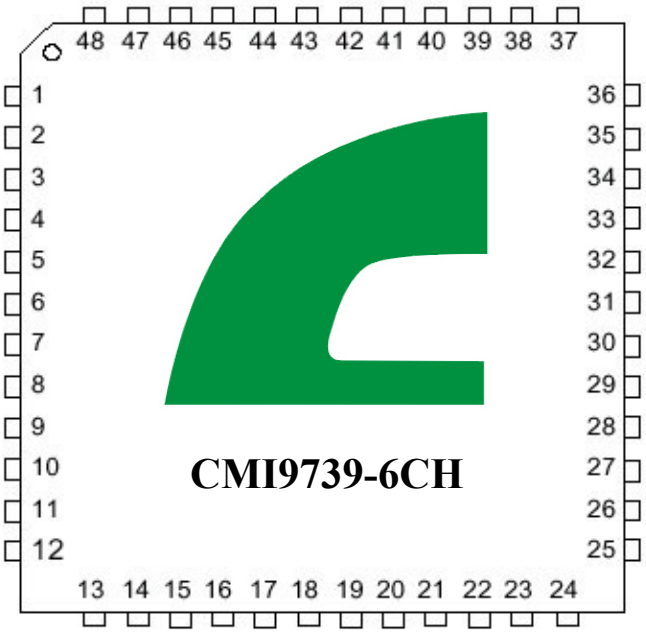
Features

- Intel® AC'97(Rev 2.2) compatible, meeting Microsoft's® PC2001 requirements
- Built-in earphone buffer and internal PLL, the latter saving additional crystal.
- Earphone buffer, optional on HP_OUT pins(9739) or LINE_HP_OUT pins(9739A).
- Line-in/rear out share the same jack.
- Center/bass share the MIC jack.
- Digital S/PDIF IN/OUT support
- 48 LQFP package.
- CRL® 3D: HRTF based DS3D compatible audio engine.
- EAX™ 1.0 & 2.0 compatible.
- Sensaura™ 3D audio enhancement (optional).
- 18-20bit DAC interface for SPDIF I/O(ICH4).

PIN DESCRIPTIONS

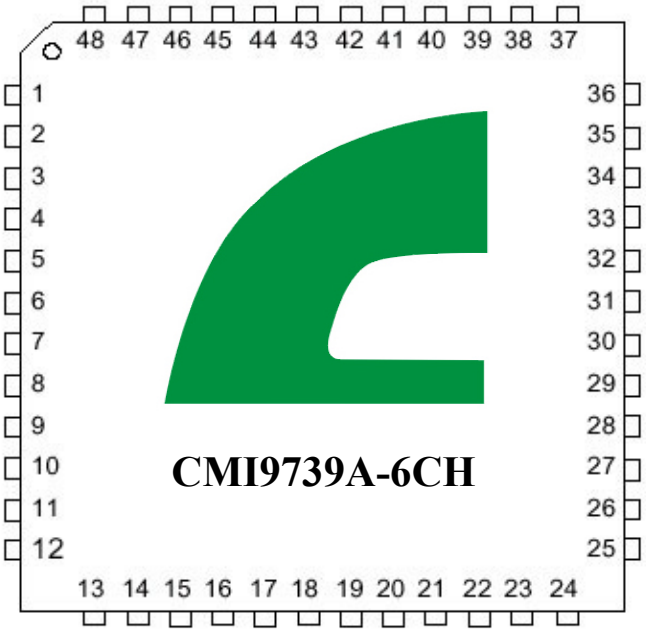
CMI9739

PIN #	Signal Name	PIN #	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	XTALS0
6	BIT_CLK	30	XTALS1
7	DVss2	31	**HP_OUT_L**
8	SDATA_IN	32	**HP_OUT_R**
9	DVdd2	33	NC
10	SYNC	34	NC
11	RESET#	35	**LINE_OUT_L**
12	PC_BEEP	36	**LINE_OUT_R**
13	NC	37	NC
14	AUX_L	38	AVdd2
15	AUX_R	39	S_OUT_L
16	NC	40	NC
17	NC	41	S_OUT_R
18	CD_L	42	AVss2
19	CD_GND	43	CENTER_OUT
20	CD_R	44	LFE_OUT
21	MIC1	45	HP_ON/GPIO0
22	MIC2	46	XTLSEL/GPIO1
23	LINE_IN_L	47	EAPD/SPDIF IN
24	LINE_IN_R	48	SPDIFO



CMI9739A

PIN #	Signal Name	PIN #	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	XTALS0
6	BIT_CLK	30	XTALS1
7	DVss2	31	**LINE_OUT_L**
8	SDATA_IN	32	**LINE_OUT_R**
9	DVdd2	33	NC
10	SYNC	34	NC
11	RESET#	35	**LINE_HP_OUT_L**
12	PC_BEEP	36	**LINE_HP_OUT_R**
13	NC	37	NC
14	AUX_L	38	AVdd2
15	AUX_R	39	S_OUT_L
16	NC	40	NC
17	NC	41	S_OUT_R
18	CD_L	42	AVss2
19	CD_GND	43	CENTER_OUT
20	CD_R	44	LFE_OUT
21	MIC1	45	HP_ON/GPIO0
22	MIC2	46	XTLSEL/GPIO1
23	LINE_IN_L	47	EAPD/SPDIF IN
24	LINE_IN_R	48	SPDIFO



CMI9739 mixer is designed according to the AC'97 specifications, capable of managing the playback and recording of all digital and analog audio sources in PC environment. It includes:

- **System audio:** digital PCM input and output for business, gaming, and multimedia applications.
- **CD/DVD**：analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**：Desktop or headset mic with programmable boost and gain
- **Speakerphone**：System mic & speakers for telephony, DSVD, and video conferencing.
- **Stereo line in**：Analog external line level source from consumer audio, video cameras, etc
- **AUX/synth**：Analog FM or wavetable synthesizer, or other internal sources.

SOURCE	FUNCTION	CONNECTION
PC_BEEP	PC beep pass through	from PC beeper output
MIC1	desktop microphone	from mic jack
MIC2	headset microphone	from headset mic jack
LINE_IN	external audio source	from line in jack
CD	audio from CD-ROM drive	cable from CD-ROM
AUX	upgrade synth or other external sources	internal connector
PCM out	digital audio output from AC '97 Controller	AC-link
Mix out	mix of all sources	AC '97 internal
Center_OUT	Center out channel	to output jack
LFE_OUT	Low frequency effect out channel	to output jack
LINE_OUT	stereo mix of all sources (front channel)	to output jack
REAR_OUT	stereo output of rear (surround) channel	to output jack
HP_OUT	stereo output with earphone buffer (NC for 9739A)	to output jack
PCM in	digital audio input to AC '97 Controller	AC-link

OUTPUT MIX SUPPORT:
•stereo mix of all sources for LINE_OUT
•stereo output for REAR_OUT

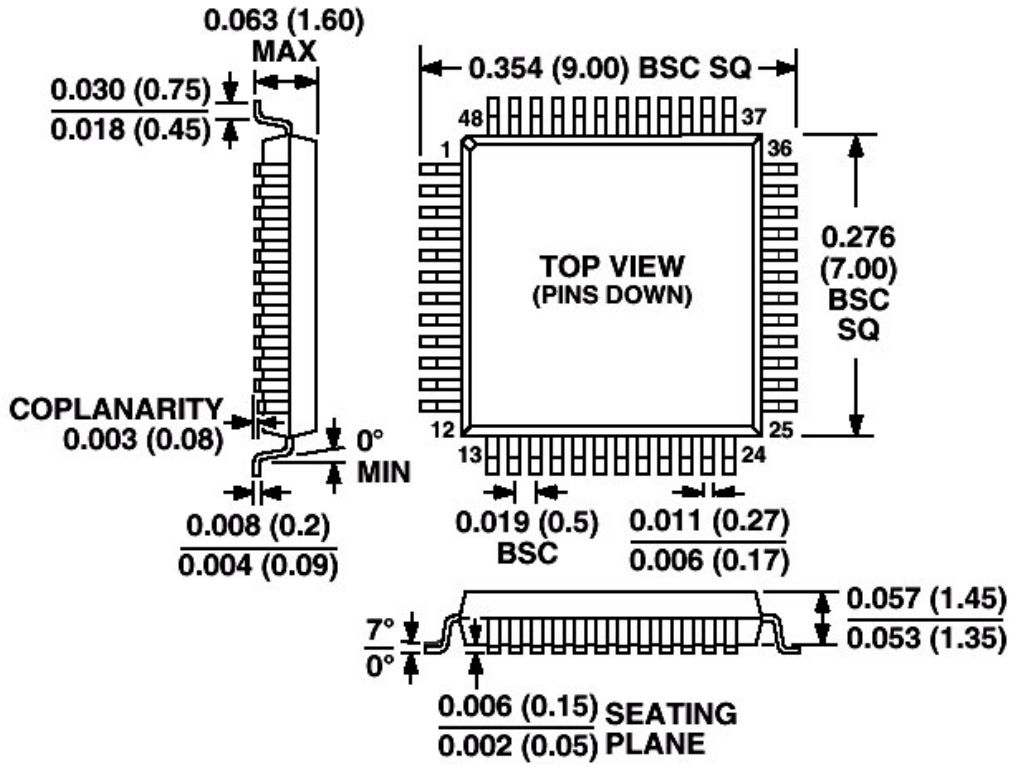
INPUT MUX SUPPORT:
•any mono or stereo source
•mono or stereo mix of all sources

2. ORDERING INFORMATION

Model Number	Package		Temperature Range	Supply Range
CMI9739	48-Pin LQFP	9mm×7mm×1.6mm	0 o C to +70 o C	DVdd = 3.3V, AVdd = 5V
CMI9739A	48-Pin LQFP	9mm×7mm×1.6mm	0 o C to +70 o C	DVdd = 3.3V, AVdd = 5V

Outline of Dimensions Dimensions shown in inches and (mm）

◆48-Lead Thin Plastic Quad Flatpack (LQFP) (ST-48)



***C-Media reserves the right to modify the specifications without further notice.**

TABLE OF CONTENTS

10. LIST OF FIGURES

11. LIST OF TABLES

3. PIN/SIGNAL DESCRIPTIONS

3.1 DIGITAL I/O

These signals connect CMI9739 to its AC'97 controller counterpart, external crystal, multi-codec selection, and external audio amplifier.

Table 1. Digital Signal List

Signal Name	Type	Description
RESET#	I	AC'97 master H/W reset
XTL_IN	I	24.576MHz crystal or external 14.318MHz clock source
XTL_OUT	O	24.576 MHz crystal
SYNC	I	48 kHz fixed rate sample sync
BIT_CLK	O	12.288 MHz serial data clock
SDATA_OUT	I	Serial, time division multiplexed, AC'97 input stream
SDATA_IN	O	Serial, time division multiplexed, AC'97 output stream

# denotes active low

3.2 ANALOG I/O

These signals connect CMI9739 to analog sources and sinks, including microphones and speakers.

Table 2. Analog Signal List

Signal Name	Type	Description
PC-BEEP	I	PC speaker input
AUX_IN_L	I	Aux left channel
AUX_IN_R	I	Aux right channel
CD_L	I	CD audio left channel
CD_R	I	CD audio right channel
CD_GND	I	CD audio analog ground
MIC1	I	Desktop microphone input
MIC2	O	Second microphone input
LINE_IN_L	I	Line in left channel
LINE_IN_R	I	Line In right channel
LINE_OUT_L	O	Line out left channel
LINE_OUT_R	O	Line out right channel
REAR_OUT_L	O	Rear out left channel
REAR_OUT_R	O	Rear out right channel
LFE_OUT	O	Low frequency effect out channel
Center_OUT	O	Center out channel

HP_OUT_L	O	Earphone left channel (for CMI9739)
HP_OUT_R	O	Earphone right channel (for CMI9739)
LINE_HP_OUT_L	O	Line out/ Earphone left channel (for CMI9739A)
LINE_HP_OUT_R	O	Line out /Earphone right channel (for CMI9739A)

3.3 REFERENCE PIN

This signal provides bias for micphone.

Table3. Filtering and Voltage References

Signal Name	Type	Description
Vrefout	O	Reference Voltage out 5mA drive

3.4 POWER AND GROUND SIGNALS

Table4. Power Signal List of CMI9739

Signal Name	Type	Description
AVdd1	I	Analog Vdd = 5V
AVdd2	I	Analog Vdd = 5V
Avss1	I	Analog Gnd
Avss2	I	Analog Gnd
DVdd1	I	Digital Vdd = 3.3V
DVdd2	I	Digital Vdd = 3.3V
DVss1	I	Digital Gnd
DVss2	I	Digital Gnd

3.5 CONFIGURATION SIGNALS

Table5. Configuration Signals of CMI9739

Signal Name	Type	Description
XTALS0	I	Select 14.318MHz as external clock when this pin is tied to digital power
XTALS1	I	Select 14.0MHz as external clock when this pin is tied to digital power, 12.288MHz when to ground. (XTALS0 has to be tied to ground)
XTLSEL	I	Select 24.576MHz crystal as clock source when is tied to digital power, select external clock as source when is tied to ground.

3.6 S/PDIF SIGNALS

Table6. S/PDIF Signals of CMI9739

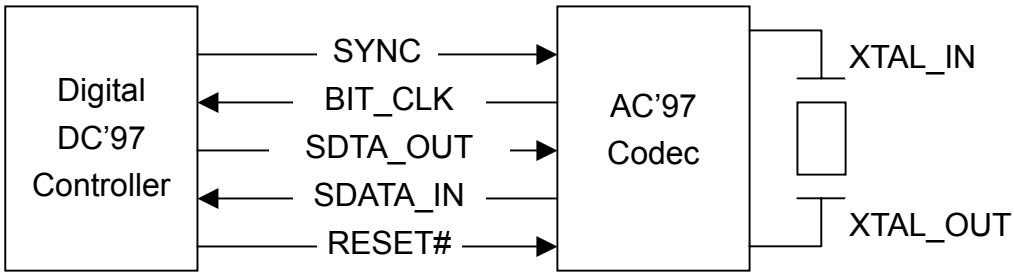
Signal Name	Type	Description
SPDIF IN	I	S/PDIF digital audio signal input
SPDIFO	O	S/PDIF digital audio signal output

4. DIGITAL INTERFACE

4.1 AC-LINK

All digital audio streams, optional modem line Codec streams, and command/status information intertransmit data over this AC-Link. A breakout of the signals connecting the two is shown in Figure 1.

Figure1. AC '97 connection to its companion controller



4.2 CLOCKING

CMI9739 generates its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controler is achieved through the BIT_CLK pin at 12.288 MHz（half **the** crystal frequency）.

The beginning of all audio sample packets or audio frames transmitted over AC-link is synchronized to the rising edge of the "SYNC" signal. "SYNC" is driven by the AC '97 Controller. Data is transmitted on AC-link and on every rising edge of BIT_CLK. Subsequently, it is sampled on the receiving side of AC-link on each immediately followed falling edge of BIT_CLK.

4.3 RESETTING

There are three types of reset detailed under "Timing Characteristics"：

1. A cold reset where all CMI9739 logic (registers included) is initialized to its default state
2. A warm reset where the contents of the CMI9739 register set are left unaltered
3. A register reset which only initializes the CMI9739 registers to their default states

After signaling a reset to CMI9739, the AC'97 controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indicator via register 26h from CMI9739.

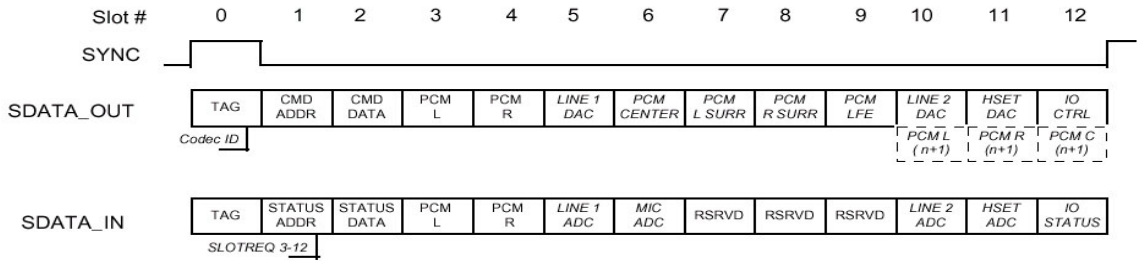
Note：When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is 1, it means that the AC-link, AC '97 control, and status registers are in a fully operating state.

4.4 AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

CMI9739 transits data to the AC'97 controller via a 5-pin digital serial AC-Link interface , which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands, and status information are transitted over this point-to-point serial transmission. The AC-Link processes multiple inputs, output audio streams, as well as control register accesses by a time division complex (TDM) scheme. The AC'97 controller synchronizes all AC-Link data transmissions.The following data streams are available on CMI9739：

· SDATA_OUT TAG	1 output slot (0)
· SDATA_IN TAG	1 input slot (0)
· Status (STATUS ADDR & DATA) read port	2 input slots (1,2)
· PCM L & R DAC Playback	2 output slots (3,4)
· PCM L & R ADC Record	2 input slots (3,4)
· PCM Center/LFE DAC Playback	2 output slots (6,9)
· PCM L-SURR/R-SURR DAC Playback	2 output slots (7,8)
· LINE2 DAC/HSET DAC Support 96K Audio Frame	2 output slots (10,11)

Figure2. AC '97 Standard Bi-directional Audio Frame



Synchronization of all AC-Link data transmissions is processed by the AC'97 controller. CMI9739 drives the serial bit clock onto AC-Link. The AC'97 controller then utilizes a synchronization signal to construct audio frames.

Fixed at 48 kHz, SYNC is derived by dividing the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, and can provide necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-Link serial data is transmitted on each rising edge of BIT_CLK. As the receiver of AC-Link data, CMI9739 for the outgoing data whereas AC'97 controller the incoming, sampling each serial bit on the falling edges of BIT_CLK.

The AC-Link protocol provides a special 16-bit (13-bit is defined with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the

corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data.

If a slot is "tagged" invalid, it should be the source of the data (CMI9739 for the input stream, AC'97 controller for the output stream) to fill in all bit positions with 0's during the active time of that slot.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Besides, for power saving, all clock, sync, and data signals can be halted.

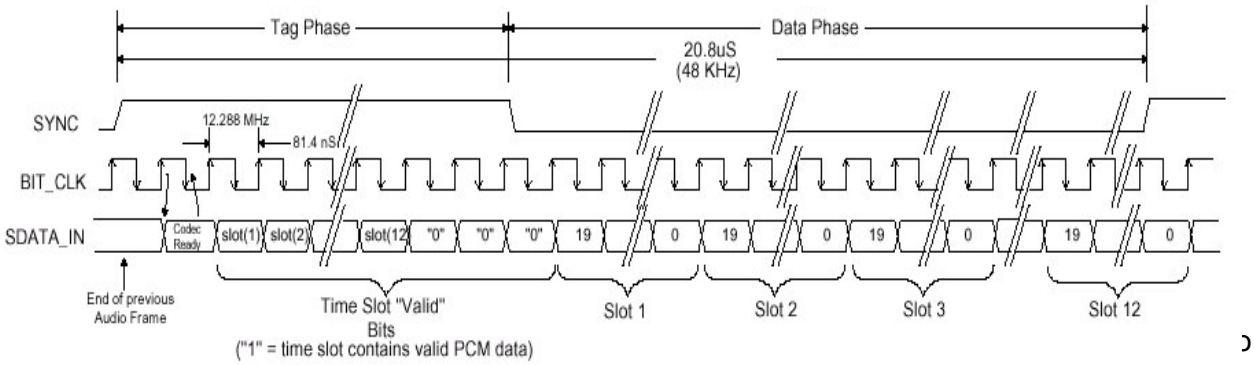
4.5 AC-LINK AUDIO INPUT FRAME（SDATA_IN）

The audio input frame data streams correspond to the complex bundles of all digital input data targeting the AC' 97 Controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20-bit timeslots. Slot 0 is a special reserved time slot containing 16-bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether CMI9739 is in the "CodecReady" state or not. If the "Codec Ready" bit is a 0, this indicates thatCMI9739 is not ready for normal operation. This condition is normal following the deassertion of power on reset for example, while CMI9739's voltage references settle. When the AC-link "Codec Ready" indicator bit is a 1 it indicates that the AC-link and CMI9739 control and status registers are in a fully operational state. The AC '97 Controller must further probe the Powerdown Control/Status Register (section 6.3) to determine exactly which subsections, if any, are ready.

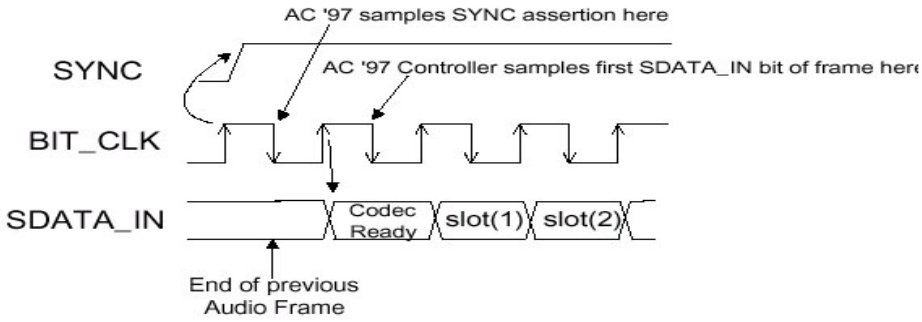
Prior to any attempts at putting CMI9739 into operation the AC '97 Controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that CMI9739 has gone "Codec Ready". Once CMI9739 is sampled "Codec Ready"8 then the next 12 bit positions sampled by the AC '97 Controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot-based AC-link protocol.

Figure3. AC-link Audio Input Frame



the rising edge of BIT_CLK. On the immediately followed falling edge of BIT_CLK, CMI9739 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, CMI9739 transmits SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the AC '97 Controller on the following falling edge of BIT_CLK. This sequence ensures that data transmits and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure4. Start of an Audio Input Frame



The composite stream of SDATA_IN is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) filled in with 0 by CMI9739. SDATA_IN data is sampled on the falling edges of BIT_CLK.

Slot 1: Status Address Port

The status port is used to monitor status for CMI9739 functions including, but not limited to, mixer settings and power management (refer to section 6.3 of this specification).

The stream of audio input frame slot 1 echoes the control register index, for prior reference, and for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by CMI9739 during slot 0.)

Status Address Port bit allocations:

Bit（19）	RESERVED	(Filled in with 0)
Bit（18：12）	Control Register Index	(Echo of register index for which data is being returned)
Bit（11：0）	RESERVED	(Filled in with 0's)

The first bit (MSB) generated by CMI9739 is always filled in with a 0. The following 7 bit positions transit the associated control register address, and the trailing 12 bit positions are filled in with 0 by CMI9739.

Slot 2: Status Data Port

The status data port delivers 16bit control register read data.

Bit（19：4）	Control Register Read Data	(Filled in by 0 if tagged "invalid")
Bit（3：0）	RESERVED	(Filled in by 0)

If Slot 2 is tagged invalid by CMI9739, then the entire slot will be filled in with 0.

Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of CMI9739 input MUX and post-ADC. CMI9739 ADCs are implemented to support 16bit resolution.
CMI9739 outputs its ADC data (MSB first), and fills in any trailing non-valid bit positions by 0 to fill with its 20bit time slot.

Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of CMI9739 input MUX and post-ADC. CMI9739 outputs its ADC data (MSB first), and fills in any trailing non-valid bit positions by 0 to fill in its 20bit time slot

.

Slot 5: Optional Modem Line 1 ADC

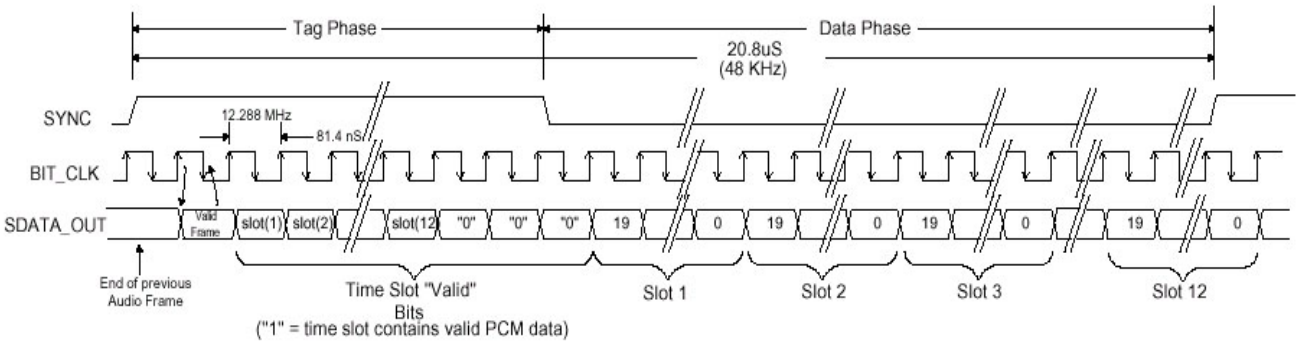
Audio input frame slots 5-12 are not used by CMI9739 and are always filled in with 0.

4.6 AC-LINK AUDIO OUTPUT FRAME（SDATA_OUT）

The audio output frame data streams correspond to the complex bundles of all digital output data targeting the CMI9739 DAC inputs, and control registers. Each audio output frame supports up to 12 to 20bit outgoing data time slots. Slot 0 is a specially reserved time slot containing 16bit that is used for AC-Link protocol infrastructure.

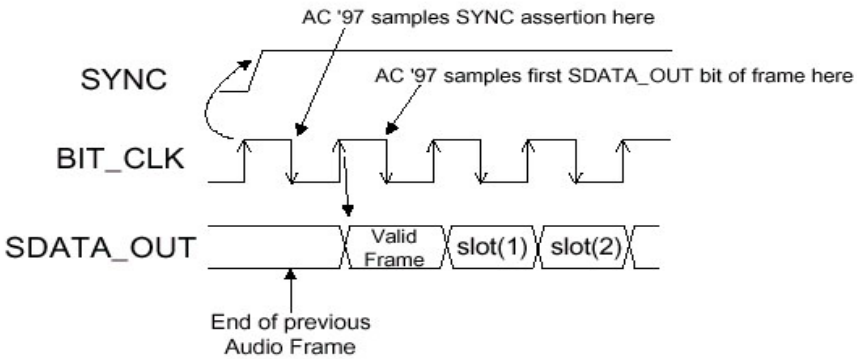
Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by CMI9739 indicate which of the corresponding 12 times slots contain valid data. In this way data streams of different sample rates can be transmitted across AC-Link at its fixed 48kHz audio frame rate. The following diagram illustrates the time slot based AC-Link protocol.

Figure5 . AC-Link Audio Output Frame



CMI9739 on the following falling edge of BIT_CLK. This sequence ensures that data transmissions and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 6. Start of an Audio Output Frame



SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions AC'97 controller. When mono audio sample streams are sent from the AC'97 controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

Slot 1: Command Address Port

The command port is used to control features and monitor status (see Audio Input Frame Slots 1 and 2) of the CMI9739 functions including, but not limited to, mixer settings, and power management (please refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid.

Audio output frame slot 1 transits control register address, and write/read command information to CMI9739.

Command Address Port bit allocations：

Bit（19）	Read/Write command	(1=read, 0=write)
Bit（18：12）	Control Register Index	(64 16-bit locations,addressed on even byte boundaries)
Bit（11：0）	Reserved	(Filled in with 0's)

The first bit (MSB) sampled by CMI9739 indicates whether the current control transmission is in a read or a write mode. The following 7 bit positions transit the targeted control register address. The trailing 12 bit positions within the slot are reserved and must be filled in with 0 by the AC '97 Controller.

Slot 2: Command Data Port

The command data port is used to deliver 16bit control register write data in the event that the current command port mode is in a write cycle. (as indicated by Slot 1, bit 19)

Bit（19：4）	Control Register Write Data	(filled in with 0 if current mode is read)
Bit（3：0）	Reserved	(filled in with 0)

If the current command port mode is in read then the entire slot time must be filled in with 0 by the AC'97 controller.

Slot 3: PCM Playback Left Channel

In a common"Games Compatible" PC, the slot comprises standard PCM (.wav), output samples digitally mixed (by the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20bit is transmitted, the AC'97 controller must fill in all trailing non-valid bit positions by 0 within this time slot.

Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a common "Games Compatible" PC, this slot comprises standard PCM (.wav) output samples digitally mixed (by the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20bit is transmitted, the AC'97 controller must fill in all trailing non-valid bit positions with 0 within this time slot.

Slot 5: Reserved

Audio output frame slot 5 is reserved for modem, not used by CMI9739.

Slot 6: PCM Center Channel

Slot 6 carries Center data in 6 channel wave output.

Slot 7: PCM Left Surround Channel

Slot 7 carries PCM left surround data in 6 channel wave output.

Slot 8: PCM Right Surround Channel

Slot 8 carries PCM right surround data in 6 channel wave output.

Slot 9: PCM Low Frequency Channel

Slot 9 carries Low Frequency data in 6 channel wave output.

Slot 10: PCM Alternate Left

Audio output frame slot 10 is not used by CMI9739.

Slot 11: PCM Alternate Right

Audio output frame slot 11 is not used by CMI9739.

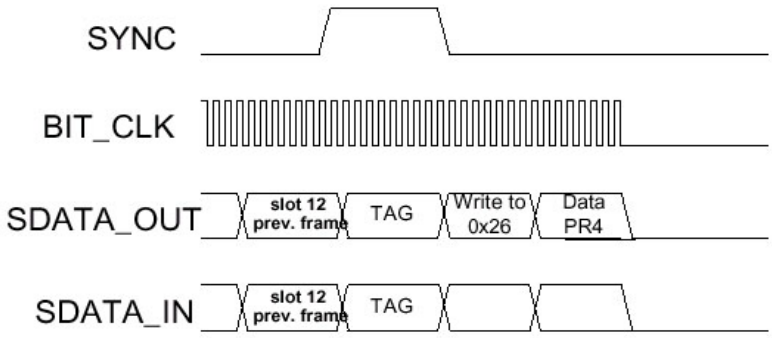
Slot 12: Reserved

Audio output frame slot 12 is reserved for modem, not used by CMI9739.

4.7 AC-LINK LOW POWER MODE

The CMI9739 AC-Link can be placed in the low power mode by programming register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC'97 controller can wake up CMI9739 by providing the appropriate reset signals.

Figure 7. AC-link Powerdown Timing



BIT_CLK and SDATA_IN are transmitted low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC and SDATA_OUT low after programming CMI9739 to this low power mode.

Waking up the AC-link

Once CMI9739 has halted BIT_CLK, there are only two ways to "wake up" the AC-Link. Both methods must be activated by the AC'97 controller. The AC-Link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current power down state would ultimately dictate which form of reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes. Once powered down, re-activation of the AC-Link via re- assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-Link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold AC '97 Reset ➔a cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low and BIT_CLK, SDATA_IN will be activated, or re-activated as the case may be, and all CMI9739 control registers will be initialized to their default power on reset values.

Note: RESET# is an asynchronous input.

# denotes active low.

Warm AC'97 Reset ➔a warm reset will re-activate the AC-Link without altering the current CMI9739 register values. A warm reset is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the CMI9739.

5. CMI9739 MIXER

The CMI9739 mixer is designed according to to the AC'97 specifications, capable of managing the playback and recording of all digital and analog audio sources in the PC environment. It includes：

- **System audio**：digital PCM input and output for business, gaming, and multimedia applications.
- **CD/DVD**：analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer.
- **Mono microphone**：Desktop or headset mic, with programmable boost and gain.
- **Speakerphone**：System mic & speakers for telephony, DSVD, and video conference.
- **Stereo line in**：analog external line level source from consumer audio, video cameras, etc.
- **AUX/synth**：analog FM or wavetable synthesizer, or other internal sources.

Table 7. Mixer Functional Connections

SOURCE	FUNCTION	CONNECTION
PC_BEEP	PC beep pass through	from PC beeper output
MIC1	desktop microphone	from mic jack
MIC2	headset microphone	from headset mic jack
LINE_IN	external audio sources	from line in jack
CD	audio from CD-ROM drive	cable from CD-ROM
AUX	upgrade synth or other external sources	internal connector
PCM out	digital audio output from AC '97 Controller	AC-link
Mix out	mix of all sources	AC '97 internal
Center_OUT	Center out channel	to output jack
LFE_OUT	Low Frequency Effect out channel	to output jack
LINE_OUT	stereo mix of all sources (front channel)	to output jack
REAR_OUT	stereo output of rear (surround) channel	to output jack
PCM in	digital audio input to AC '97 Controller	AC-link

OUTPUT MIX SUPPORT:
•stereo mix of all sources for LINE_OUT
•stereo output for REAR_OUT

INPUT MUX SUPPORT:
•any mono or stereo source
•mono or stereo mix of all sources

5.1 MIXER INPUT

The input of CMI9739 mixer is a MUX design which offers the capability to record audio sources or the outgoing mix of all sources. This design is more efficient to implement, compared with an independent input mix. It offers simple monitoring when a mix is recorded: what you hear is what you get (WYHIWYG). CMI9739 supports the following input sources：

◆any mono or stereo source

◆mono or stereo mix of all sources

5.2 MIXER OUTPUT

The mixer generates four distinct outputs:

- ◆a stereo mix of all sources for output to the LINE_OUT
- ◆a stereo output of rear (surround) channel for REAR_OUT
- ◆a mono output of center channel for CENTER_OUT
- ◆a mono output of Low Frequency Effect channel for LFE_OUT

6. REGISTER INTERFACE

Table 8. Mixer Registers

Reg NUM	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0000h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
0Ah	PC_BEEP volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	BOOST	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line-In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol	Mute	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	x	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	X	X	X	X	X	X	X	MS	LPBK	X	X	X	X	X	X	X	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh
28h	Extended Audio ID	ID1	ID0	X	X	REV1	REV0	X	LDAC	SDAC	CDAC	DSA1	DSA0	X	SPDIF	DRA	X	05C6h
2Ah	Extended Audio Stat/Ctrl	X	X	PRK	PRJ	PRI	SPCV	X	LDAC	SDAC	CDAC	SPSA1	SPSA0	X	SPDIF	DRA	X	3C30h
36h	Center/LFE Mute Control	LFE Mute	X	X	X	X	X	X	X	C Mute	X	X	X	X	X	X	X	8080h
38h	6CH Vol:L,R Surr	Mute	X	X	X	X	X	X	X	Mute	X	X	X	X	X	X	X	8080h
3Ah	S/PDIF Control	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	Copy	Audio	PRO	2000h
5Ah	Vendor Defined Control	REV15	REV14	REV13	REV12	REV11	REV10	REV9	REV8	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	0000h
64h	Vender Define	REV15	REV14	REV13	REV12	REV11	REV10	REV9	REV8	REV7	REV6	REV5	REV4	REV3	REV2	REV1	BSTSEL	0000h
66h	Vendor Defined Control	REV15	REV14	REV13	REV12	REV11	REV10	REV9	REV8	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	0000h
68h	SPDIF IN0	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	0000h

6Ah	SPDIF IN1	SP31	SP30	SP29	SP28	SP27	SP26	SP25	SP24	SP23	SP22	SP21	SP20	SP19	SP18	SP17	SP16	0000h
6Ch	SPDIF Function Control	X	X	X	X	X	X	X	SPD32	X	X	X	SPI2SDI	SPI2F	IG_SPIV	SPDIFS	SPDI_EN	0000h
70h	GPIO Setup	GPI2SDI	GPITAG	X	X	X	X	GP1I/O	GP0I/O	X	X	GPIO1P	GPIO0P	X	X	GPI1EN	GPI0EN	0000h
72h	GPIO Status	X	X	X	X	X	X	GPII1S	GPII0S	X	X	GPIO1S	GPIO0S	X	X	GPO1	GPO0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	434Dh
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	4961h

6.1 Register Descriptions

Reset Register (Index 00h) (Read Only)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	0000h

No Hardware 3D : SE4…SE0 = 00000b
16bit ADC & DAC : ID9…ID0 = 0000000000b
Writing this register will reset the mixer register.

Master Volume Registers (Index 02h)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h

◆Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set at -∞ dB.

◆The volume control bit per channel is 5. Support for the 6th bit (MSB) of the level is optional. If it is written by 1, CMI9739 will interpret that as x11111. It will also respond when read with x11111 rather then 1xxxxx, the value written to it. The default value is 8000h, which corresponds to 0dB attenuation with mute.

Mute	*M*x5...*M*x0	Function
0	000000	0 dB Attenuation
0	011111	46.5dB Attenuation
0	1xxxxx	46.5dB Attenuation
1	xxxxxx	∞ dB Attenuation

PC BEEP Volume Registers (Index 0Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	PC BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h

◆The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set at -∞ dB. The default value is 0000h, which corresponds to 0dB attenuation with mute off.

Mute	*PV3*...PV0	Function
0	0000	0 dB Attenuation
0	1111	45dB Attenuation
1	xxxx	∞ dB Attenuation

Analog Mixer Input Gain Registers (Index 0Eh - 18h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	**Mic Volume**	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	**LineIn Volume**	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	**CD Volume**	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	**Aux Volume**	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	**PCM Out Vol**	Mute	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	8808h

◆ Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set at -∞ dB.

◆Register 0Eh (Mic Volume Register) has an extra bit that is for a 20 dB boost. When bit 6 is set to 1, the 20 dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on.

Mute	*G*x4...Gx0	Function
0	00000	12dB Gain
0	01000	0 dB Attenuation
0	11111	34.5dB Attenuation
1	xxxx	∞ dB Attenuation

Record Select Control Register (Index 1Ah) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	**Record Select**	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h

The default value is 0000h, which corresponds to Mic in.

SR2...SR0	Right Record Source
0	Mic
1	CD In (R)
2	N/A
3	Aux In (R)
4	Line In (R)
5	Stereo Mix (R)
6	Mono Mix
7	**PC BEEP**

SL2...SL0	Left Record Source
0	Mic
1	CD In (L)
2	N/A
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	**PC BEEP**

◆ If Sx0-2 are written by 7, it selects record from PC BEEP channel. It makes PC BEEP input channel equivlent to PHONE-IN.

Record Gain Registers (Index 1Ch) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	**Record Gain**	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h

◆Each step corresponds to 1.5 dB. 22.5dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB. The default value is 8000h, which corresponds to 0 dB gain with mute on.

Mute	*G*x3...*G*x0	Function
0	1111	+22.5 dB Gain
0	0000	0 dB Gain
1	xxxxx	∞ dB Attenuation

General Purpose Register (Index 20h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	**General Purpose**	X	X	X	X	X	X	X	MS	LPBK	X	X	X	X	X	X	X	0000h

Bit	Function
LPBK	ADC/DAC loopback mode
MS	Microphone selection: 0=MIC1,1=MIC2

Powerdown Control/Status Register (Index 26h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	**Powerdown Ctrl/Stat**	X	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Xh

◆This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is "ready". Ready is defined as the subsection is able to perform in its nominal state. When this register is written, the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and AC '97 control and status registers are in a fully operational state. The AC '97 Controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Bit	Function
X	Reserved
REF	Vref's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

These bits are pseudo. Default are ready and controlled by PRX.

Bit	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (external clk off)
PR5	Internal Clk disable
PR6	*HP amp powerdown*

Except for PR4, other bits are pseudo.
When is set, corresponding bits will be not ready.
Ex. PR1 =1 causes DAC=0.
PRXX must set the volume to mute!!
PR4 when is set, will shut down the ACLINK.

Extended Audio ID Register (Index 28h) (Read Only)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1	ID0	X	X	REV1	REV0	X	LDAC	SDAC	CDCA	X	X	X	SPDIF	DRA	X	05C6h

◆ID1,ID0 is always "00".
◆REV[1:0]=1 indicated that CMI9739 is AC'97 rev2.2 compliant.
◆SDAC=1 indicates PCM Surround DAC is supported.
◆LDAC=1 indicates PCM LFE DAC is supported.
◆CDAC=1 indicates PCM Center DAC is supported.
◆SPDIF=1 indicates SPDIF is supported.
◆DRA=1 indicates Double Rate Audio is supported.

Extended Audio Status and Control Register (Index 2Ah)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Extended audio Stat/Ctrl	X	X	PRK	PRJ	PRI	SPCV	X	LDAC	SDAC	CDAC	SPSA1	SPSA0	X	SPDIF	DRA	X	3C30h

◆DRA=1 enables double-rate audio mode

◆SPDIF=1 enables the S/PDIF transmitter, S/PDIF defaults to transmitter off (powerdown)

◆SPSA[1:0]=00, S/PDIF source data assigned to AC-link slots 3&4

◆SPSA[1:0]=01, S/PDIF source data assigned to AC-link slots 7&8

◆SPSA[1:0]=10, S/PDIF source data assigned to AC-link slots 6&9

◆SPSA[1:0]=11, S/PDIF source data assigned to AC-link slots 10&11(default)

◆Bits D6-8 is read only status of the extended audio feature readiness:

SDAC=1 indicates the PCM Surround DACs are ready,

CDAC=1 means Center DACs are ready,

LDAC=1 means LFE DACs are ready.

◆SPCV=1 indicates current S/PDIF configuration {SPSA} is supported

◆Bits D11-13 are read/write controls of the extended audio feature powerdown:

PRJ=1 turns the PCM Surround DACs off,

PRI=1 Center DACs off,

PRK=1 LFE DACs off.

◆The default value after cold or warm register reset for this register (xxxxh) is all extended features disabled (D3-D0=0) and powered down (D12=1). The feature readiness status should always be accurate (D7=x).

These bits are pseudo.

When in 2CH and 6CH, these bits are still visible.

PRXX must set volume to mute

Center/LFE Channel Mute Control (Index 36h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
36h	Center/LFE Mute	LFE Mute	X	X	X	X	X	X	X	C Mute	X	X	X	X	X	X	X	8080h

◆ The D15/D7 of the register are the mute bits. When these bits are set to 1, the level for that channel(s) is set at -∞ dB.

Surround Channel Mute Control (Index 38h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
38h	Surround Mute	L Mute	X	X	X	X	X	X	X	R Mute	X	X	X	X	X	X	X	8080h

◆ The D15/D7 of the register are the mute bits. When these bits are set to 1, the level for that channel(s) is set at -∞ dB.

S/PDIF Output Channel Status and Control (Index 3Ah) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ah	S/PDIF Ctl	V	X	SPSR1	SPSR0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	Copy	Audio	Pro	2000h

◆V : Validity, If this bit is set to 1, each S/PDIF subframe should have bit 28 "Valid flag" = 1. This tags both samples as Invalid.

◆SPSR[1:0] is "10", and it means sample rate is 48kHz.

◆L : Generation Status

◆ CC[6:0] : Category Code

◆PRE: Pre-emphasis

◆ COPY : Copyright (0: copy inhibited, 1: copy permitted)

◆ AUDIO : Audio Mode (0: PCM, 1: AC-3 or other non-PCM data)

◆ PRO : Professional or Consumer Format (0: consumer, 1: professional)

Vendor Defined Register (Index 5A/66h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah	Vendor Defined Control	REV 15	REV 14	REV 13	REV 12	REV 11	REV 10	REV 9	REV 8	REV 7	REV 6	REV 5	REV 4	REV 3	REV 2	Rev 1	REV0	0000h
66h	Vendor Defined Control	REV 15	REV 14	REV 13	REV 12	REV 11	REV 10	REV 9	REV 8	REV 7	REV 6	REV 5	REV 4	REV 3	REV 2	Rev 1	REV0	0000h

◆All of registers are reserved. Please do not write any value!

Multi-channel Control Register (Index 64h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
64h	Mixer Control	PCB SW	P47	REF Ctl	CLCtl	X	S2LNI	MIX2S	X	X	X	X	X	X	X	X	BSTSEL	0000h

◆PCBSW : Controls PCBEEP Path
0: Bypass master volume/mute controls,
1: PC BEEP controls by master volume/mute
◆P47: Configures the Pin 47 Definition
0: as SPDIFIN,
1: as EAPD out
◆REF Ctl: Internal Vref Output for Micphone Bios
0: No internal Vref output,
1: internal Vref output enabled
◆CLCtl: Center/LFE Channel Output Control
0: No Center/LFE output,
1: Center/LFE output enabled
◆S2LNI: Line-In/ Surround Output Control
0: Chip LINE_IN pins as line-in purpose
1: Chip LINE_IN pins as surround output purpose.
◆MIX2S: Analog Input Pass to Surround Control
0: off
1: on
◆BSTSEL: MIC Boost Selection
0: for 20dB ,
1: for 30dB

S/PDIF-IN Status Register(Index 68/6Ah) (R/O)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
68h	SPDIF IN Status0	SPIS15	SPIS14	SPIS13	SPIS12	SPIS11	SPIS10	SPIS9	SPIS8	SPIS7	SPIS6	SPIS5	SPIS4	SPIS3	SPIS2	SPIS1	SPIS0	0000h
6Ah	SPDIF IN Status0	SPIS31	SPIS30	SPIS29	SPIS28	SPIS27	SPIS26	SPIS25	SPIS24	SPIS23	SPIS22	SPIS21	SPIS20	SPIS19	SPIS18	SPIS17	SPIS16	0000h

These registers are read only and indicate SPDIF-IN consumer status bits data.

◆SPIS30-31: Reserved

◆SPIS28-29: Clock Accuracy

◆SPIS24-27: Sample Frequency

0000: 44.1KHz,

0010: 48KHz,

Others: reserved

◆SPIS20-23: Channel Number

◆SPIS16-19: Source Number

◆SPIS15 : Generation Status

◆SPIS8-14 : Category Code

◆SPIS6-7: Mode

◆SPIS3-5: Pre-Emphasis

◆SPIS2: Copyright (0: copy inhibited, 1: copy permitted)

◆SPIS1: Audio Mode (0: PCM, 1: AC-3 or other non-PCM data)

◆SPIS0: Professional or Consumer Format (0: consumer, 1: professional)

S/PDIF Function Control Register(Index 6Ch) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
6Ch	SPDIF Function Control	X	X	X	X	X	X	X	SPD32	X	X	X	SPI2SDI	SPI2F	IG_SPIV	SPDIFS	SPDI_EN	0000h

◆SPDI_EN : S/PDIF Input Function Control

0: SPDIF IN disable,

1: SPDIF IN enable

◆SPDIFS: S/PDIF Output Source
0: S/PDIF output data is from controller,
1: S/PDIF output data is from ADC

◆IG_SPIV: S/PDIF Input Valid Bit Processing
0: ignore valid bit,
1: valid bit active

◆SPI2F: S/PDIF Input Data Send to Front Channel for Monitoring
0: Front channel is from ACLINK,
1: Front channel if from S/PDIF IN

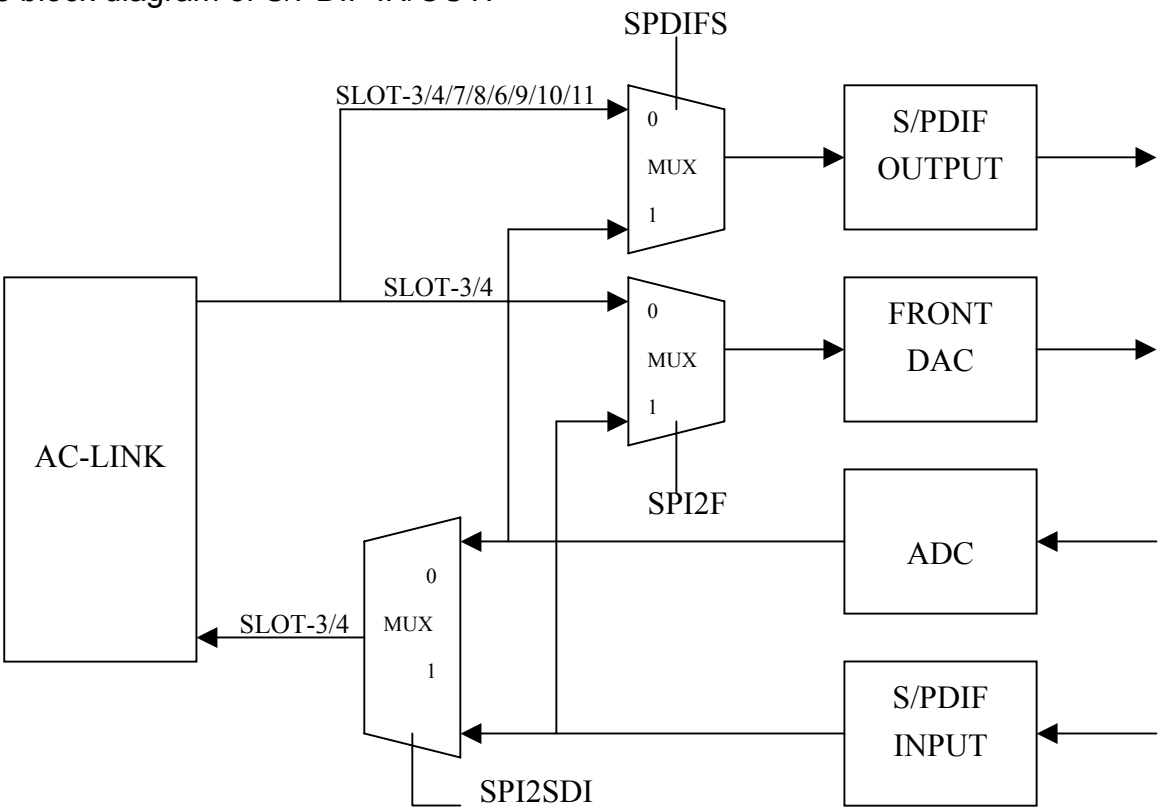
◆SPI2SDI: S/PDIF Input Data Send to Controller
0 : S/PDIF IN is not to SDATA_IN,
1 : S/PDIF IN is to SDATA_IN

◆SPD32: 32bit Software support mode for SPDIF OUT
SPDIF OUT is controlled by software using slot3&7 for left channel, slot4&8 for right channel. Parts of slot3[19:0], slot4[19:0], slot7[19:0] and slot8[19:0] will be selected to form SPDIF 32bit:
→ slot3[19:4]+slot4[19:4] to form one 32bit subframe
→ slot7[19:4]+slot8[19:4] to form the following 32bit subframe
slot3[7:4] and slot7[7:4] are for header

	slot[4]	slot[5]	slot[6]	slot[7]
Header_B	1	0	0	0
Header_M	0	0	1	0
Header_W	0	1	0	0

SPDIF 32 bit mapping:
0-3 Header → by slot3[4:7] or slot7[4:7]
4-15 → slot3[8]… slot3[19] (or slot7[8]… slot7[19])
16-31 → slot4[4]… slot4[19](or slot8[4]…slot8[19])

The block diagram of S/PDIF IN/OUT:



GPIO Setup and GPIO Status Register(Index 70/72h) (R/W)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
70h	**GPIO Setup**	GPI 2SDI	GPI TAG	X	X	X	X	GPI1 I/O	GPI 0 I/O	X	X	GPI O1P	GPI O0P	X	X	GPI 1EN	GPI0 EN	0000h
72h	**GPIO Status**	X	X	X	X	X	X	GPII1S	GPII 0S	X	X	GPI O1S	GPI O0S	X	X	GP O1	GPO 0	0000h

◆GPI2SDI: GPIO Status Indication in SDATA_IN

0: The GPIO0/GPIO1 status and its valid tag are not indicated in SDATA_IN.

1: The GPIO0/GPIO1 status and its valid tag are indicated in SDATA_IN

◆GPITAG:

0: GPI TAG (slot12) is inactive,

1: GPI TAG (slot12) is active when GPI INT asserted

◆GPIO1I/O: GPIO1 Function Control

0: Set GPIO1 as input pin.

1: Set GPIO1 as output pin.

◆GPIO0I/O: GPIO0 Function Control

0: Set GPIO0 as input pin.

1: Set GPIO0 as output pin.

◆GPIO1P: GPIO1 Interrupt Polarity

0: Low to high transition (default)

1: High to low transition

◆GPIO0P: GPIO0 Interrupt Polarity

0: Low to high transition (default)

1: High to low transition

◆GPI1EN: GPIO1 Interrupt Enable (when GPIO1 is used as input)

0: Disable

1: Enable.

A transaction which polarity depends on GPIO1P will trigger the GPIO interrupt in bit0 of SDATA_IN's slot 12. Software has to confirm the primitiveness of GPIO1 before enabling GPIO1's interrupt.

◆GPI0EN: GPIO0 Interrupt Enable (when GPIO0 is used as input)

0: Disable

1: Enable.

A transaction which polarity depends on GPIO0P will trigger the GPIO interrupt in bit0 of SDATA_IN's slot 12. Software has to confirm the primitiveness of GPIO0 before enabling GPIO0's interrupt.

◆GPII1S: GPIO1 Interrupt Status. (when GPIO1 is used as input)

0: No GPIO1 interrupt.

1: GPIO1 interrupt.

◆GPII0S: GPIO0 Interrupt Status. (when GPIO0 is used as input).

0: No GPIO0 interrupt.

1: GPIO0 interrupt.

◆GPIO1S: GPIO1 Input Status

0: GPIO1 is driven low by external device.

1: GPIO1 is driven high by external device.

◆GPIO0S: GPIO0 Input Status

0: GPIO0 is driven low by external device.

1: GPIO0 is driven high by external device.

◆GPO1: GPIO1 Output Control

0: Drive GPIO1 low.

1: Drive GPIO1 high.

◆GPO0: GPIO0 Output Control

0: Drive GPIO0 low.

1: Drive GPIO0 high.

Vendor ID Registers (Index 7Ch - 7Eh) (Read Only)

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	**Vendor ID1**	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	434Dh
7Eh	**Vendor ID2**	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	4961h

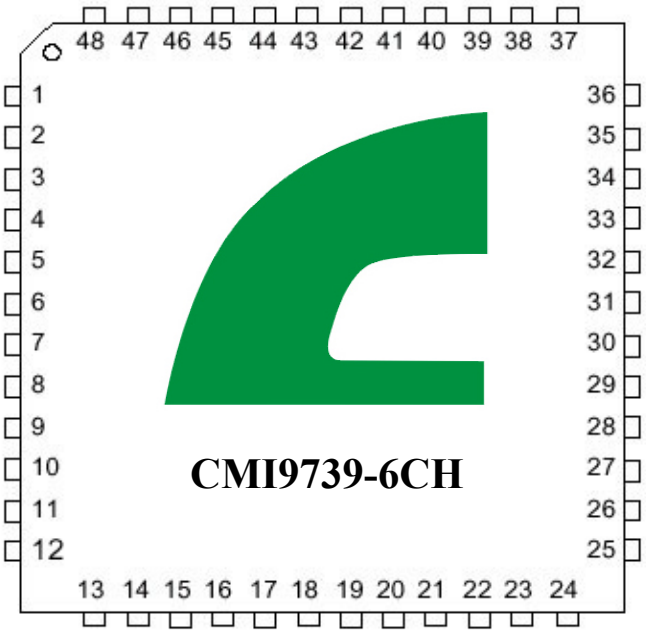
7Ch : 434Dh ASCII code : CM

7Eh : 4961h ASCII code: I a

6.2 PIN DESCRIPTIONS

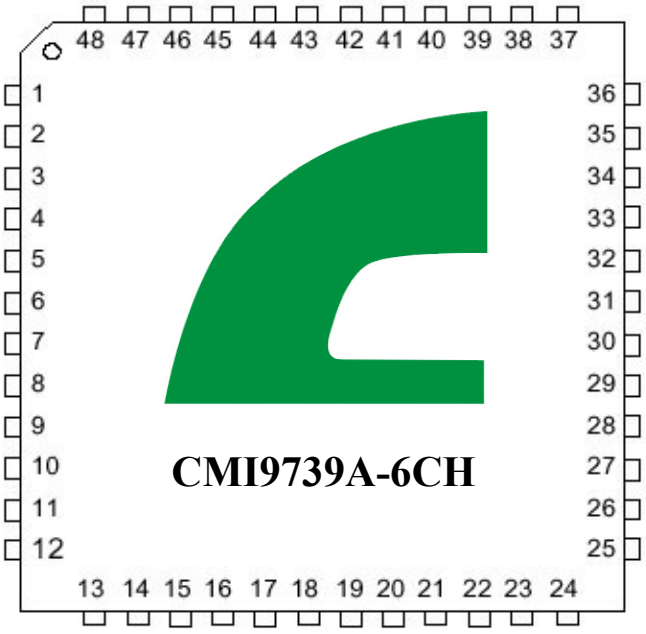
CMI9739

PIN #	Signal Name	PIN #	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	XTALS0
6	BIT_CLK	30	XTALS1
7	DVss2	31	**HP_OUT_L**
8	SDATA_IN	32	**HP_OUT_R**
9	DVdd2	33	NC
10	SYNC	34	NC
11	RESET#	35	**LINE_OUT_L**
12	PC_BEEP	36	**LINE_OUT_R**
13	NC	37	NC
14	AUX_L	38	AVdd2
15	AUX_R	39	S_OUT_L
16	NC	40	NC
17	NC	41	S_OUT_R
18	CD_L	42	AVss2
19	CD_GND	43	CENTER_OUT
20	CD_R	44	LFE_OUT
21	MIC1	45	HP_ON/GPIO0
22	MIC2	46	XTLSEL/GPIO1
23	LINE_IN_L	47	EAPD/SPDIF IN
24	LINE_IN_R	48	SPDIFO



CMI9739A

PIN #	Signal Name	PIN #	Signal Name
1	DVdd1	25	AVdd1
2	XTL_IN	26	AVss1
3	XTL_OUT	27	Vref
4	DVss1	28	Vrefout
5	SDATA_OUT	29	XTALS0
6	BIT_CLK	30	XTALS1
7	DVss2	31	**LINE_OUT_L**
8	SDATA_IN	32	**LINE_OUT_R**
9	DVdd2	33	NC
10	SYNC	34	NC
11	RESET#	35	**LINE_HP_OUT_L**
12	PC_BEEP	36	**LINE_HP_OUT_R**
13	NC	37	NC
14	AUX_L	38	AVdd2
15	AUX_R	39	S_OUT_L
16	NC	40	NC
17	NC	41	S_OUT_R
18	CD_L	42	AVss2
19	CD_GND	43	CENTER_OUT
20	CD_R	44	LFE_OUT
21	MIC1	45	HP_ON/GPIO0
22	MIC2	46	XTLSEL/GPIO1
23	LINE_IN_L	47	EAPD/SPDIF IN
24	LINE_IN_R	48	SPDIFO



7. AC-LINK TIMING CHARACTERISTICS

(Tambient = 25 °C, AVdd = 5.0V ± 5% ,DVdd = 3.3V ± 5%, AVss=DVss+0V; 50pF external load)

7.1 COLD RESET

Figure 8. Cold Reset Timing Diagram

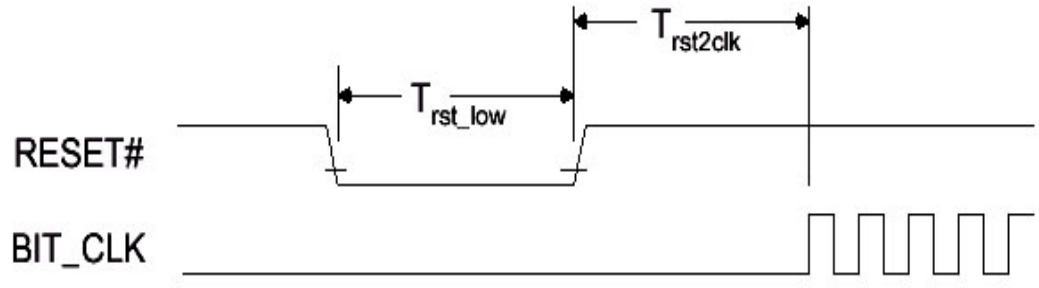


Table 9. Cold Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

# denotes active low.

7.2 WARM RESET

Figure 9. Warm Reset

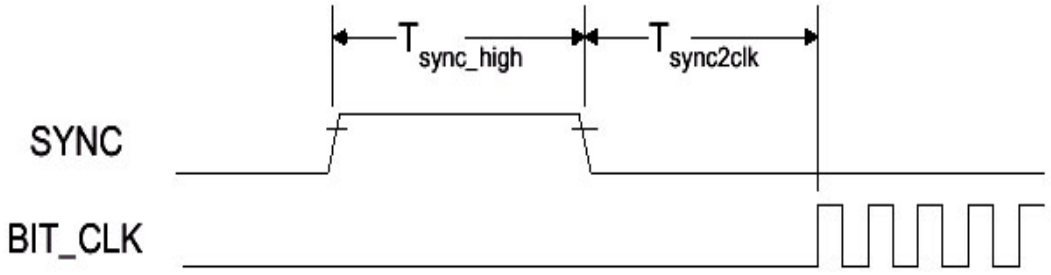


Table 10. Warm Reset

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tres_high	1.0	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

7.3 CLOCKS

Figure 10. BIT_CLK to SYNC Timing Diagram

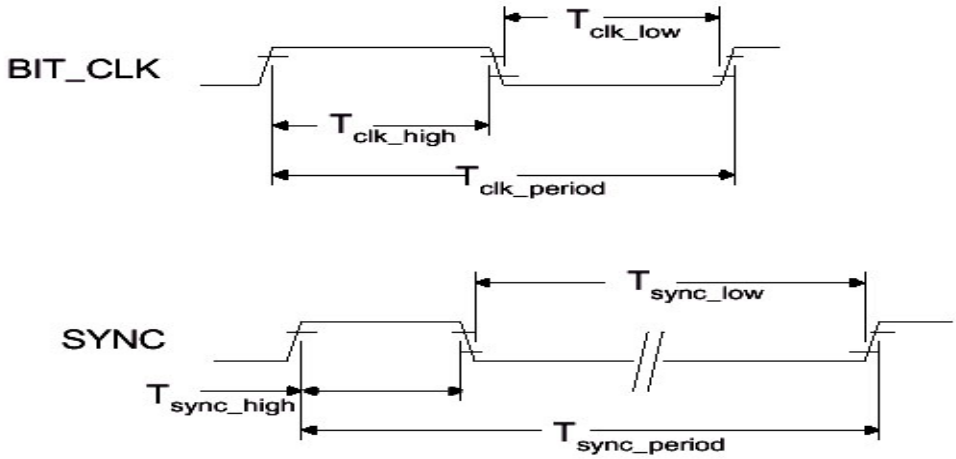


Table 11. Clocks

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BLT_CLK high pulsewidth (note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Note: Worst case duty cycle restricted to 45/55.

7.4 DATA SETUP AND HOLD

(50pF external load)

Figure 11. Data Setup and Hold

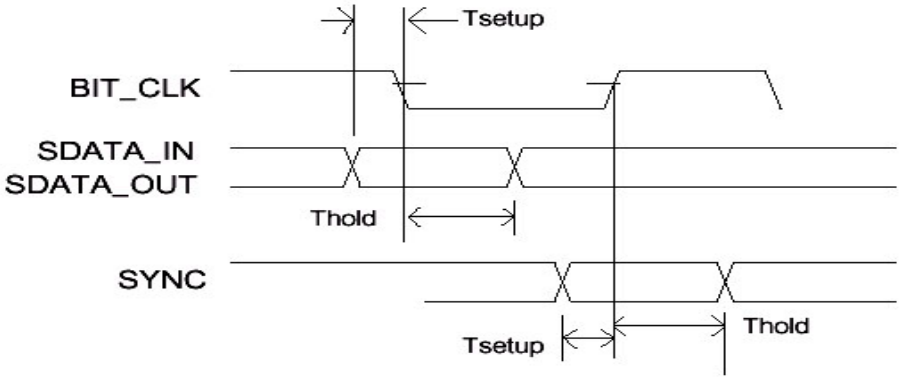


Table 12. Data Setup and Hold Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10.0	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10.0	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC '97 Controller.

7.5 SIGNAL RISING AND FALLING TIMES

(50pF external load; from 10% to 90% of Vdd)

Figure 12. Signal Rising and Falling Times Diagram

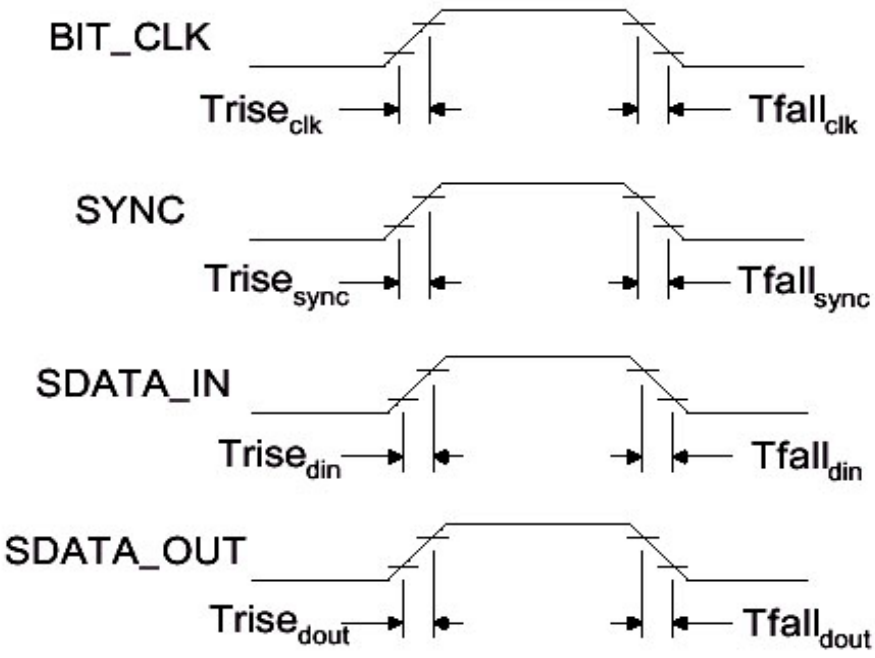


Table 13. Signal Rising and Falling time Parameters

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rising time	Triseclk	2	-	6	ns
BIT_CLK falling time	Tfallclk	2	-	6	ns
SYNC rising time	Trisesync	2	-	6	ns
SYNC falling time	Tfallsync	2	-	6	ns
SDATA_IN rising time	Trisedin	2	-	6	ns
SDATA_IN falling time	Tfalldin	2	-	6	ns
SDATA_OUT rising time	Trisedout	2	-	6	ns
SDATA_OUT falling time	Tfalldout	2	-	6	ns

7.6 AC-LINK LOW POWER MODE TIMING

Figure 13. AC-link Low Power Mode Timing Diagram

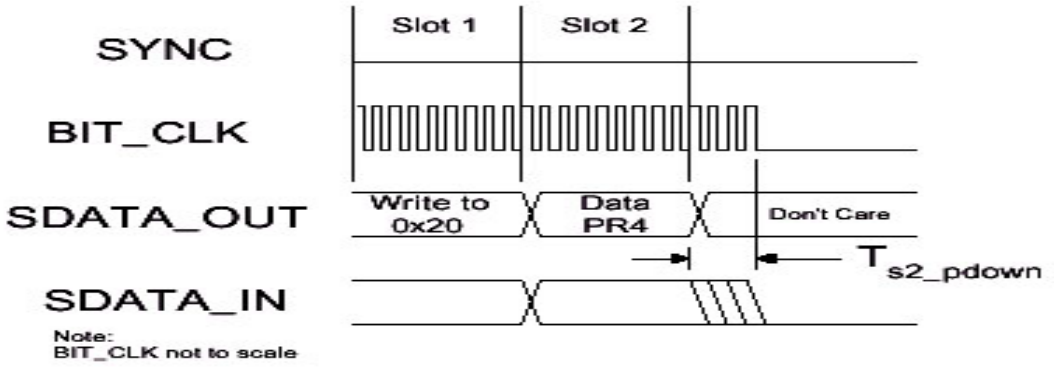


Table 14. AC-link Low Power Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

7.7 ATE TEST MODE

Figure 14. ATE Test Mode Timing Diagram

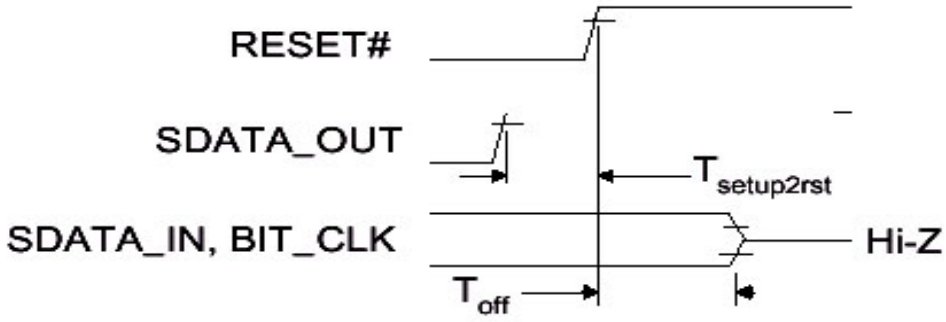


Table 15. ATE Test Mode Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Notes:

❶All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes the AC-Link outputs of CMI9739 to go high impedance which is suitable for ATE in circuit testing.

❷Once either of the two test modes has been entered, CMI9739 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.

# denotes active low.

8. RELEASE NOTE

v1.0/V1.1 Basic

v1.2 04/15/2002

1. Modify register description.
2. Modify pin description.

v1.3 05/23/2002

1. Correct pin difinition for CMI9739A codec.

9. REFERENCES

Intel, Audio Codec '97 Component Specification, Revision 2.2, September, 2000.

—End of Specifications—

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