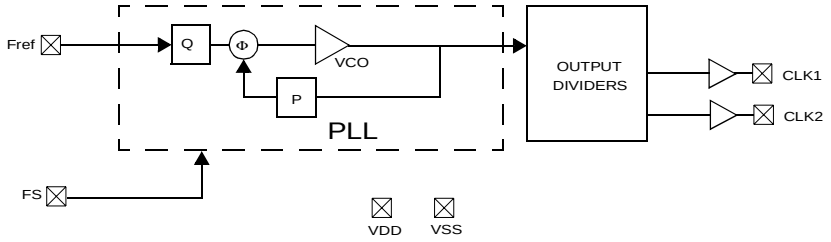
PacketClock™
T1/E1 Clock Generator

Features	Benefits
• **Integrated phase-locked loop**	High performance PLL tailored for T1/E1 clock generation
• **Low jitter, high accuracy outputs**	Meets critical timing requirements in complex system designs
• **3.3V Operation**	Enables application compatibility

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY26211	2	1.544 or 2.048 MHz	19.44 MHz, 77.76 MHz

Logic Block Diagram



Pin Configuration

CY26211
8-pin SOIC

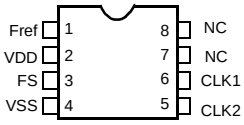


Table 1. CY26211 Frequency Select Option

Frequency Select	Fref	CLK1	CLK2	Unit
0	1.544	19.44	77.76	MHz
1	2.048	19.44	77.76	MHz

Pin Description

Name	Pin Number	Description
Fref	1	1.544-MHz/2.048-MHz Reference Input
VDD	2	Voltage Supply
FS	3	Frequency Select. Weak internal pull-up. See *Table 1* for a description of pin function.
VSS	4	Ground
CLK2	5	77.76-MHz Clock Output
CLK1	6	19.44-MHz Clock Output
NC	7	No Connect
NC	8	No Connect

Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[1]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electro-Static Discharge	2000		V

Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature (Commercial)	0		70	° C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	Reference Frequency	1.544		2.048	MHz

DC Electrical Specifications (Commercial)

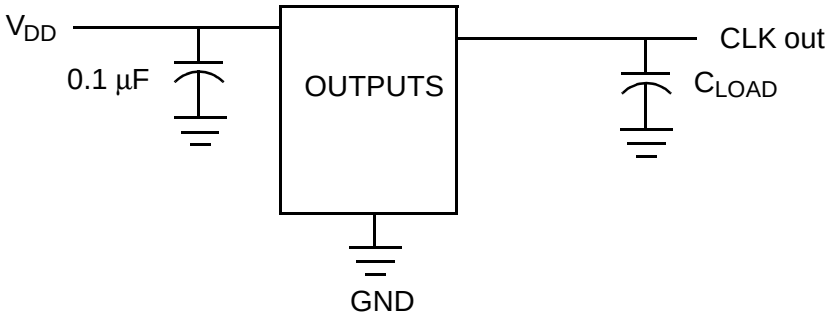
Parameter	Name	Description	Min	Typ	Max	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IH}	Input Low Current	$V_{IL} = 0V$			50	µA
I_{IL}	Input High Current	$V_{IH} = V_{DD}$			5	µA
I_{DD}	Supply Current	Sum of Core and Output Current			20	mA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	$0.7V_{DD}$			V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}			$0.3V_{DD}$	V
R_{UP}	Pull-up resistor	V_{DD}=3.14V to 3.47V, measured at $V_{IN} = 0V$		100	150	kΩ

AC Electrical Specifications (V_{DD} = 3.3V)

Parameter[2]	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
ERO	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15pF See *Figure 2*.	0.8	1.4		V/ns
EFO	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15pF See *Figure 2*.	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak Period Jitter		200		ps
t_{10}	PLL Lock Time				3	ms

Notes:
1. Rated for 10 years
2. Not 100% tested

Test and Measurement Set-up



Voltage and Timing Definitions

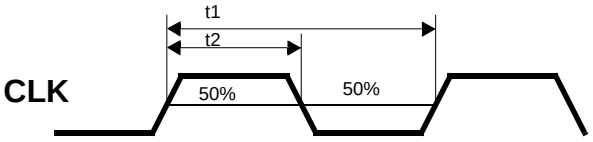


Figure 1. Duty Cycle Definition; DC = t2/t1

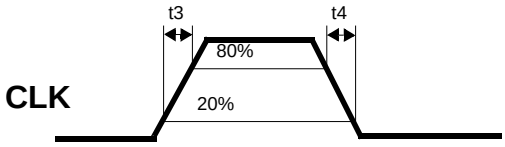


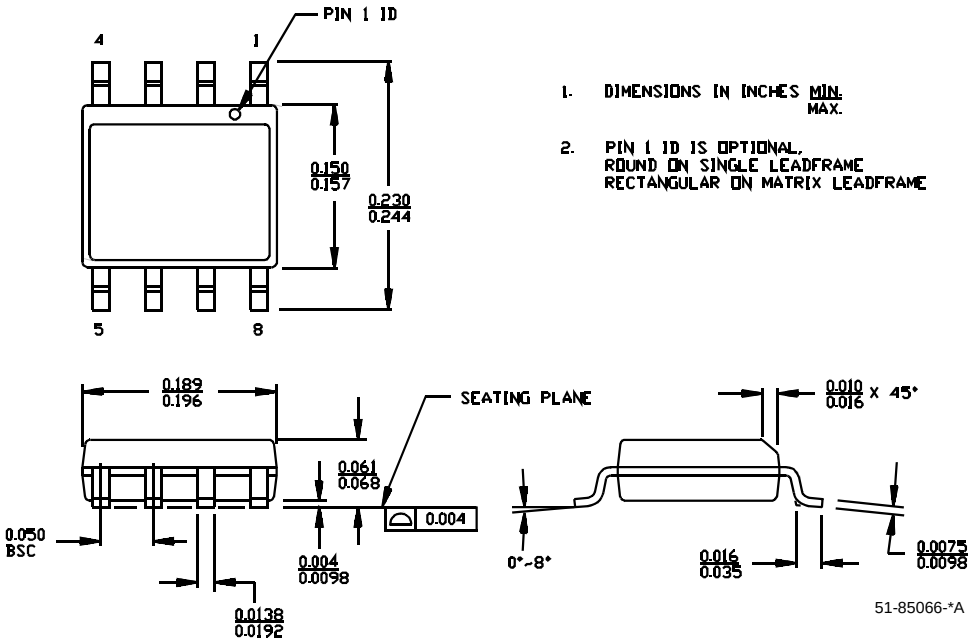
Figure 2. Rise and Fall Time Definitions: ER = 0.6 x V_{DD} / t3, EF = 0.6 x V_{DD} / t4

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY26211SC	S8	8-Pin SOIC	Commercial	3.3V
CY26211SCT	S8	8-Pin SOIC - Tape and Reel	Commercial	3.3V

Package Drawing and Dimensions

8-Lead (150-Mil) SOIC S8



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Document History Page

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**	121428	12/10/02	CKN	New data sheet