



CYPRESS

CY7C65100

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# CY7C65100

## Four-port Universal Serial Bus Fixed-function Hub Controller

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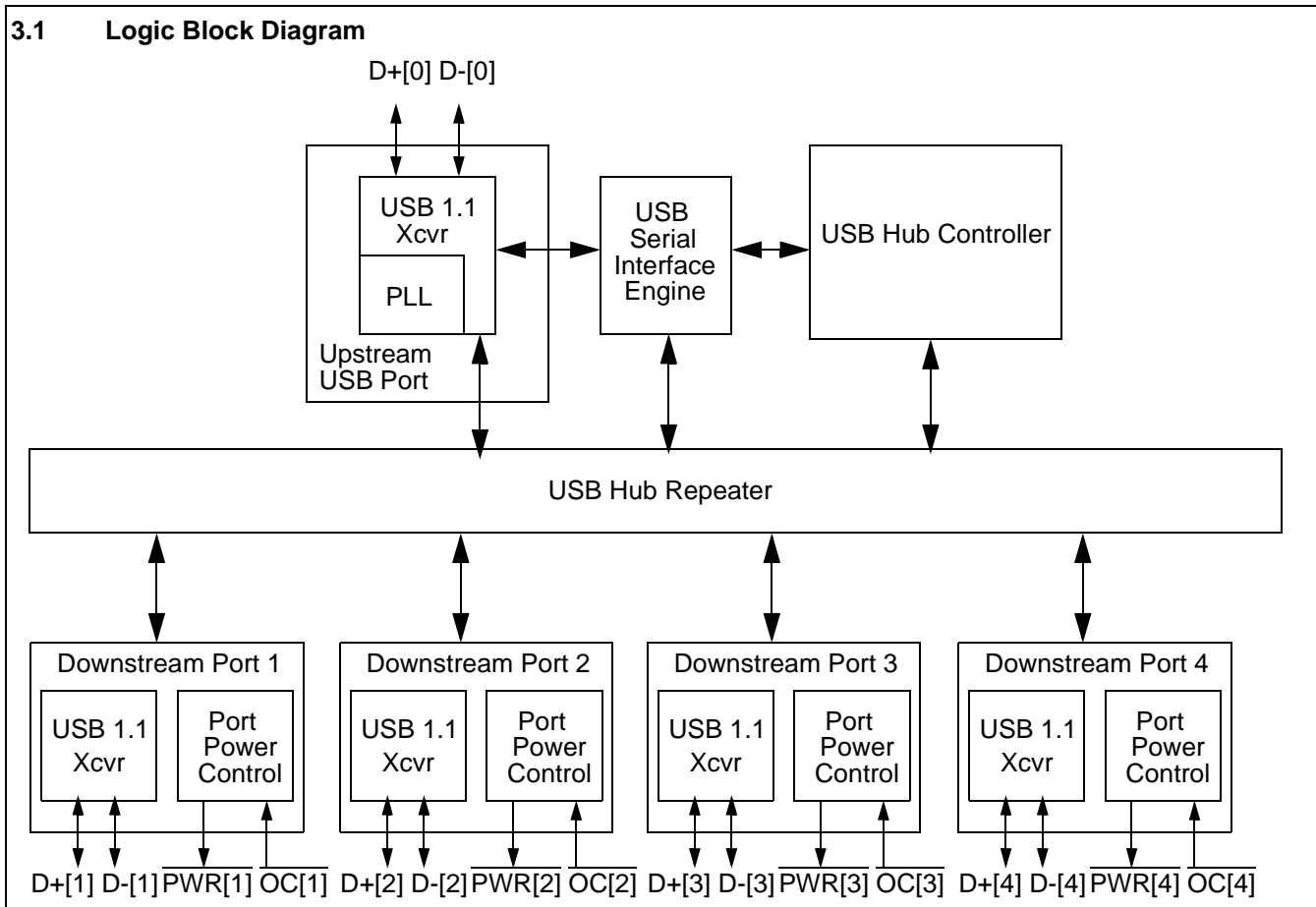
## 1.0 Features

- Fixed-function four-port USB hub devices with integrated hub repeater, hub controller, Serial Interface Engine (SIE), and USB transceivers
- USB Specification Compliance
  - Conforms to *USB Specification, Rev. 1.1*
  - Complies with the USB HUB Device Class
- Supports self-powered and bus-powered applications
- Individual downstream port power switching
- Individual downstream port overcurrent detection
- Integrated USB transceivers reduce EMI
- Internal 48-MHz phase-locked loop (PLL) reduces design cost by requiring only an external 6-MHz crystal
- Operating voltage from 4.0V–5.5V DC
- Operating temperature from 0°–70° Celsius
- Available in a space-saving 28-lead SOIC package

## 2.0 Functional Overview

The CY7C65100 series offers high-performance fixed-function Universal Serial Bus (USB) hub devices that comply with *USB Specification, Rev. 1.1*. Up to four downstream USB ports are available to expand the USB attachment points available in your PC system. These self-contained devices require no firmware development for your design, thereby reducing the design risk associated with some microcontroller solutions. These Application Specific Standard Products (ASSP) can improve time-to-market in a number of USB designs, including standalone hubs, motherboard hubs, and monitor hubs.

The CY7C65100 series supports self-powered or bus-powered applications. Power management for all downstream ports supports power-switching and overcurrent detection with individual port control. The four downstream ports support both full-speed (12-Mbps signaling rate) and low-speed (1.5-Mbps signaling rate) devices. The CY7C65100 series has a reduced frequency (6-MHz) crystal oscillator for lower system cost as well as improved EMI performance. The four-port CY7C65100 series is available in a cost-effective and space-saving 28-lead SOIC package.

**3.0 Product Summary**
**3.1 Logic Block Diagram**

**3.2 Pin Configuration**
**CY7C65100  
28-pin SOIC**

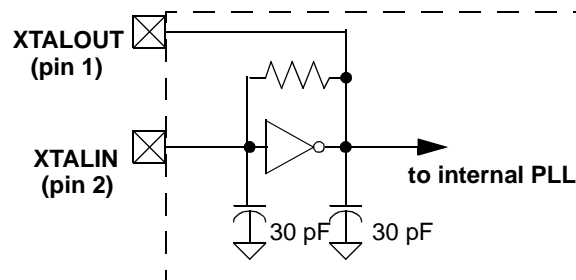
|                  |    |    |                 |
|------------------|----|----|-----------------|
| XTALOUT          | 1  | 28 | V <sub>CC</sub> |
| XTALIN           | 2  | 27 | PSTAT[3/4]      |
| V <sub>REF</sub> | 3  | 26 | PSTAT[1/2]      |
| GND              | 4  | 25 | PWR_SEL         |
| D+[0]            | 5  | 24 | D-[3]           |
| D-[0]            | 6  | 23 | D+[3]           |
| D+[1]            | 7  | 22 | D-[4]           |
| D-[1]            | 8  | 21 | D+[4]           |
| D+[2]            | 9  | 20 | GND             |
| D-[2]            | 10 | 19 | GND             |
| OC[4]            | 11 | 18 | PWR[1]          |
| OC[2]            | 12 | 17 | PWR[3]          |
| PWR[4]           | 13 | 16 | OC[1]           |
| PWR[2]           | 14 | 15 | OC[3]           |

### 3.3 Pin Assignments

**Table 3-1. Pin Assignments**

| Name   | I/O | Pin         | Description  |
|--|-----|-------------|--|
| D+[0], D-[0]   | I/O | 5,6         | Upstream port, USB differential data   |
| D+[1], D-[1]   | I/O | 7,8         | Downstream port 1, USB differential data   |
| D+[2], D-[2]   | I/O | 9,10        | Downstream port 2, USB differential data   |
| D+[3], D-[3]   | I/O | 23,24       | Downstream port 3, USB differential data   |
| D+[4], D-[4]   | I/O | 21,22       | Downstream port 4, USB differential data   |
| $\overline{\text{PWR}}[1]-\overline{\text{PWR}}[4]$          | OUT | 18,14,17,13 | Downstream port power enable output  |
| $\overline{\text{OC}}[1]-\overline{\text{OC}}[4]$            | IN  | 16,12,15,11 | Downstream port power over-current detection signals   |
| XTALIN   | IN  | 2           | 6-MHz crystal or external clock input  |
| XTALOUT  | OUT | 1           | 6-MHz crystal out  |
| V <sub>CC</sub>  | PWR | 28          | Voltage supply   |
| GND  | GND | 4,19,20     | Ground   |
| V <sub>REF</sub>   | IN  | 3           | Input for external 3.3V supply voltage for the upstream and downstream differential data output buffers and the D+ pull-up |
| PWR_SEL  | IN  | 25          | Bus or self-power function select input  |
| $\overline{\text{PSTAT}}[1/2], \overline{\text{PSTAT}}[3/4]$ | OUT | 26,27       | Downstream port LED status enable  |

### 4.0 Clocking


**Figure 4-1. Clock Oscillator On-chip Circuit**

XTALIN and XTALOUT are the clock pins to the CY7C65100 series. The user can connect either an external oscillator or a crystal to these pins. A 6-MHz fundamental crystal can be connected to these pins to provide a reference frequency for the internal PLL. When using an external crystal, keep PCB traces between the chip leads and crystal as short as possible (less than 2 cm). A ceramic resonator is not an adequate clock source to meet the timing specifications of a high-speed USB function and therefore cannot be used with these parts. An external 6-MHz clock can be applied to the XTALIN pin if the XTALOUT pin is left open. Please note that grounding the XTALOUT pin when driving XTALIN with an oscillator will not work as the internal clock is effectively shorted to ground.

### 5.0 USB Overview

The USB hardware includes a USB Hub repeater with one upstream port and up to four downstream ports. An external series resistor of  $R_{\text{ext}} = 20\Omega (\pm 5\%)$  must be placed in series with all upstream and downstream USB I/O in order to meet the USB driver impedance requirements as defined by the USB specification (see *Figure 6-1*).

#### 5.1 USB SIE

The SIE allows the CY7C65100 series to communicate with the USB host through the USB repeater portion of the hub. The SIE handles the following USB bus activity independently of the hub microcontroller:

- Bit stuffing/unstuffing
- Checksum generation/checking

- ACK/NAK/STALL
- TOKEN type identification
- Address checking.

The following protocol handling is done at a higher level by the Hub Control Block:

- Coordinate enumeration by responding to SETUP packets
- Fill and empty the FIFOs
- Suspend/Resume coordination
- Verify and select DATA toggle values
- Port power control and over-current detection.

## 5.2 Hub Design

The power switching and over-current detection of downstream ports is managed by control pins connected to an external power switch device (see *Figure 6-1*). The active-LOW  $\overline{\text{PWR}}[n]$  output pins of the CY7C65100 series are connected to the respective external power switch's port power enable signals. (Note that each port power output pin of the external power switch must be bypassed with an electrolytic or tantalum capacitor as required by the USB specification. These capacitors supply the inrush currents which occur during downstream device hot-attach events.) The active-LOW  $\overline{\text{OC}}[n]$  pins of the CY7C65100 series are connected to the respective external power switch's port over-current indication (output) signals. Upon detecting an over-current condition, the hub device reports the over-current condition to the host and disables (sets to logic HIGH) the respective  $\overline{\text{PWR}}[n]$  signal connected to the external power device.

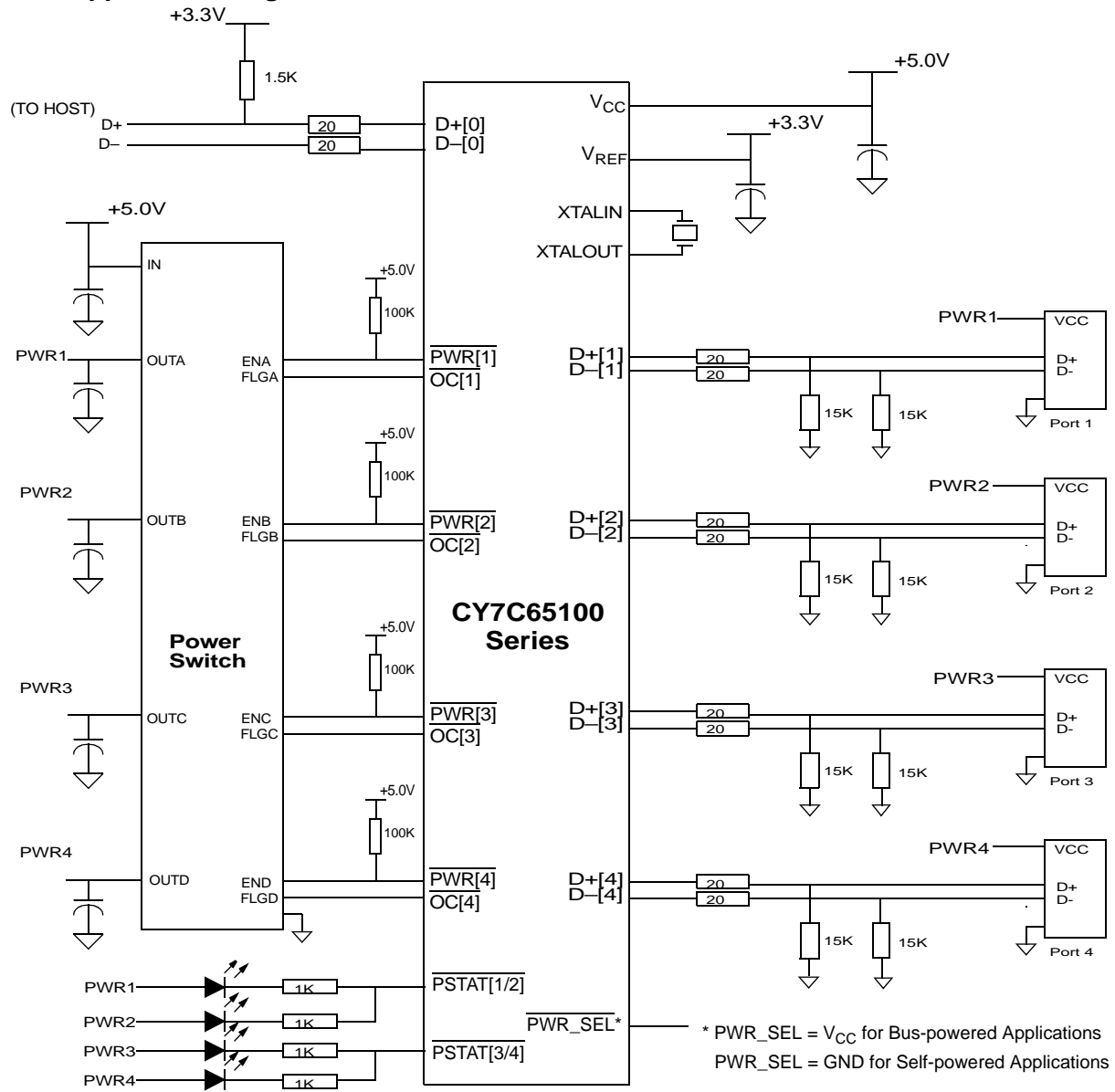
## 5.3 Vendor ID and Product ID

The CY7C65100 Series will enumerate with the default Vendor ID and Product ID as follows.

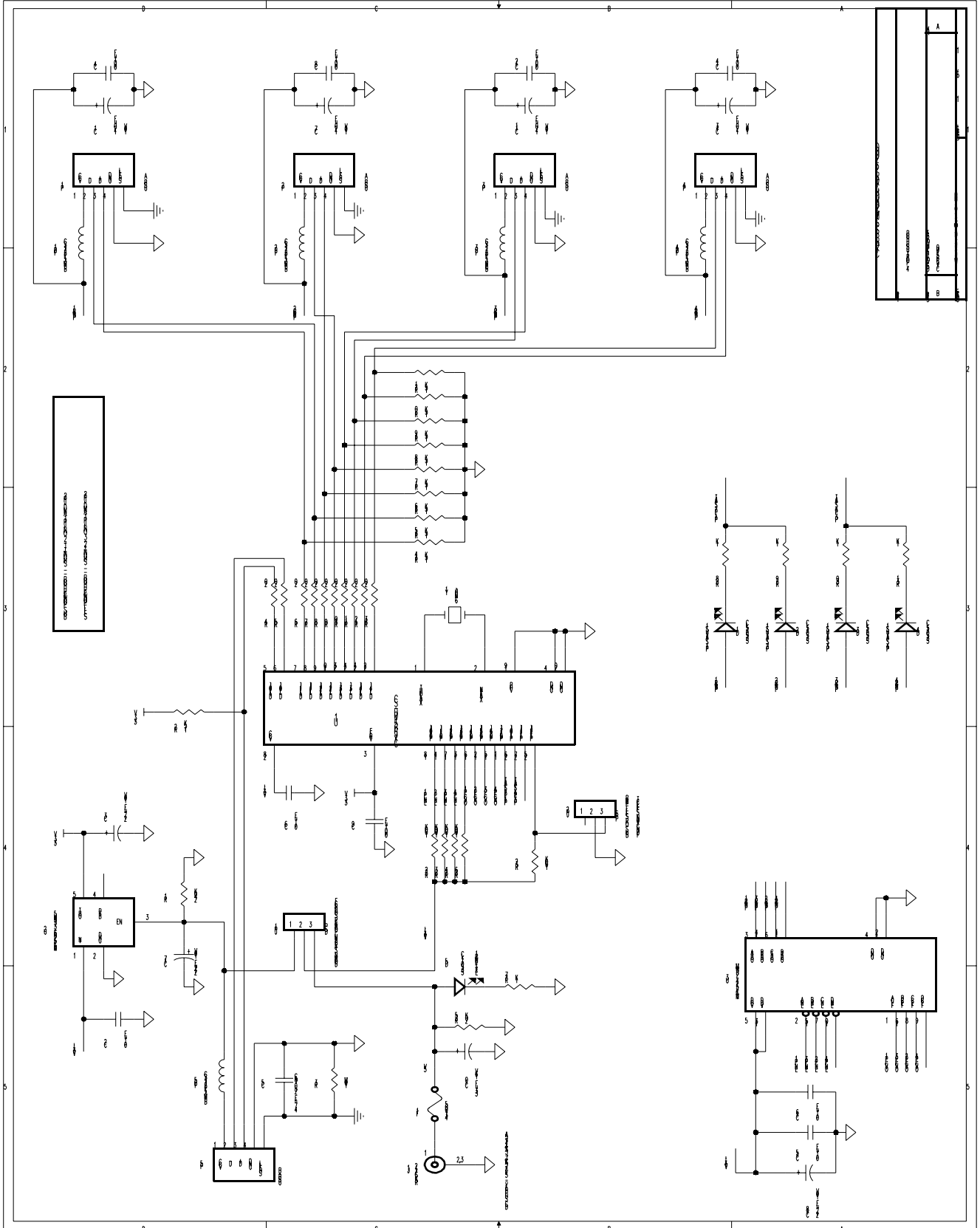
|            | <b>Bus-powered</b> | <b>Self-powered</b> |
|------------|--------------------|---------------------|
| Vendor ID  | 0x04b4             | 0x04b4              |
| Product ID | 0x5204             | 0x5203              |

Pin 25 (PWR\_SEL) is a strapping option that selects the device's power configuration report (PWR\_SEL = GND for self-powered, PWR\_SEL = Vcc for bus-powered).

For high-volume business, Cypress has the capability to factory-program a Custom Vendor ID and Product ID. Please contact your local Cypress sales office for more information.

**6.0 Application Diagrams**

**Figure 6-1. USB Standalone Hub Application Diagram**

6.1 USB Standalone Hub Schematics





## 7.0 Absolute Maximum Ratings

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -0°C to +70°C  
 Supply voltage on  $V_{CC}$  relative to  $V_{SS}$  ..... -0.5V to +7.0V  
 DC Input Voltage ..... -0.5V to  $+V_{CC} + 0.5V$   
 Power Dissipation ..... 500 mW  
 Static Discharge Voltage ..... > 2000V  
 Latch-up Current ..... > 200 mA  
 Max Output Sink Current into  $\overline{PWR[n]}$  Pins  
 ( $V_{out} = 2.0V$ ) ..... 60 mA

## 8.0 Electrical Characteristics $F_{OSC} = 6\text{ MHz}$ ; Operating Temperature = 0° to 70°C, $V_{CC} = 4.0V$ to 5.5V

| Parameter                                  | Description                                     | Conditions  | Min.  | Max.  | Unit    |
|--|---|---|-------|-------|---------|
| <b>General</b>                             |   |   |       |       |         |
| $V_{ref}$                                  | Reference Voltage                               | $3.3V \pm 5\%$  | 3.15  | 3.45  | V       |
| $I_{CC}$                                   | $V_{CC}$ Operating Current                      |   |       | 50    | mA      |
| $I_{REF}$                                  | $V_{ref}$ Operating Current                     | No USB Traffic  |       | 10    | mA      |
| $I_{SB1}$                                  | Standby Current                                 |   |       | 50    | $\mu A$ |
| $I_{IL}$                                   | Input Leakage Current                           | any pin   |       | 1     | $\mu A$ |
| <b>USB Interface</b>                       |   |   |       |       |         |
| $V_{di}$                                   | Differential Input Sensitivity                  | $ (D+) - (D-) $   | 0.2   |       | V       |
| $V_{cm}$                                   | Differential Input Common Mode Range            |   | 0.8   | 2.5   | V       |
| $V_{se}$                                   | Single Ended Receiver Threshold                 |   | 0.8   | 2.0   | V       |
| $C_{in}$                                   | Transceiver Capacitance                         |   |       | 20    | pF      |
| $I_{io}$                                   | High-Z State Data Line Leakage                  | $0V < V_{in} < 3.3V$  | -10   | 10    | $\mu A$ |
| $R_{D+}$                                   | USB Power Setting Pull-up Resistor              |   | 1.425 | 1.575 | KW      |
| $R_{ext1}$                                 | External USB Pull-down Resistor                 | Downstream data lines                                       | 14.25 | 15.75 | KW      |
| $R_{ext2}$                                 | External USB Series Resistor                    | In series with each USB pin                                 | 19    | 21    | W       |
| <b>Power-On Reset</b>                      |   |   |       |       |         |
| $t_{vccs}$                                 | $V_{CC}$ Ramp Rate                              | Linear ramp: $V_{CC}=0$ to Operating Voltage <sup>[1]</sup> | 0     | 100   | ms      |
| <b>USB Upstream/Downstream Port</b>        |   |   |       |       |         |
| $V_{oh}$                                   | Static Output HIGH                              | RL of $15\text{ k}\Omega \pm 5\%$ to Gnd                    | 2.8   | 3.6   | V       |
| $V_{ol}$                                   | Static Output LOW                               | RL of $1.5\text{ k}\Omega \pm 5\%$ to 3.6V                  |       | 0.3   | V       |
| $V_{crs}$                                  | Crossover Voltage                               |   | 1.3   | 2.0   | V       |
| $Z_o$                                      | USB Driver Output Impedance                     | Including $R_{ext}$   | 28    | 44    | W       |
| <b>OC[n] Pins</b>                          |   |   |       |       |         |
| $V_{IL}$                                   | Input LOW Threshold Voltage                     |   |       | 0.8   | V       |
| $V_{IH}$                                   | Input HIGH Threshold Voltage                    |   | 2.0   |       | V       |
| <b><math>\overline{PWR[n]}</math> Pins</b> |   |   |       |       |         |
| $I_{\overline{PWR[n]}}$                    | $\overline{PWR[n]}$ Sink Current (typical 7 mA) | $V_{out} = 2.0V$ DC   | 3.5   | 10.6  | mA      |

**Note:**

1. Power-on Reset will occur whenever the voltage on  $V_{CC}$  is below approximately 2.5V.

| Parameter                | Description                            | Min.           | Max.   | Unit |
|--------------------------|--|----------------|--------|------|
| Clock Source             |  |                |        |      |
| $f_{OSC}$                | Clock Rate                             | 5.985          | 6.015  | MHz  |
| $t_{CYC}$                | Clock Period                           | 166.25         | 167.08 | nsec |
| $t_{CH}$                 | Clock HIGH Time                        | $0.45 t_{CYC}$ |        | ns   |
| $t_{CL}$                 | Clock LOW Time                         | $0.45 t_{CYC}$ |        | ns   |
| USB Full-speed Signaling |  |                |        |      |
| $t_r$                    | Transition Rise Time                   | 4              | 20     | ns   |
| $t_f$                    | Transition Fall Time                   | 4              | 20     | ns   |
| $t_{rfm}$                | Rise/Fall Time Matching; ( $t_r/t_f$ ) | 90             | 110    | %    |
| $t_{drate}$              | Full-speed Data Rate                   | 11.97          | 12.03  | Mb/s |
| USB Low-speed Signaling  |  |                |        |      |
| $t_r$                    | Transition Rise Time                   | 75             | 300    | ns   |
| $t_f$                    | Transition Fall Time                   | 75             | 300    | ns   |
| $t_{rfm}$                | Rise/Fall Time Matching; ( $t_r/t_f$ ) | 80             | 120    | %    |
| $t_{drate}$              | Low-speed Data Rate                    | 1.4775         | 1.5225 | Mb/s |

## 9.0 Switching Characteristics

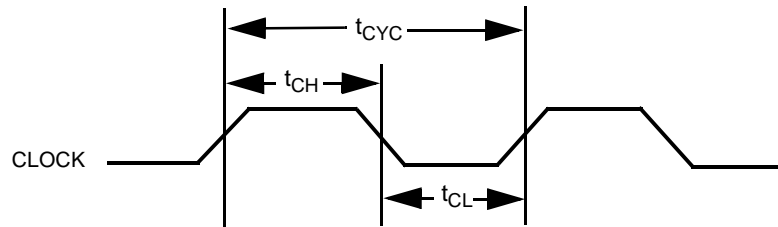


Figure 9-1. Clock Timing

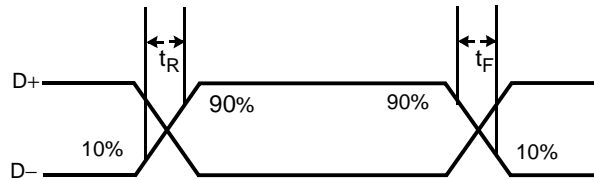


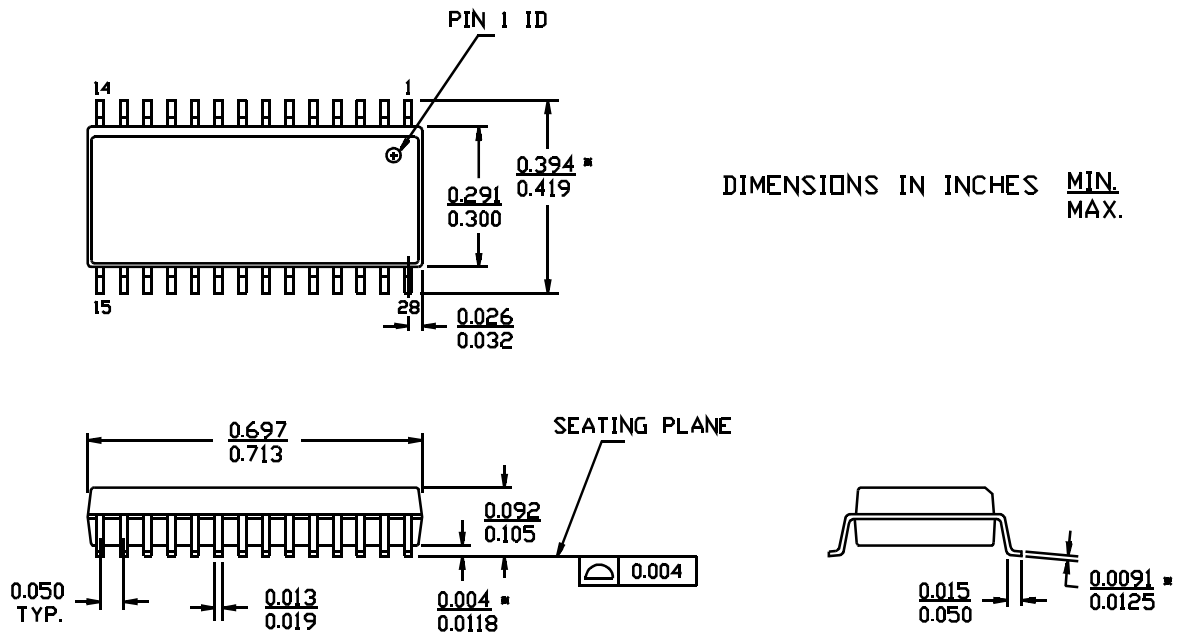
Figure 9-2. USB Data Signal Timing

## 10.0 Ordering Information

| Ordering Code | Package Name | Description | Operating Range |
|---------------|--------------|-------------|-----------------|
| CY7C65100-SC  | S21          | 28-pin SOIC | Commercial      |

11.0 Package Diagram

28-lead (300-mil) Molded SOIC S21



51-85026-A

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| <b>Document Title: CY7C65100 Four-port Universal Serial Bus Fixed-function Hub Controller</b><br><b>Document Number: 38-08021</b> |                |                   |                        |                              |
|---|----------------|-------------------|------------------------|------------------------------|
| <b>REV.</b>   | <b>ECN NO.</b> | <b>Issue Date</b> | <b>Orig. of Change</b> | <b>Description of Change</b> |
| **  | 113849         | 06/25/02          | BON                    | New Data Sheet               |