CY7C960
CY7C961

Low Cost VMEbus Interface Controller Family

Features

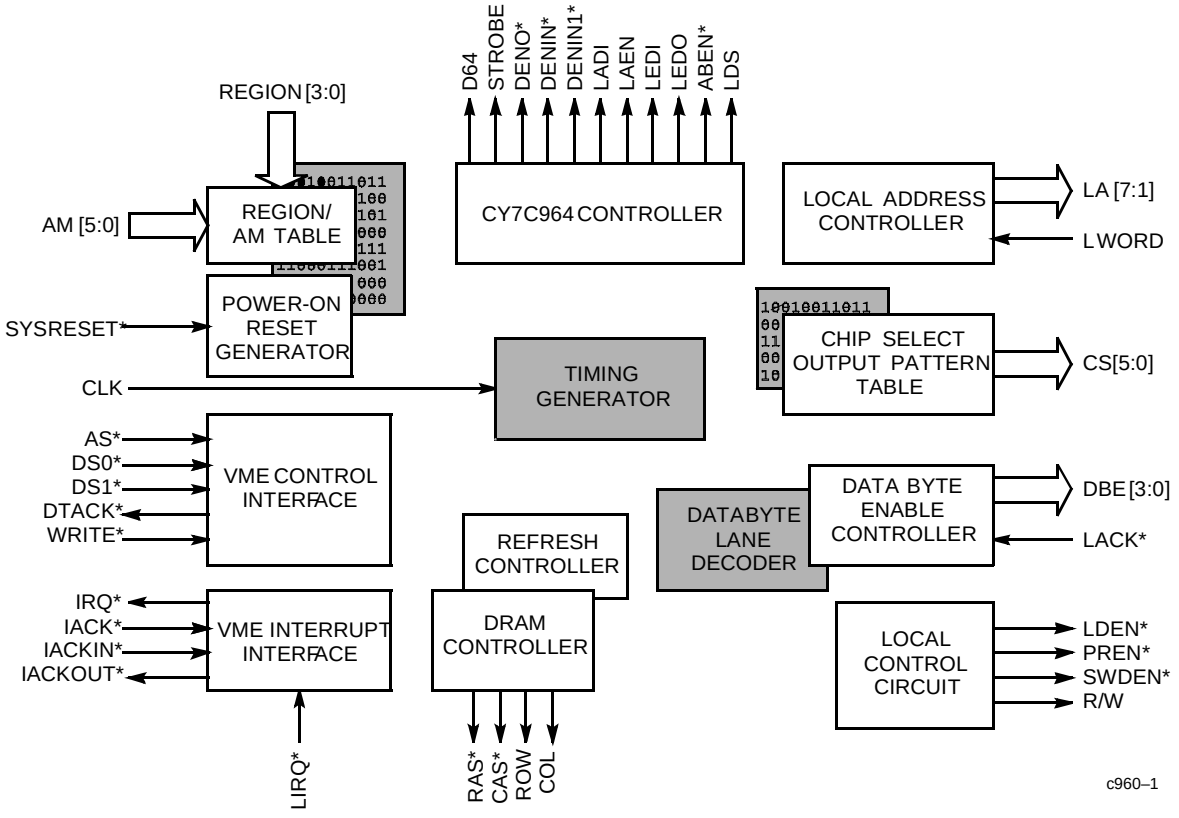
- **80-Mbyte-per-second block transfer rates**
- **All VME64 transactions provided, including A64/D64, A40/MD32 transfers**
- **Auto Slot ID**
- **CR/CSR space**
- **All standard (Rev C) VMEbus transactions implemented**
- **VMEbus Interrupter**
- **No local CPU required**
- **Programmable from VMEbus, serial PROM, or local bus**
- **DRAM controller, including refresh**
- **On-chip DMA controller**
- **Local I/O controller**
- **Flexible VMEbus address scheme**
- **User-configured VMEbus response**
- **64-pin TQFP, 10x10mm (CY7C960)**
- **100-pin TQFP, 14x14mm (CY7C961)**

Functional Description

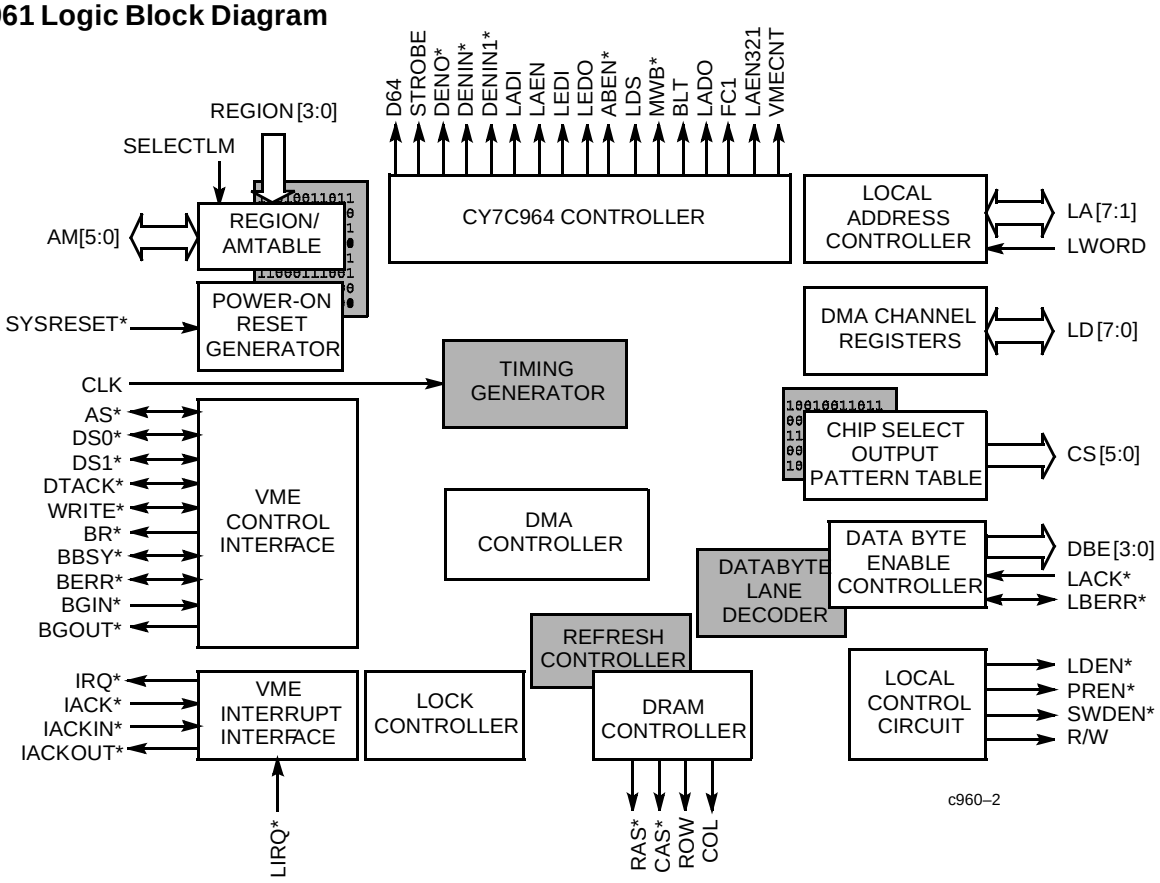
The CY7C960 Slave VMEbus Interface Controller provides the board designer with an integrated, full-featured VME64 interface. This 64-pin device can be programmed to handle every transaction defined in the VME64 specification. The CY7C961 is based upon the CY7C960: additional features include Remote Master capability whereby the CY7C961 can be commanded to move data as a VMEbus master. The CY7C961 is packaged in a 100-pin outline.

The CY7C960 contains all the circuitry needed to control large DRAM arrays and local I/O circuitry without the intervention of a local CPU. There are no registers to read or write, no complex command blocks to be constructed in memory. The CY7C960 simply fetches its own configuration parameters during the power-on reset period. After reset the CY7C960 responds appropriately to VMEbus activity and controls local circuitry transparently.

CY7C960 Logic Block Diagram

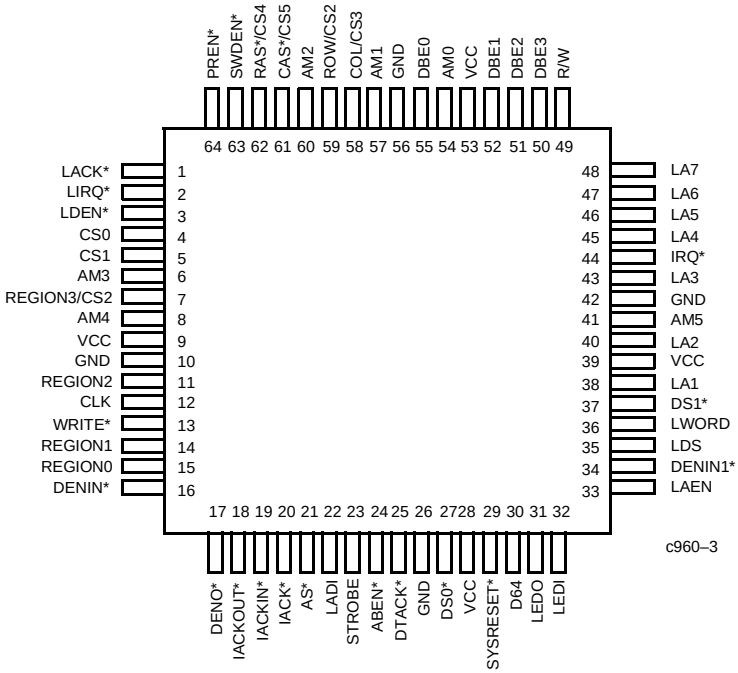


CY7C961 Logic Block Diagram



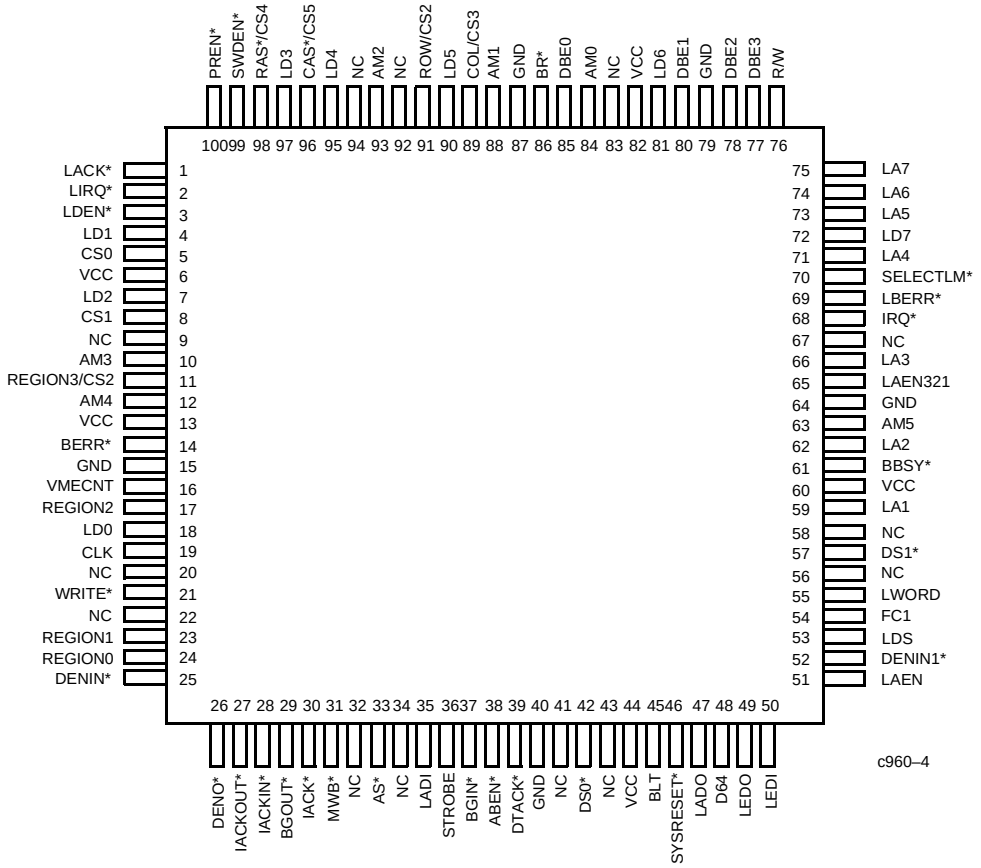
CY7C960 Pin Configuration

TQFP
Top View



CY7C961 Pin Configuration

TQFP
Top View



c960–4

Functional Description (continued)

The CY7C960 controls a bridge between the VMEbus and local DRAM and I/O. Once programmed, the CY7C960 provides activities such as DRAM refresh and local I/O handshaking in a manner that requires no additional local circuitry. The VMEbus control signals are connected directly to the CY7C960. The VMEbus address and data signals are connected to companion address/data transceivers which are controlled by the CY7C960. The CY7C964 VMEbus Interface Logic Circuit is an ideal companion device: the CY7C964 provides a slice of data and address logic that has been optimized for VME64 transactions. In addition to providing the specified drive strength and timing for VME64 transactions, the CY7C964 contains all the circuitry needed to multiplex the address/data bus for multiplexed VMEbus transactions. It contains counters and latches needed during BLT operations; and it also contains address comparators which can be used in the board's Slave Address Decoder. For a 6U or 9U application, four CY7C964 devices are controlled by a single CY7C960. For 3U applications, the CY7C960 controls two CY7C964 devices and an address latch.

The design of the CY7C960 makes it unnecessary to know the details of the VMEbus transaction timing and protocol. The complex VMEbus activities are translated by CY7C960 to simple local cycles involving a few familiar control signals. Similarly, it is not necessary to understand the operation of the companion device, CY7C964: all control sequences for the part are generated automatically by the CY7C960 in response to VMEbus or local activity. If more information is desired, consult the CY7C964 chapter in the *VIC64 Design Notes* (available separately).

VMEbus transactions supported by the CY7C960 include D8, D16, D32 (incl. UAT), MD32, D64, A16, A24, A32, A40, A64 single-cycle and block-transfer reads and writes, Read-Modify-Write cycles (incl. multiplexed), and Address-only (with or without Handshake). The CY7C960 functions as a VMEbus Interrupter, and supports the new Auto Slot ID standard and CR/CSR space. The CY7C960 also handles LOCK cycles, although full LOCK support is not possible within the constraints of the CY7C960 pinout. Full LOCK support is provided by the CY7C961.

On the local side, no CPU is needed to program the CY7C960, nor to manage transactions. All programmable parameters are initialized through the use of either the VMEbus, a serial PROM, or some other local circuit. As the CY7C960 incorporates a reliable power-on reset circuit, parameters are self-loaded by the device at power-up or after a system reset. If the VMEbus is used to provide parameters, a VMEbus Master provides the programming information using a protocol, described in the User's Guide, which is compliant with the Auto Slot ID protocol from the new VME64 specification.

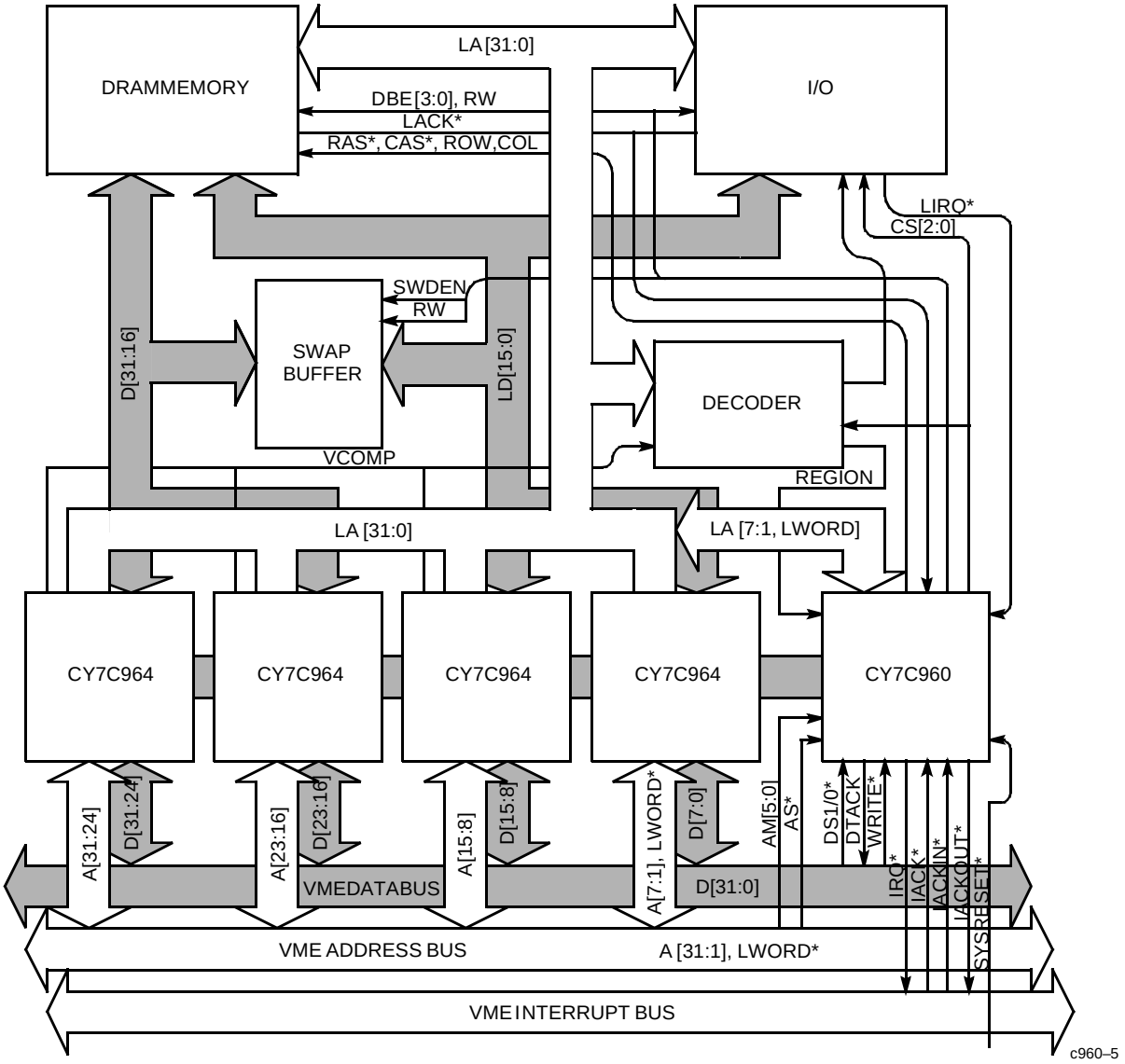
To assist in generating the configuration file, a Windows™-based program is available which guides the user through the process of selecting appropriate options. Contact your Sales Office for further details.

The CY7C961 is a true superset of the CY7C960. Signal pins have been added to control CY7C964 DMA functions. Existing VMEbus input pins have been changed to bidirectional and augmented to complete a master interface. A data port and chip select signal (SELECTLM*) complete the pin additions. As a VMEbus Slave, the CY7C961 behaves in every respect like the CY7C960. It simply has more pins, a master block transfer facility, and (because of the addition of the BBSY* connection) full lock cycle support.

From a system perspective, the CY7C961 master block transfer capability can be viewed as a DMA channel that resides on the slave card, but is controlled over the VMEbus by one or more VMEbus masters or programmed from the local bus.

The CY7C961 master block facility provides “block transfer on demand” capability for slave cards built around the Cypress CY7C961/CY7C964 chipset. This facility allows one or many VMEbus masters to write short series of commands to the slave card, telling it how much data to move, where to get it from, where to put it, and what transfer protocol to use while moving it. Blocks can be moved over the VMEbus as indivisible single cycles or BLTs. The protocol menu includes D8, D16, D32, MD32, or D64. A16, A24, A32, A40, and A64 address spaces can be specified. Burst lengths from 16 bytes to 8 megabytes can be requested. Eight registers accessible from the VMEbus make the facility simple to configure and simple to control. The facility has a busy semaphore, a VMEbus Interrupt on completion feature with a programmable Status/ID byte, and a built in requester and bus grant daisychain.

System Diagram Using the CY7C960



DC Specifications - VMEbus Signals AS*, DS1*, DS0*, DTACK*, BBSY

Parameter	Description	Test Conditions	Comm.	Industrial	Military	Units
V_{IH}	Minimum High-Level Input Voltage		2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage		0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{CC} = Min., I_{OH} =	2.4 –16 mA	2.4 –10 mA	2.4 –9 mA	V
V_{OL}	Maximum Low-Level Output Voltage	V_{CC} = Min., I_{OL} =	0.6 64 mA	0.6 60 mA	0.6 52 mA	V
I_L	Maximum Input Leakage Current	V_{CC} = Max., GND < V_{IN} < V_{CC}	±5	±5	±5	µA
V_{IK}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA	–1.2	–1.2	–1.2	V
I_{OZ}	Maximum Output Leakage Current	V_{CC} = Max. GND ≤ V_{OUT} ≤ V_{CC} Outputs Disabled	±10	±10	±10	µA

DC Specifications - VMEbus Signals AM5, AM4, AM3, AM2, AM1, AM0, IRQ*, BERR*, Write, BR[1]

Parameter	Description	Test Conditions	Comm.	Industrial	Military	Units
V_{IH}	Maximum High-Level Input Voltage		2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage		0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{CC} = Min., I_{OH} =	2.4 –16 mA	2.4 –10 mA	2.4 –9 mA	V
V_{OL}	Minimum Low-Level Output Voltage	V_{CC} = Min., I_{OL} =	0.6 48 mA	0.6 44 mA	0.6 38 mA	V
I_L	Maximum Input Leakage Current	V_{CC} = Max., GND < V_{IN} < V_{CC}	±5	±5	±5	µA
V_{IK}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA	–1.2	–1.2	–1.2	V
I_{OZ}	Maximum Output Leakage Current	V_{CC} = Max. GND < V_{OUT} < V_{CC} Outputs Disabled	±5	±5	±10	µA

DC Specifications - All Other Output Signals[2]

Parameter	Description	Test Conditions	Comm.	Industrial	Military	Units
V_{IH}	Maximum High-Level Input Voltage		2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage		0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{CC} = Min., I_{OH} =	2.4 –16 mA	2.4 –10 mA	2.4 –9 mA	V
V_{OL}	Minimum Low-Level Output Voltage	V_{CC} = Min., I_{OL} =	0.6 20 mA	0.6 18 mA	0.6 16 mA	V
I_L	Maximum Input Leakage Current	V_{CC} = Max., GND < V_{IN} < VCC	±5	±5	±5	µA
V_{IK}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA	–1.2	–1.2	–1.2	V
I_{OZ}	Maximum Output Leakage Current	V_{CC} = Max. GND < V_{OUT} < V_{CC} Outputs Disabled	±5	±5	±10	µA

Notes:
1. The BERR* signal has an on-chip pull-up resistor. For this signal the I_{OZ} value is modified by Pullup/Pulldown Current.
2. Some signals have an on-chip pull-up or pull-down resistors. For these signals I_{OZ} value is modified.

Capacitance - All Signals

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	15	pF
C_{OUT}	Output Capacitance		15	pF

Pullup/Pulldown Current - All Signals

Parameters	Description	Test Conditions	Typ.	Max.
I_{PU}	Input Pullup Current	T_A = –55°C, V_{CC} = 5.5V V_{IN} = GND	100 µA	250 µA
I_{PU}	Input Pullup Current	T_A = –55°C, V_{CC} = 5.5V V_{IN} = V_{CC}	100 µA	250 µA

Operating Current (CY7C960/CY7C961)

Parameters	Description	Test Conditions	Max.	Units
I_{DD}	Maximum Operating Current	No external DC load	100	mA

Related Documents

VMEBus Interface Handbook

Ordering Information

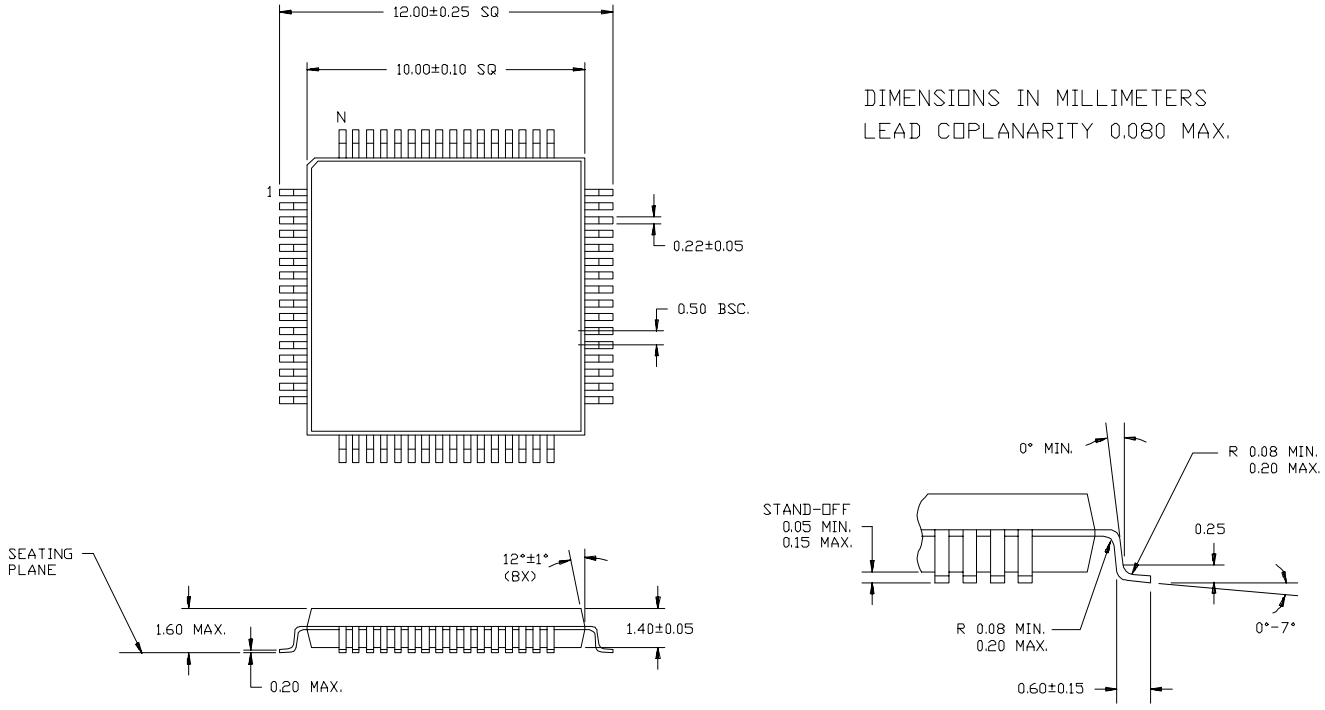
Ordering Code	Package Name	Package Type	Operating Range
CY7C960-ASC	A64	10x10 mm body 64-Lead Plastic Thin Quad Flatpack	Commercial
CY7C960-NC	N65	14x14 mm body 64-Lead Plastic Thin Quad Flatpack	
CY7C960-UM	U65	14x14 mm body 64 lead Ceramic Quad Flatpack	Military
CY7C960-UMB	U65	14x14 mm body 64 lead Ceramic Quad Flatpack	

Ordering Code	Package Name	Package Type	Operating Range
CY7C961-NC	A100	14x14 mm body 100-Lead Plastic Thin Quad Flatpack	Commercial

Document #: 38-00250-D

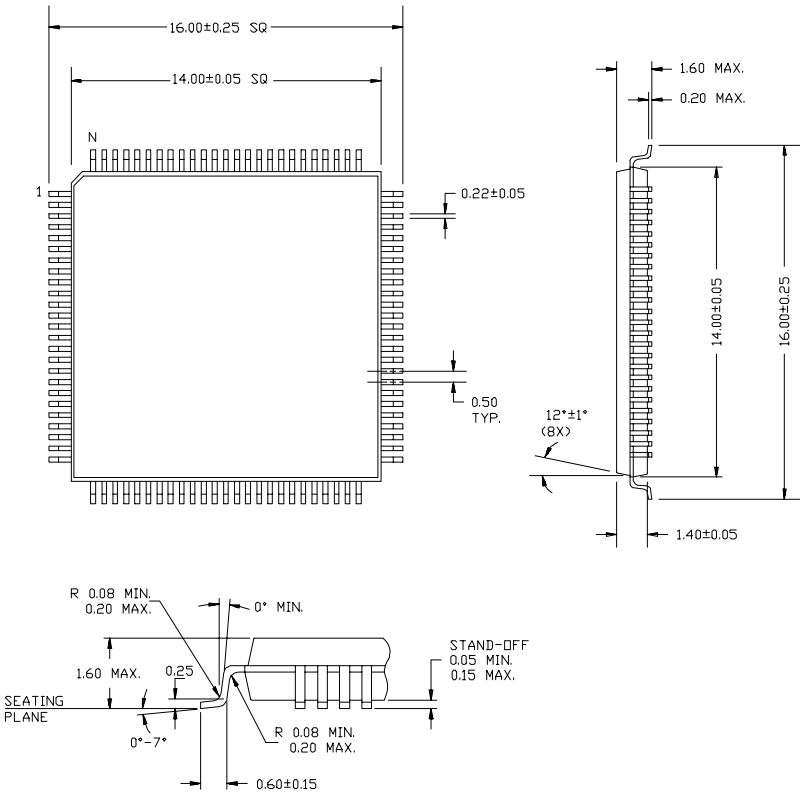
Package Diagrams

64-Pin Thin Quad Flatpack A64



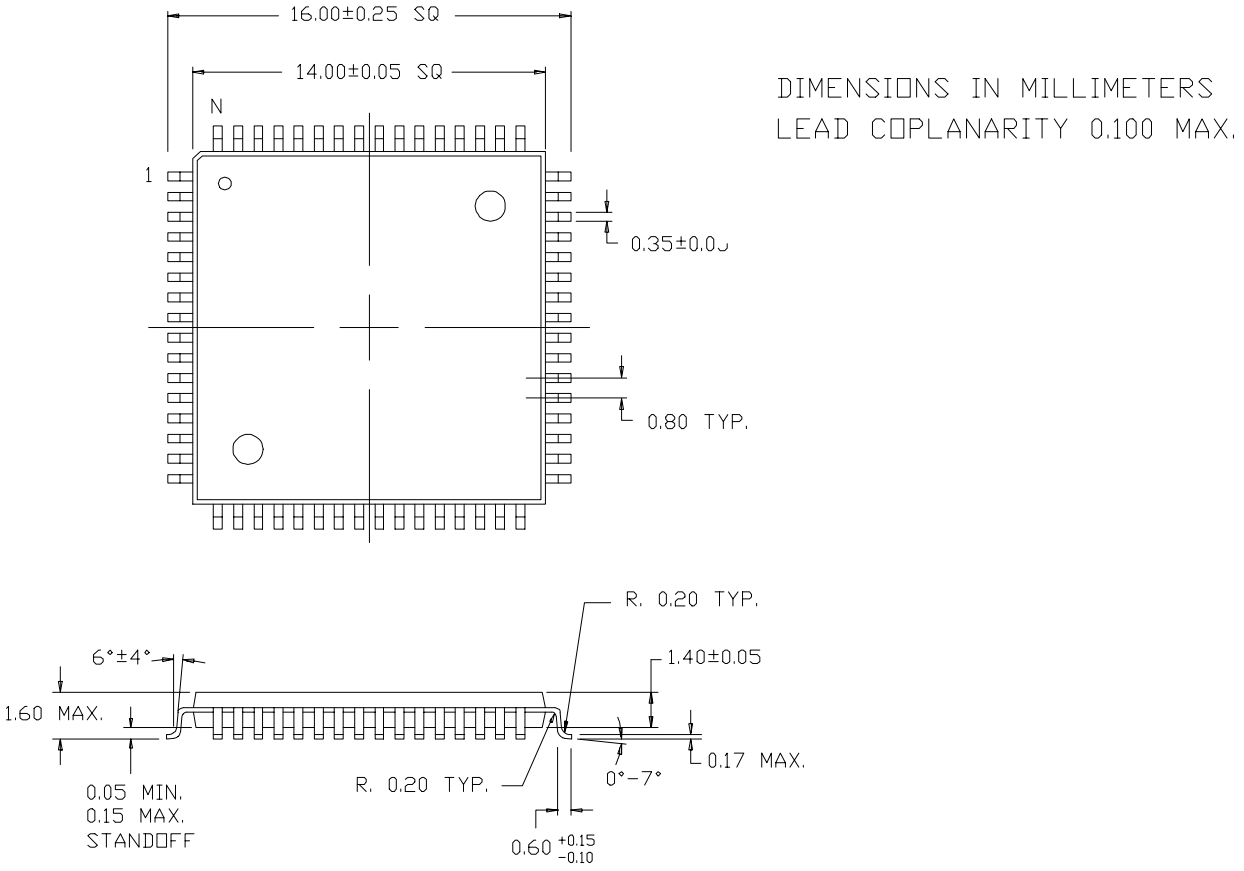
Package Diagrams (continued)

100-Pin Thin Quad Flatpack A100



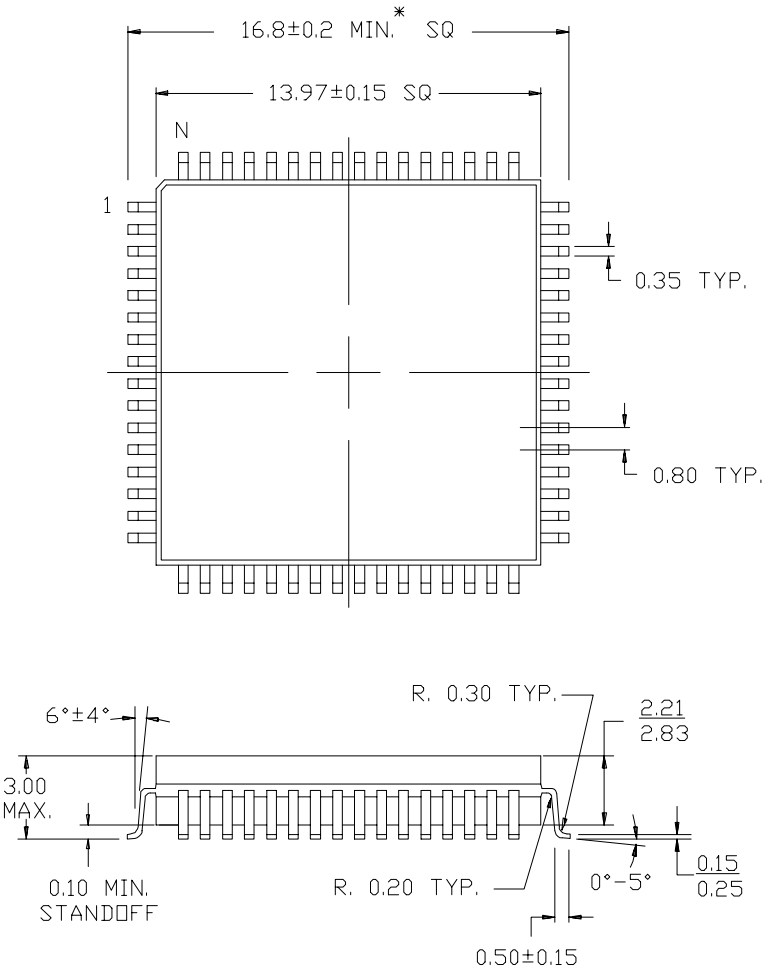
Package Diagrams (continued)

64-Lead Plastic Thin Quad Flatpack N65



Package Diagrams (continued)

64-Lead Ceramic Quad Flatpack (Cavity Up) U65



DIMENSIONS IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.

DIMENSION	MIN. / MAX.