# STAR250
## Radiation HardCMOS image sensor

Datasheets

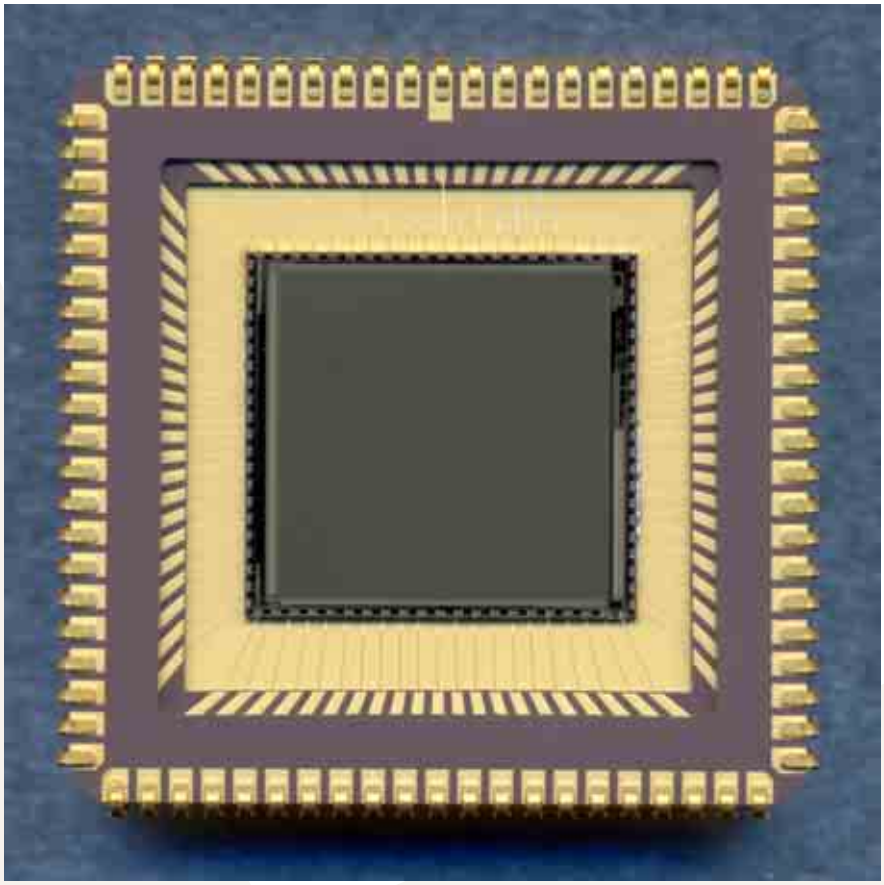


**Table of contents**

***Purpose***
*This document is the data sheet of a Radiation-Hard CMOS active pixel. The specifications are based upon the results of the electro-optical measurements.*

# 1 Image Sensor Description

The STAR250-sensor is a CMOS Active Pixel Sensor that is designed for application in Optical Inter-Satellite Link beam trackers. Apart from this, the design also envisaged a broader range of applications in space-borne systems like sun sensing and star tracking.

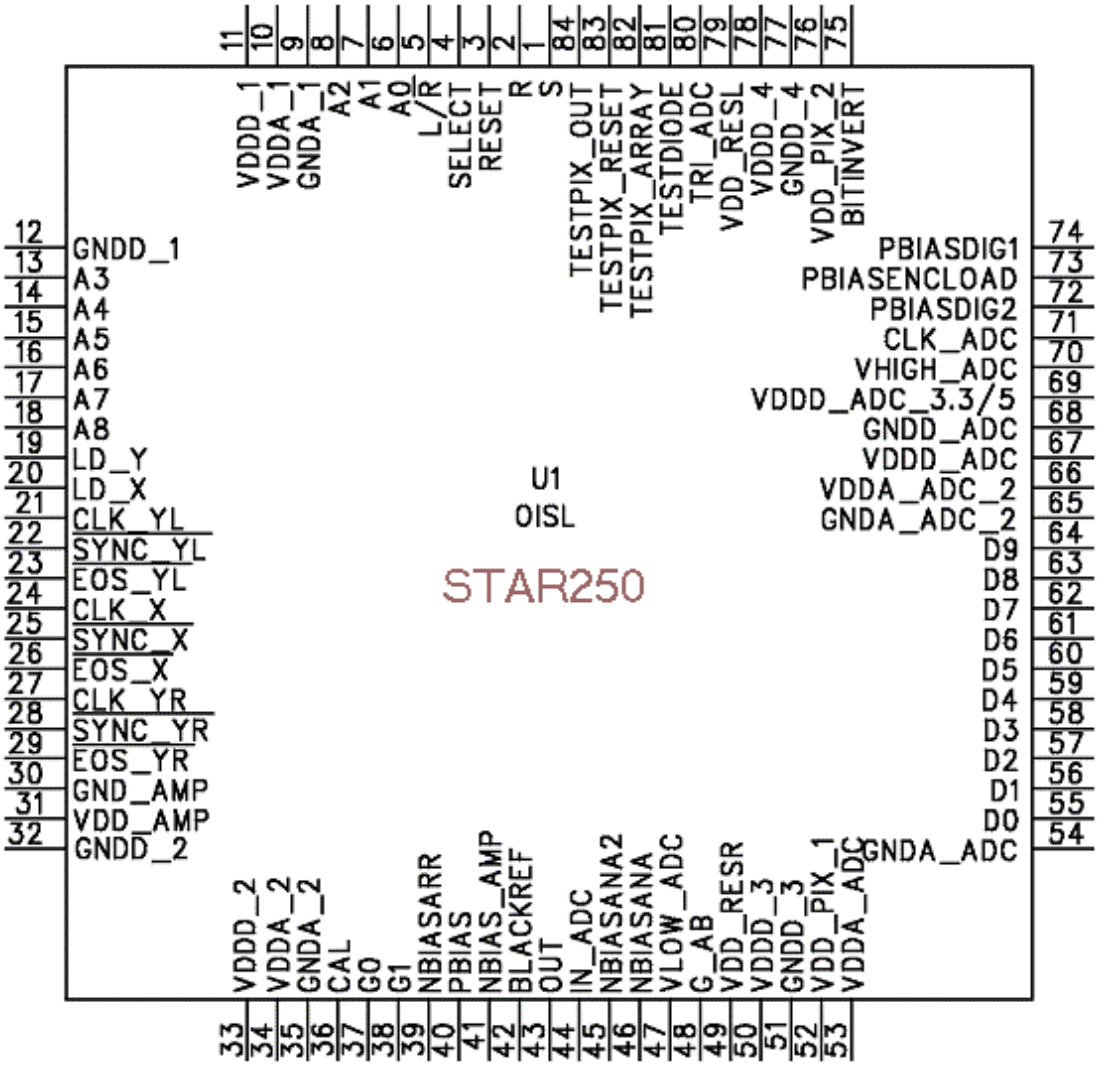
The sensor has an outstanding radiation tolerance that has been obtained by using proprietary technology modifications and design techniques.

## 1.1 Features

The STAR250 sensor has the following characteristics:

- Integrating 3-transistor Active Pixel Sensor
- 0.5 μm CMOS technology
- 512 by 512 pixels on 25 μm pitch
- 4 diodes per pixel for improved MTF and PRNU
- Radiation tolerant design
- On-chip double sampling circuit to cancel Fixed Pattern Noise
- Electronic shutter
- Readout rate: up to 30 full frames per second
- ROI windowing through pre-settable start point of read-out
- On-chip 10-bit ADC
- Ceramic JLCC-84 package

## 1.2 Electrical symbol



## 1.3 Pin configuration

**Table 1: STAR250 sensor pin configuration**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|
| **1** | S | **22** | SYNC_YL | **43** | OUT | **64** | D9 |
| **2** | R | **23** | EOS_YL | **44** | IN_ADC | **65** | GND_ADC_ANA |
| **3** | RESET | **24** | CLK_X | **45** | NBIASANA2 | **66** | VDD_ADC_ANA |
| **4** | SELECT | **25** | SYNC_X | **46** | NBIASANA | **67** | VDD_ADC_DIG |
| **5** | L/R | **26** | EOS_X | **47** | VLOW_ADC | **68** | GND_ADC_DIG |
| **6** | A0 | **27** | CLK_YR | **48** | G_AB | **69** | VDD_ADC_DIG_3.3/5 |
| **7** | A1 | **28** | SYNC_YR | **49** | VDD_RESR | **70** | VHIGH_ADC |
| **8** | A2 | **29** | EOS_YR | **50** | VDD_DIG | **71** | CLK_ADC |
| **9** | GND_ANA | **30** | GND_AMP | **51** | GND_DIG | **72** | PBIASDIG2 |
| **10** | VDD_ANA | **31** | VDD_AMP | **52** | VDD_PIX | **73** | PBIASENCLOAD |
| **11** | VDD_DIG | **32** | GND_DIG | **53** | VDD_ADC_ANA | **74** | PBIASDIG1 |
| **12** | GND_DIG | **33** | VDD_DIG | **54** | GND_ADC_ANA | **75** | BITINVERT |
| **13** | A3 | **34** | VDD_ANA | **55** | D0 | **76** | VDD_PIX |
| **14** | A4 | **35** | GND_ANA | **56** | D1 | **77** | GND_DIG |
| **15** | A5 | **36** | CAL | **57** | D2 | **78** | VDD_DIG |
| **16** | A6 | **37** | G0 | **58** | D3 | **79** | VDD_RESL |
| **17** | A7 | **38** | G1 | **59** | D4 | **80** | TRI_ADC |
| **18** | A8 | **39** | NBIASARR | **60** | D5 | **81** | TESTDIODE |
| **19** | LD_Y | **40** | PBIAS | **61** | D6 | **82** | TESTPIXELARRAY |
| **20** | LD_X | **41** | NBIAS_AMP | **62** | D7 | **83** | TESTPIXEL_RESET |
| **21** | CLK_YL | **42** | BLACKREF | **63** | D8 | **84** | TESTPIXEL_OUT |

## 1.4 Image sensor architecture

The base line of the STAR250 sensor design consists of an imager with a 512 by 512 array of active pixels at 25 µm pitch. The detector contains on-chip correction for Fixed Pattern Noise (FPN) in the column amplifiers, a programmable gain output amplifier and a 10-bit Analog to Digital Converter (ADC). Through additional preset registers the start position of a window can be programmed to enable fast read out of only part of the detector array.

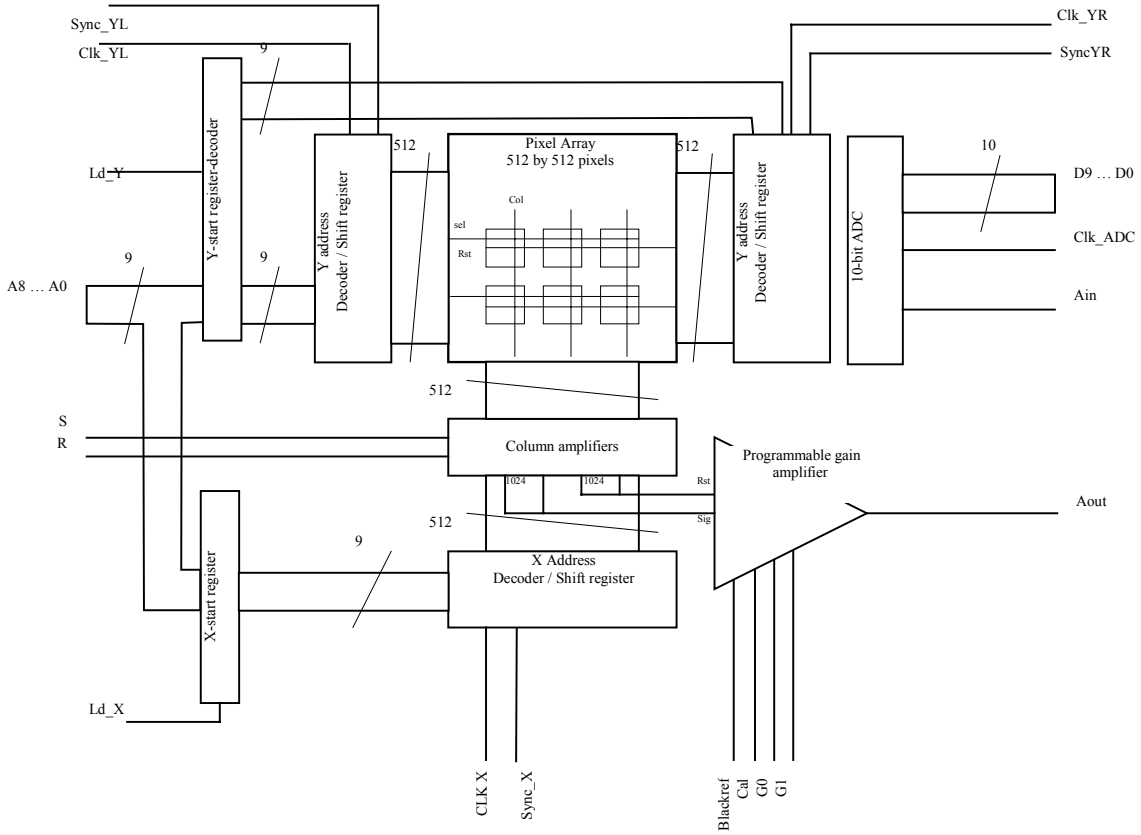



**Fig. Star250 schematic**

### *Electrical signal path*

The image sensor consists of several building blocks as outlined in Figure 1. The central element is a 512 by 512 pixel array with square pixels at 25 µm pitch. Unlike in classical designs the pixels of this sensor contain four photodiodes. This configuration enhances the MTF and reduces the PRNU. Figure 2 shows an electrical diagram of the pixel structure. The four photodiodes are connected in parallel to the reset transistor (T1). Transistor T2 converts the charge, collected on the photo diode node to a voltage signal that can be connected to the column bus by T3. The “Reset”- and the “Read”- entrance of the pixel are connected to one of the Y shift registers each.

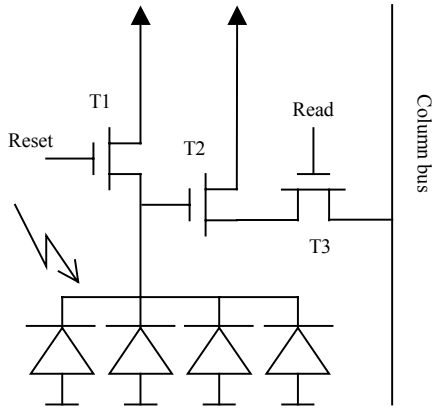



**Fig. Pixel schematic**

These shift registers are located next to the pixel array and contain as many outputs as there are rows in the pixel array. They are designed as"1-hot" registers (YL and YR shift register) each allowing selection of one row of pixels at a time. A clock pulse moves the pointer one position down the register resulting in the subsequent selection of every individual row for either reset or for read-out. The spatial offset between the two selected rows determines the integration time. A synchronisation pulse to the shift registers loads the value from a preset register into the shift register forcing the pointer to a pre-determined position. Windowing in the vertical (Y-) direction is achieved by presetting the registers to a row that is not the first row and by clocking out only the required number of rows.

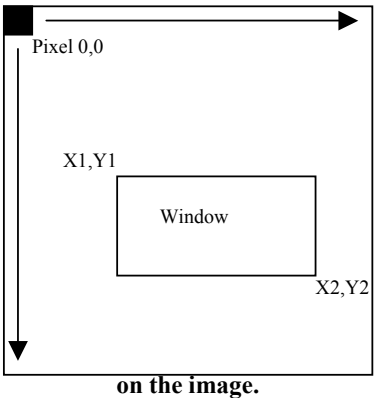
All pixel outputs are connected to a column bus and each column bus feeds the pixel signal to a column amplifier. Using a double sampling technique these amplifiers can subtract the remaining pixel offset from the signal. To serialise the output signal from the column amplifiers an identical shift/preset technique is used as for the vertical (Y-) direction. Windowing is thus also possible in the X-direction.

The signal from the column amplifiers is then fed to an output amplifier with four pre-settable gains. The offset correction of this amplifier is done through a black-reference procedure. The signal from the output amplifier is externally available on the analogue output terminator of the device.

The on-chip 10-bit ADC is electrically separated from the other circuits of the device and can be used if required. Alternatively an external ADC can be used and the internal ADC can be powered down.

## 1.5 Integrating imager operation principles

The STAR250 is a line-scan based integrating imager with provisions for versatile readout (windowing, electronic shuttering...). This combination results in certain timing relations and dependencies that are relevant to the end-user. These relations are defined and explained in the following paragraphs.




**on the image.**

### *1.5.1 Image definitions*

The following definitions concern the STAR250 image plane dimensions, and the format of the resulting pictures.

Image coordinates are defined with respect to an absolute origin1 (0,0). Figure 3a shows the coordinate system projected on the image, as it can be seen on a computer display or a printout. Figure 3b shows the coordinate system on the physical die.

This origin is at the *top-left corner* of the image, corresponding to the *top-right corner* on the actual STAR250 chip. The imager X-axis runs horizontally towards the right from the origin; the Y-axis runs vertically and downwards from the origin. In the resulting image reference frame, windows are scanned line by line, from top to bottom. Lines are scanned pixel by pixel, from the left to the right.

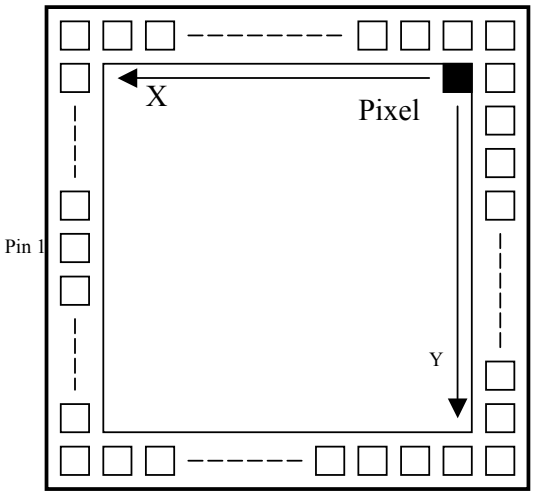



**Figure 2b: Coordinate system on the physical die.**

**Table 2: terms and definitions**

| Term | Definition | Value |
|---|---|---|
| Matrix | Full-size picture, 512 x 512 pixels | |
| Window | Region-of-interest, portion of a matrix under readout, a rectangular area of less than 512 x 512 pixels, at a user-defined position in the matrix plane | |
| Frame | Synonym to window, including the special case of a matrix | |
| $H_{frame}$ | Effective frame height | (Y2-Y1+1) |
| $W_{frame}$ | Effective frame width | (X2-X1+1) |
| $H_{matrix}$ | Matrix height | 512 lines |
| $W_{matrix}$ | Matrix width | 512 pixels |
| X1 | Top-left X coordinate of a frame | |
| Y1 | Top-left Y coordinate of a frame | |
| X2 | Bottom-right X coordinate of a frame | |
| Y2 | Bottom-right Y coordinate of a frame | |
| $X_{rd}$ | X coordinate of pixel currently under readout | |
| $Y_{rd}$ | Y coordinate of line currently under readout (YL) | |
| $Y_{rst}$ | Y coordinate of line currently under reset (YR) | |
| Delay Lines | Number of lines equivalent to the integration time | SYNC_YL-SYNC_YR |

## 1.6 Operation

### *1.6.1 Integrating imager operation*

In a line-scan integrating imager with electronic shutter, two continuous processes take care of image gathering. The first process resets lines in a progressive scan. At line reset, all of the pixels in a line are drained from any photocharges collected since their last reset or readout. After reset, a new exposure cycle starts for that particular line.

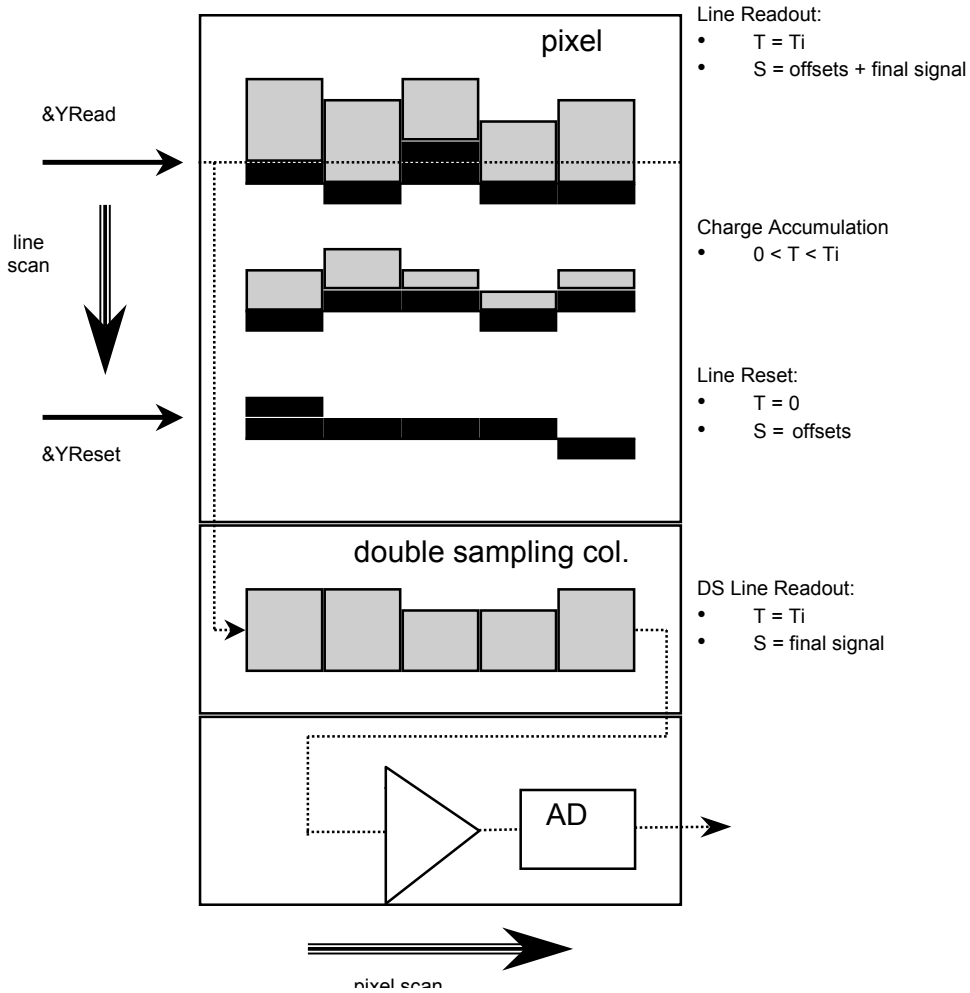



**Figure 4: Pixel signal sampling**

The second process is the actual readout, which also happens ins an equally fast line-wise progressive scan.
During readout, photo charges collected since the previous reset, are converted into an output voltage, which is then passed on - pixel by pixel - to the imager's pixel-serial output and ADC. Readout is destructive, i.e. the accumulation of charges from successive exposure phases is not possible in the present architecture.
Three internal address pointers control the processes of line and pixel readout and line reset. These pointers indicate the current line under readout ($Y_{rd}$), the current line under reset ($Y_{rst}$), and the current pixel under readout ($X_{rd}$), also see Figure 4. The progress rate of line resets is equal to the progress rate of line readouts. *Physically the Yread and Yrst register are located at left and right sides of the imager, and therefore named YL (the readout register) and YR (the reset register). The control of the row signals can be given to each of them, by the pin named L/R.*

The actual line readout process starts with addressing the line to read. This can be done either by initialising the $Y_{rd}$ pointer with a new value, or by shifting it one position beyond its previous value. (Addressing the line to be reset, Yrst is done in an analogous fashion). During the "blanking time", after the new line is addressed on the sensor, the built-in column-parallel double sampling amplifiers are operated, which renders offset-corrected values of the line under readout.

After the blanking time, the pixels of the row addressed by YL, are read by multiplexing all of the pixels one by one to the serial output chain. The pixel is selected by the $X_{rd}$ pointer, and that pointer can either be initialised with a new value, or be an increment of the previous position. The analog chain has further a track&hold stage, output buffer, followed by an (electrically separate) ADC.

The time between row resets and their corresponding row readouts is the effective exposure time (or integration time). This time is proportional to the number of lines, (*DelayLines*) between the line currently under reset and the line currently under readout: $DelayLines = (Y_{rst} - Y_{rd} + 1)$. This time is thus also equal to *the delay between the SYNC_YR pulse and the subsequent SYNC_YR.*
The effective integration time $t_{int}$ is thus calculated as (*delaylines * line time*). The line time itself is a function of four terms: the time to output the desired number of pixels in the line ($W_{frame}$), and the overhead ("blanking") time that is needed to select an new line and perform the double sampling and reset operations.

### 1.6.2 Variable integration time (electronic shuttering)

Figure 5 illustrates the variable integration time, for the case of $t_{int}$ equal to the frame read time $t_{rd,frame}$, the case of under-exposure, and the case of over-exposure.

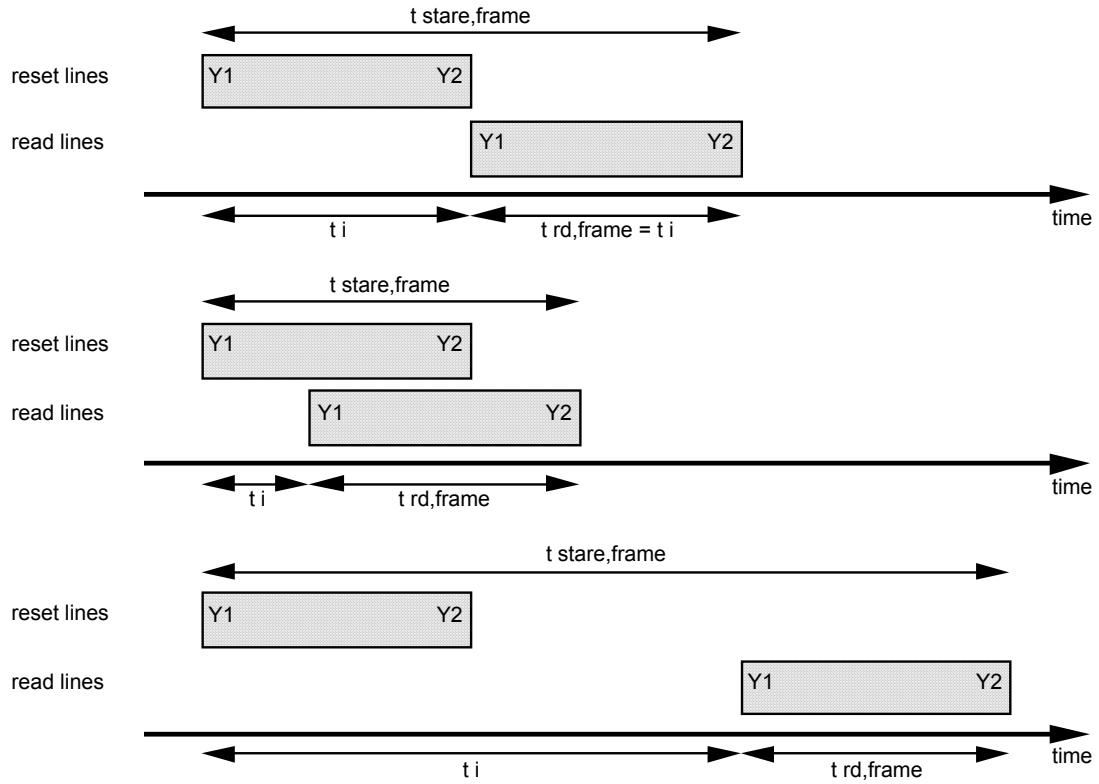



**figure 5: Variable integration time: nominal exposure, under-exposure and over-exposure. A new reset or reset cycle (not shown) may start whitel the previous read is still going on. Note that a read cycle also resets, thus in principle a reset cycle is only neede in underexposure.**

### *Image readout procedure*

The procedure to read out a windowed image, characterized with the coordinates (X1, Y1) and (X2, Y2), and with an integration time equivalent to `DelayLines` lines, is:

*A pre-amble or initialisation phase is not considered relevant. The sensor is read out continuously. The first frame – as there was no preceding reset of each pixel – is generally saturated and useless.*

**Image readout**
In an infinite uninterrupted loop, do, line-by-line:

**Synchronise** the read (YL) and/or reset (YR) registers, IN THIS CASES:
-SYNC_YL to re-initiate the readout sequence to row position Y1
-SYNC_YR to re-initiate the reset pointer to row position Y1
for all other lines do not pulse one of these SYNC_Y*.
**Operate** the double sampling column amplifiers, with two RESETs. Apply one to reset the line that is currently selected to produce the reset reference level for the double sampling column amplifiers. Apply the other reset to another line, depending on the required integration time reduction.

**Perform a line-readout:**
Reset the X read address shift register to the value in its shadow register (X1).
For (X2-X1+1) pixels do:
Perform a pixel readout operation, operating the track/hold and the ADC
Shift the X read address shift register one position further.
Shift the Y read and reset address shift registers one position further; note: if either of Y read or reset address shift register comes at a position equivalent to Y2, wrap it around to position Y1 by pulsing SYNC_YL.

## 1.7 Timing and control sequences

The following paragraphs describe the timing of the digital control signals to be applied to the sensor. The given information is based upon simulations and must be confirmed by practical experiments after fabrication of test samples.

### *1.7.1 Basic timing*

Figure 6 and Figure 7 show the basic timing diagram of the STAR250 image sensor and Table 3 shows the timing specifications of the clocking scheme.

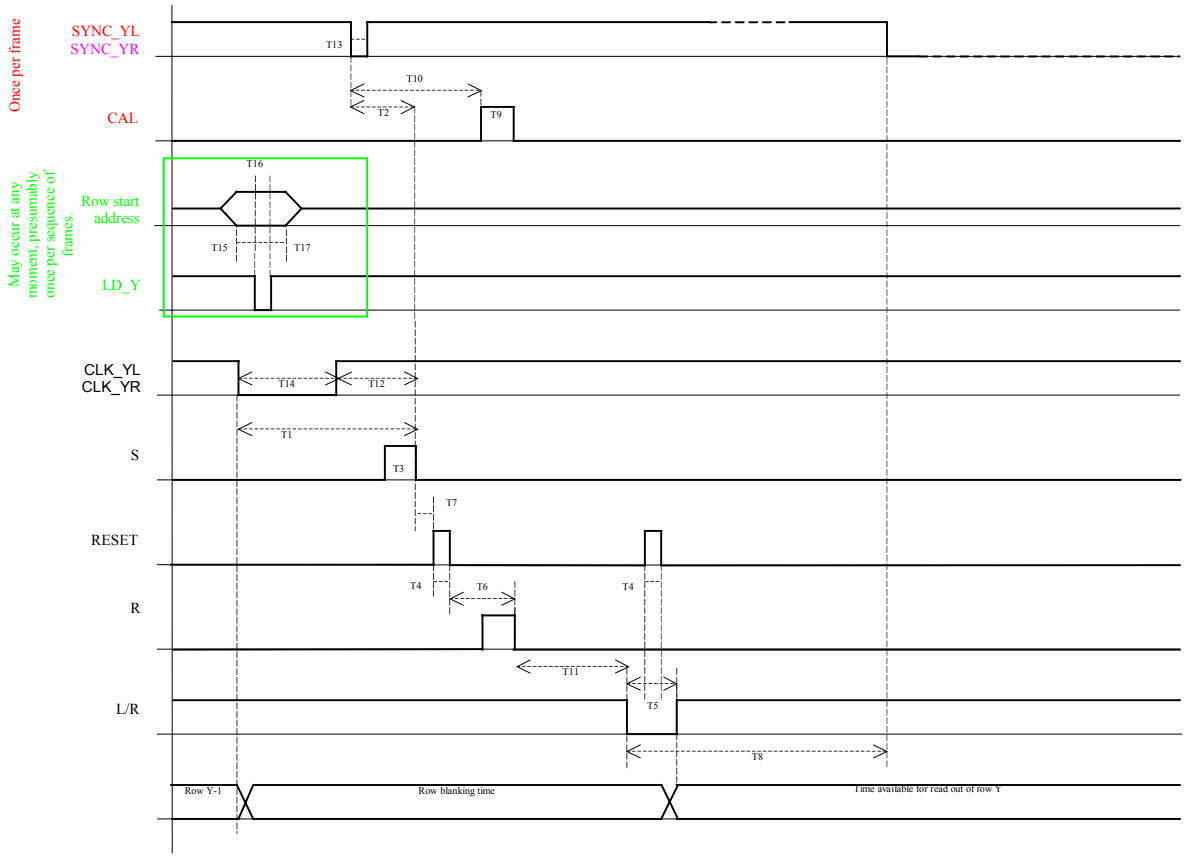



Figure 6: Frame read-out timing sequence

Note: SYNC_YR is not identical to as SYNC_YL. SYNC_YR is used in case of electronic shutter. The CLK_YR is driven identically as CLK_YL, but the SYNC_YR pulse leads the SYNC_YL pulse by a certain number of rows. This lead-time is the effective integration (electronic shutter ~) time. Relative to the row timing, both SYNC pulses are given at the same time position, once per frame, but during different rows.
SYNC_YL is pulsed when the first row will be read out and SYNC_YR is pulsed for the electronic shutter to start for this first row. CAL is pulsed on the first row too, 2 µs later than SYNC_YL.
The minimal idle time is 1.4 µs (before starting reading pixels). However, it is advised not to read out pixels during the complete row initialisation process (in between the rising edge on S and the falling edge on L/R). In this case, the total idle time is minimally .
This timing assumes that the Y start register has been loaded in advance, which can occur at any time but before the pulse on SYNC_YL or SYNC_YR.

**Table 4: Timing specifications**

| Symbol | Min | Typ | Description |
|---|---|---|---|

| | | | |
|---|---|---|---|
| **T1** | 1.8 µs | | Delay between selection of new row by falling edge on CLK_YL and falling edge on S.<br>Minimal value. Normally, CLK_YR should be low already at the end of the previous sequence. |
| **T2** | 1.8 µs | | Delay between selection of new a row by SYNC_YL and falling edge on S. |
| **T3** | 0.4 µs | | Duration of S and R pulse. |
| **T4** | 0.1 µs | | Duration of RESET pulse. |
| **T5** | T4 + 40 ns | 0.3 µs | L/R pulse must overlap second RESET pulse at both sides. |
| **T6** | 0.8 µs | | Delay between falling edge on RESET and falling edge on R. |
| **T7** | 20 ns | 0.1 µs | Delay between falling edge on S and rising edge on RESET. |
| **T8** | 0 | 1 µs | Delay between falling edge on L/R and falling edge on CLK_Y. |
| **T9** | 100 ns | 1 µs | Duration of cal pulse. The CAL pulse is given once each frame. |
| **T10** | 0 | 2 µs | Delay between falling edge of SYNC_YL and rising edge of CAL pulse. |
| **T11** | 40 ns | 0.1 µs | Delay between falling edge on R and rising edge on L/R. |
| **T12** | 0.1 µs | 1 µs | Delay between rising edge of CLK_Y and falling edge on S. |
| **T13** | | 0.5 µs | Pulse width SYNC_YL / YR |
| **T14** | | 0.5 µs | Pulse width CLK_YL / YR |
| **T15** | 10 ns | | Address set-up time |
| **T16** | 20 ns | | Load X / Y start register value |
| **T17** | 10 ns | | Address stable after load |
| **T18** | 10 ns | | |
| **T19** | 20 ns | | SYNC_X pulse width. SYNC_X while CLK_X is high. |
| **T20** | 10 ns | | |
| **T21** | | 40 ns | Analogue output is stable during CLK_X low. |
| **T22** | | 40 ns | CLK_X pulse width: During this clock phase the analogue output ramps to the next pixel level. |
| **T23** | | 125 ns | ADC digital output stable after falling edge of CLK_ADC |

### *1.7.2 How to load the X- and Y- start positions*

The start positions (start addresses) for “ROI” (region of interest) are pre-loaded in the X or Y start register. They becom effective by the appication of the SYNC_X, SYNC_YL and/or SYNC_YR. The start X- or Y address must be applied to their common address bus, and the corresponding LD_X or LD_Y pin must be pulsed.

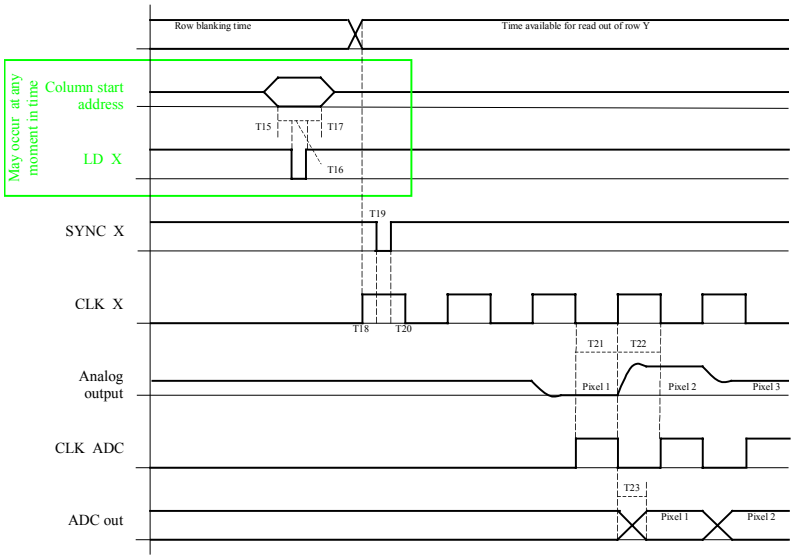



**Figure 7: Column read-out timing sequence**

On each **falling** edge of CLK_X, a new pixel of the same row (line) is accessed. The output stage is in hold when CLK_X is low and starts generating a new output after a rising edge on CLK_X.

The following timing constraints apply:
The X or Y start addresses can be uploaded well in advance, before the X or Y shift registers are preset by a SYNC pulse. However, if necessary, they can be loaded just before the SYNC_X or SYNC_Y pulse as shown in the figure.

E.g. the X start register can be loaded during the row idle time. The Y start register can be loaded during readout of the last row of the previous frame.
If the X or Y start address does not change for subsequent frames, it does not need to be reloaded in the register.

### *1.7.3 Other signals:*

The SELECT signal must be tied to Vdd for normal operation. This signal was added for diagnostic reasons and inhibits the pixel array operation when held low.
The CAL signal sets the output amplifier DC offset level. When this signal is active (high) the pixel array is internally disconnected from the output amplifier, its gain is set to unity and its input signal is connected to the BLACK_REF input. This action must be performed at least once per frame. (on may even choose to do it once per line – but not advised)
EOS_X, EOS_YL and EOS_YR produce a pulse when the respective shift register comes at its end. These outputs are used mainly during testing to verify proper operation of the shift registers.
TEST DIODE and TESTPIXEL ARRAY are connections to optical test structures that are used for electro-optical evaluation. TEST-DIODE is a plain photodiode with an area of 14x5 pixels. TESTPIXEL_ARRAY is an array (14x5) of pixels where the photodiodes are

connected in parallel. These structures are used to measure the photocurrent of the diodes directly.
TESTPIXEL_RESET and TESTPIXEL-OUT are connections to a single pixel that can be used for test purposes.

# 2 Absolute maximum ratings

**Table 4: absolute maximum ratings**

| Parameter | Value | Units |
|---|---|---|
| Any supply voltage | -0.5 to +7 | V |
| Voltage on any input pin | -0.5 to Vdd+0.5 | V |
| Operating temperature | 0 to 65 | Deg C |
| Storage temperature | -40 to 100 | Deg C |

# 3 Specifications

## 3.1 DC operating conditions

**Table 5: DC operating conditions**

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| VDD_ANA | Analogue supply voltage to imager part | | 5 | | V |
| VDD_DIG | Digital supply voltage to image opart | | 5 | | V |
| VDD_ADC_ANA | Analogue supply voltage to ADC | | 5 | | V |
| VDD_ADC_DIG | Digital supply voltage to ADC | | 5 | | V |
| VDD_ADC_DIG_3.3/5 | Supply voltage of ADC output stage | | 3.3 to 5 | | V |
| VIH | Logical ‘1’ input voltage | 2.3 | | Vdd | V |
| VIL | Logical ‘0’ input voltage | 0 | | 1 | V |
| VOH | Logical ‘1’ output voltage | 4.25 | 4.5 | | V |
| VOL | Logical ‘0’ output voltage | | 0.1 | 1 | V |

## 3.2 Resistor biases: power vs. speed

## 3.3 AC operating conditions

**Table 6: AC operating conditions**

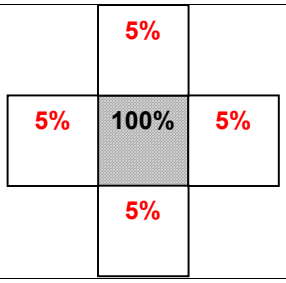
| Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|
| Pixel output rate | | 5 | 8 | MHz |
| Frame rate | | 18 | 29 | Full frames /s |

## 3.4 Electro-optical characteristics

### *3.4.1 Overview*

**Table 7: Electro-optical specifications**

| Parameter | Specification (all typical) | Comment |
|---|---|---|
| Detector technology | CMOS Active Pixel Sensor | |
| Pixel structure | 3-transistor active pixel<br>4 diodes per pixel | Radiation-tolerant pixel design<br>4 Photodiodes for improved MTF |
| Photodiode | High fill factor photodiode | |
| Sensitive area format | 512 by 512 pixels | |
| Pixel size | 25 x 25 $\mu m^2$ | |
| Spectral range | 200 – 1000 nm | See curves |
| Quantum Efficiency x Fill Factor | Max. 35% | Above 20% between 450 and 750 nm.<br>(note: metal fillfactor (MFF) is 63%) |
| Full Well capacity | 311K electrons | When output amplifier gain = 1 |
| Linear range within $\pm$ 1% | 128K electrons | When output amplifier gain = 1 |
| Output signal swing | 1.68 V | When output amplifier gain = 1 |
| Conversion gain | 5.7 $\mu$V/e- | When output amplifier gain = 1<br>near dark |
| Temporal noise | 76 e- | Dominated by kTC |
| Dynamic Range | 74 dB (5000:1) | At the analog output |
| FPN (Fixed Pattern Noise) | $1\sigma$ < 0.1% of full well (typical) | Measured local, on central image area 50% of pixels, in the dark |
| PRNU (Photo Response Non-uniformity) | Local: $1\sigma$ = 0.39% of response<br>Global: $1\sigma$ = 1.3% of response | Measured in central image area 50% of pixels, at Qsat/2 |
| Average dark current signal | 4750 e-/ s | At RT |
| DSNU (dark signal non uniformity) | … e-/s RMS (TBC) | At RT, scale linearly with integration time. |
| MTF | Horizontal: 0.36<br>Vertical: 0.39 | at 600 nm. |

| | | |
|---|---|---|
| Optical cross talk | 5% (TBC) to nearest neighbour if central pixel is homogeneously illuminated |   |
| Anti-blooming capacity | x 1000 to x 100 000 | |
| Output amplifier gain | 1, 2, 4 or 8 | Controlled by 2 bits |
| Windowing | X and Y 9-bit programmable shift registers | Indicate upper left pixel of each window |
| Electronic shutter range | 1 : 512 | Integration time is variable in time steps equal to the row readout time |
| ADC | 10 bit | |
| ADC linearity | ± 3.5 counts | INL |
| Missing codes | none | |
| ADC setup time | 310 ns | To reach 1% of final value |
| ADC delay time | 125 ns | |
| Power Dissipation | < 350 mW | Average at 8 MHz pixel rate |

### *3.4.2 Spectral response*

Figure 5 shows a typical spectral response curve. The fringes in the curve result from optical interference in the top dielectric layers.

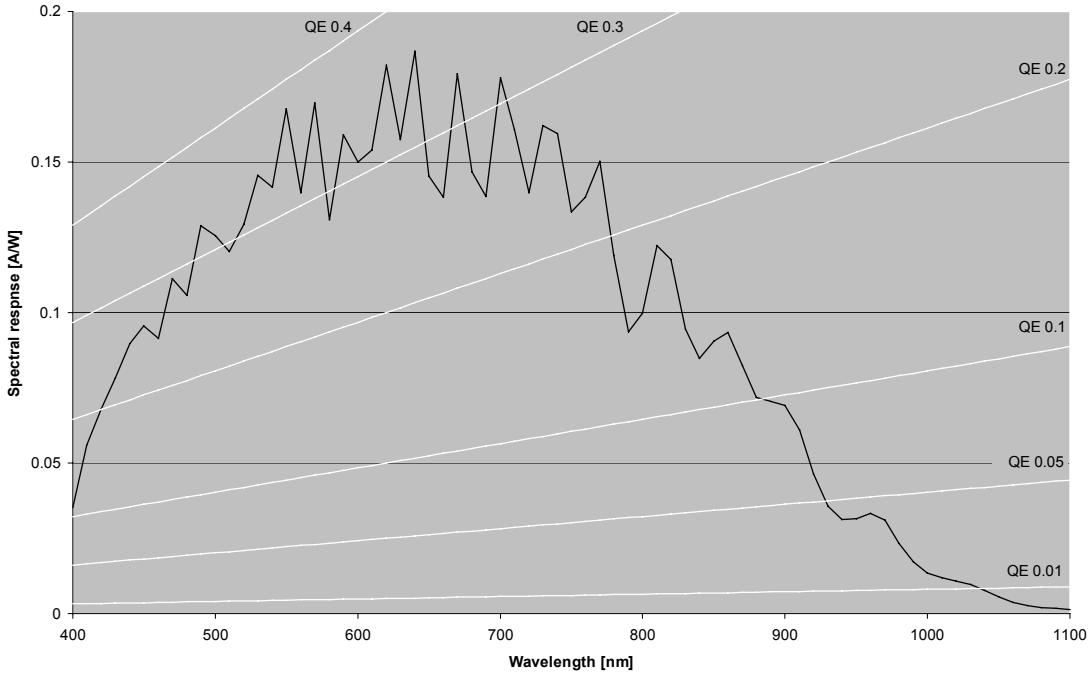
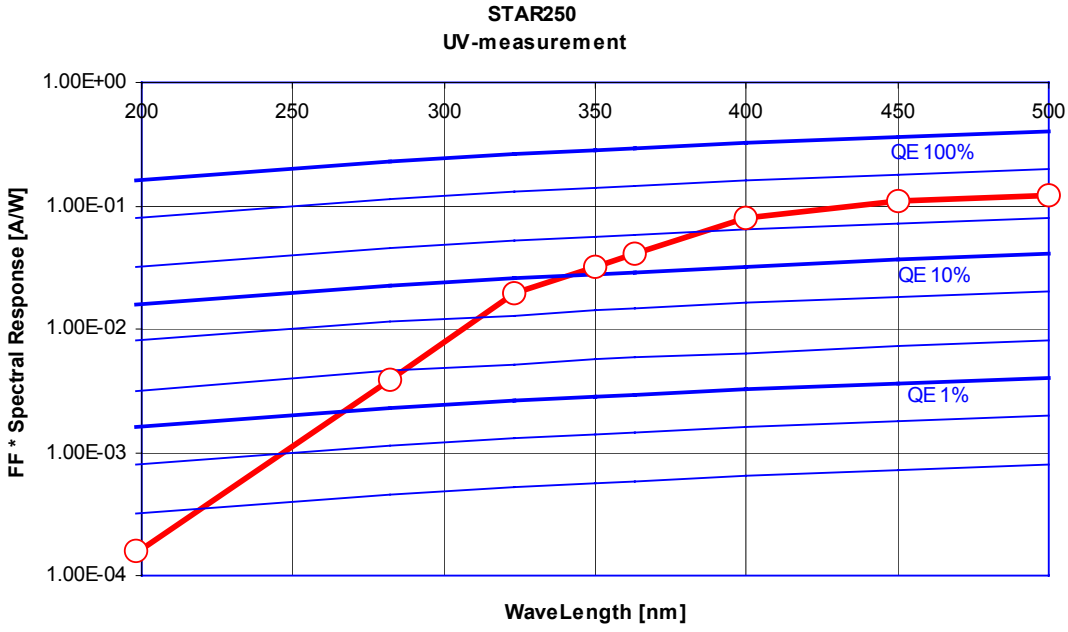



**Figure 5: Typical spectral response curve lines of equal QE*FF are indicated.**



### 3.4.3 Pixel profile

The pixel profile was measured using the 'knife-edge' method: the image of a target containing a black-to white transition is scanned over a certain pixel with sub-pixel resolution steps. The image sensors settings and the illumination conditions are adjusted such that are the transitions covers 50 % of the output range. The scan is performed both in horizontal and in vertical direction.

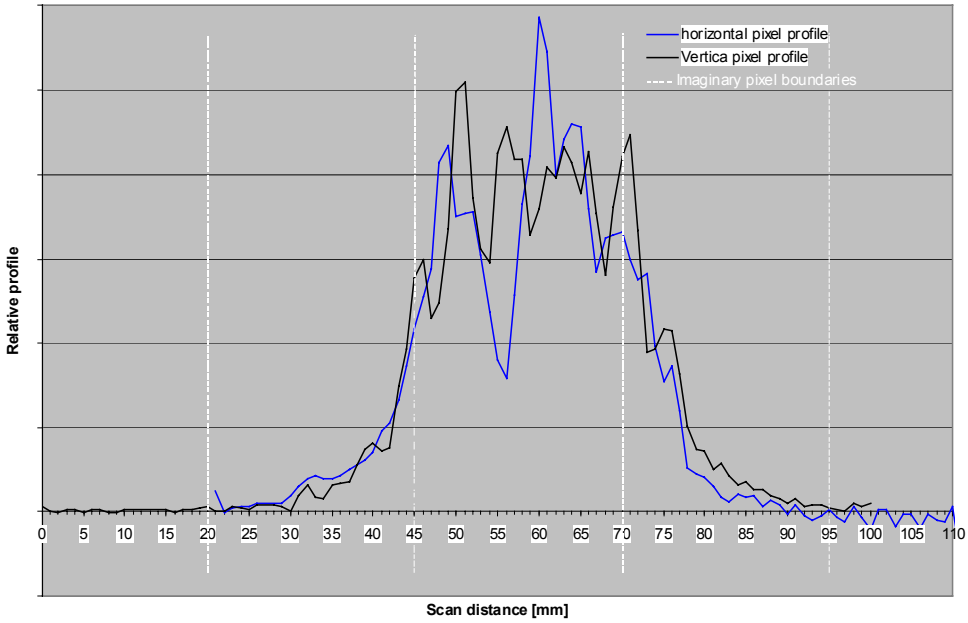



**Figure 4: Typical pixel profiles**

# 4 Environmental characteristics

## 4.1 Temperature

**Table 8: Temperature specifications**

| Parameter | Value | Units |
|---|---|---|
| Operating temperature | 0 to 65 | Deg C |
| Storage temperature | -40 to 100 | Deg C |

## 4.2 Radiation tolerance

**Table 9: Radiation specifications**

| Parameter | Criterion | Qualification level |
|---|---|---|
| Gamma Total Dose Radiation tolerance | Increase in average dark current < 1 $nA/cm^2$ after 3 MRad | see graph |
| | Image operation with dark signal < 1V/s | 10 Mrad demonstrated (Co60) |
| | Single (test) pixel operation with dark signal < 1V/s | 24 Mrad demonstrated (Co60) |
| Proton radiation tolerance | 1% of pixels has an increase in dark current > 1 $nA/cm^2$ after 3*10^10 protons at 11.7 MeV | see graph |
| SEL threshold | > 80 MeV $cm^3$ $mg^{-1}$ | To be confirmed |

Next figure shows the increase in dark current under total dose irradiation. This curve was measured during high dose rate radiation. Annealing results in a significant decrease of dark current.

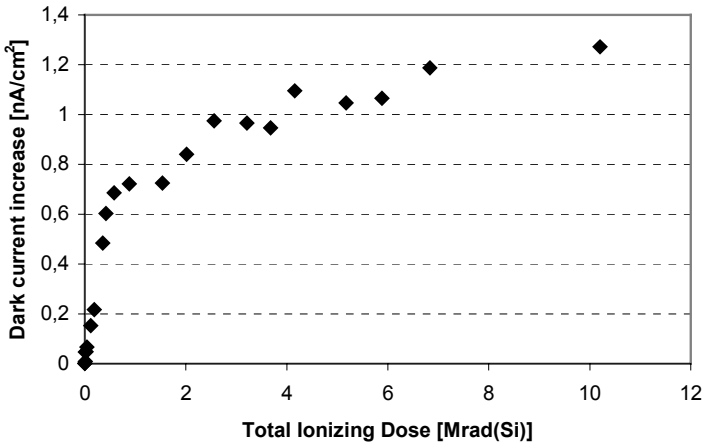



**Figure 5: Increase in dark current vs. total dose radiation**

Next figure shows the percentage of pixels with a dark current increase under 11.7 Mev radiation with protons.

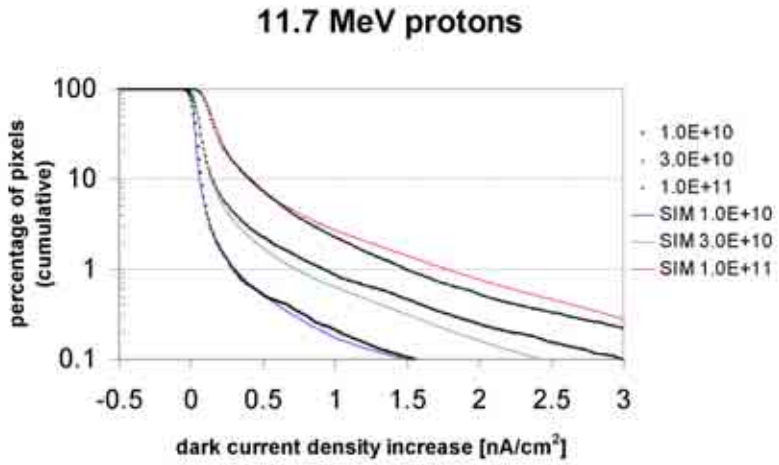



**Figure 6: Increase in dark current under proton irradiation (measurements / simulation model)**

# 5 Pin configuration

**Table 10: Power supply connections**

| | | |
|---|---|---|
| **10** | VDD_ANA | Analog power supply: 5 V |
| **11** | VDD_DIG | Digital power supply 5V |
| **31** | VDD_AM | Power supply of output amplifier: 5 V |

| | | |
|---|---|---|
| | P | |
| **33** | VDD_DIG | Digital power supply 5V |
| **34** | VDD_ANA | Analogue power supply: 5 V |
| **49** | VDD_RESR | Reset power supply 5V |
| **50** | VDD_DIG | Digital power supply 5V |
| **53** | VDD_ADC_ANA | ADC analogue power supply 5V |
| **66** | VDD_ADC_ANA | ADC analogue power supply: 5 V |
| **67** | VDD_ADC_DIG | ADC digital power supply 5V |
| **69** | VDD_ADC_DIG_3.3/5 | ADC 3.3V power supply for digital output of ADC.<br>For interface with 5V external system: connect to VDD_ADC_DIG.<br>For interface with 3.3 V external system: connect to 3.3V power supply. |
| **52**<br>**76** | VDD_PIX | Pixel array power supply [default: 5V, the device is then in "soft reset". In order to avoid the image lag associated with soft reset, reduce this voltage to 3…3.5 V "hard reset"] |
| **78** | VDD_DIG | Digital power supply 5V |
| **79** | VDD_RESL | Reset power supply 5V |

**Table 11: Ground connections**

| | | |
|---|---|---|
| **9** | GND_ANA | Analog ground |
| **12** | GND_DIG | Digital ground |
| **30** | GND_AMP | Ground of output amplifier |
| **32** | GND_DIG | Digital ground |
| **35** | GND_ANA | Analog ground |
| **51** | GND_DIG | Digital ground |
| **54** | GND_ADC_ANA | ADC analog ground |
| **65** | GND ADC A | ADC analog ground |

| | | |
|---|---|---|
| | NA | |
| **68** | GND_ADC_DIG | ADC digital ground |
| **77** | GND_DIG | Digital ground |

**Table 12: digital input signals**

| | | |
|---|---|---|
| **1** | S | Control signal for column amplifier<br>Apply pulse pattern – see sensor timing diagram |
| **2** | R | Control signal for column amplifier<br>Apply pulse pattern – see sensor timing diagram |
| **3** | RESET | Resets row indicated by left/right shift register<br>high active (1= reset row)<br>Apply pulse pattern – see sensor timing diagram |
| **4** | SELECT | Selects row indicated by left/right shift register<br>high active (1=select row)<br>Apply 5 V DC for normal operation |
| **5** | L/R | Use left or right shift register for SELECT and RESET<br>1 = left / 0 = right – see sensor timing diagram |
| **6** | A0 | Start address for X- and Y-pointers (LSB) |
| **7** | A1 | Start address for X- and Y-pointers |
| **8** | A2 | Start address for X- and Y-pointers |
| **13** | A3 | Start address for X- and Y-pointers |
| **14** | A4 | Start address for X- and Y-pointers |
| **15** | A5 | Start address for X- and Y-pointers |
| **16** | A6 | Start address for X- and Y-pointers |
| **17** | A7 | Start address for X- and Y-pointers |
| **18** | A8 | Start address for X- and Y-pointers (MSB) |
| **19** | LD_Y | Latch address (A0…A8) to Y start register (0 = track, 1 = hold) |
| **20** | LD_X | Latch address (A0…A8) to X start register(0 = track, 1 = hold) |
| **21** | CLK_YL | Clock YL shift register (shifts on falling edge) |
| **22** | SYNC_YL | Sets YL shift register to location preloaded in Y start register<br>Low active (0=sync) |

| | | |
|---|---|---|
| | | Apply SYNC_YL when CLK_YL is high |
| **24** | CLK_X | Clock X shift register (output valid & stable when CLK_X is low) |
| **25** | SYNC_X | Sets X shift register to location preloaded in X start register.<br>Low active (0=sync)<br>Apply SYNC_X when CLK_X is high<br>After SYNC_X, apply falling edge on CLK_X, and rising edge on CLK_X. |
| **27** | CLK_YR | Clock YR shift register (shifts on falling edge) |
| **28** | SYNC_YR | Sets YR shift register to location preloaded in Y start register<br>Low active (0=sync)<br>Apply SYNC_YR when CLK_YR is high |
| **36** | CAL | Initialise output amplifier<br>Output amplifier will output BLACKREF in unity gain mode when CAL is high (1)<br>Apply pulse pattern (one pulse per frame) – see sensor timing diagram |
| **37** | G0 | Select output amplifier gain value: G0 = LSB; G1 = MSB<br>00 = unity gain; 01 = x2; 10= x4; 11=x8 |
| **38** | G1 | idem |
| **71** | CLK_ADC | ADC clock<br>ADC converts on falling edge |
| **75** | BITINVERT | 1 = invert output bits<br>0 = no inversion of output bits |
| **80** | TRI_ADC | Tri-state control of digital ADC outputs<br>1 = tri-state; 0 = output |

**Table 13: Digital output signals**

| | | |
|---|---|---|
| **23** | EOS_YL | End-of-scan of YL shift register<br>Low first clock period after last row (low active) |
| **26** | EOS_X | End-of-scan of X shift register<br>Low first clock period after last active column (low active) |
| **29** | EOS_YR | End-of-scan of YR shift register<br>Low first clock period after last row (low active) |

| | | |
|---|---|---|
| **55** | D0 | ADC output bit (LSB) |
| **56** | D1 | ADC output bit |
| **57** | D2 | ADC output bit |
| **58** | D3 | ADC output bit |
| **59** | D4 | ADC output bit |
| **60** | D5 | ADC output bit |
| **61** | D6 | ADC output bit |
| **62** | D7 | ADC output bit |
| **63** | D8 | ADC output bit |
| **64** | D9 | ADC output bit (MSB) |

**Table 14: Analog input signals**

| | | |
|---|---|---|
| **39** | NBIASARR | Connect with 500 KΩ to Vdd and decouple to ground by 100 nF capacitor |
| **40** | PBIAS | Connect with 40 KΩ to ground and decouple to Vdd by 100 nF capacitor for 12.5 MHz pixel rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation) |
| **41** | NBIAS_AMP | Output amplifier speed/power control<br>Connect with 82K to VDD and decouple with 100 nF to GND for 12.5 MHz output rate. (Lower resistor values yield higher maximal pixel rates at the cost of extra power dissipation) |
| **42** | BLACKREF | Control voltage for output signal offset level<br>Buffered on-chip, the reference level can be generated by a 100K resistive divider.<br>Connect to +/- 2 V DC for use with on-chip ADC |
| **44** | IN_ADC | Input, connect to sensor's output<br>Input range is between 2 & 4 V (VLOW_ADC & VHIGH_ADC) |
| **45** | NBIASANA2 | Connect with 100 KΩ to VDD and decouple to GND |
| **46** | NBIASANA | Connect with 100 KΩ to VDD and decouple to GND |
| **47**<br>**70** | VLOW_ADC<br>VHIGH_ADC | Low reference and high reference voltages of ADC should be about 2 and 4 V.<br>The internal resistance between VLOW_ADC and VHIGH_ADC is about 1.1 K.<br>The required voltage settings on VLOW ADC and |

| | | |
|---|---|---|
| | | VHIGH_ADC can be approximated by tying VLOW_ADC with 1.2 K to GND and VHIGH_ADC with 560 Ohm to VDD |
| **48** | G_AB | Anti-blooming drain control voltage:<br>Default: connect to ground. The anti-blooming is operational but not maximal<br>Apply 1 V DC for improved anti-blooming |
| **72** | PBIASDIG2 | Connect with 100K to GND and decouple to VDD |
| **73** | PBIASENCLOAD | Connect with 100K to GND and decouple to VDD |
| **74** | PBIASDIG1 | Connect with 47K to GND and decouple to VDD |

**Table 15: Analog output signals**

| | | |
|---|---|---|
| **43** | OUT | Analogue output signal<br>To be connected to the analogue input of the ADC |

**Table 16: Test structures**

| | | |
|---|---|---|
| **81** | TESTDIODE | Plain photo diode, size: 14 x 25 pixels<br>Must be left open for normal operation |
| **82** | TESTPIXARRAY | Array of test pixels, connected in parallel (14 x 25 pixels)<br>Must be left open for normal operation |
| **83** | TESTPIXEL_RESET | Reset input of single test pixel<br>Must be tied to GND for normal operation |
| **84** | TESTPIXEL_OUT | Output of single test pixel<br>Must be left open for normal operation |

# 6 Mechanical data

## 6.1 Package drawing

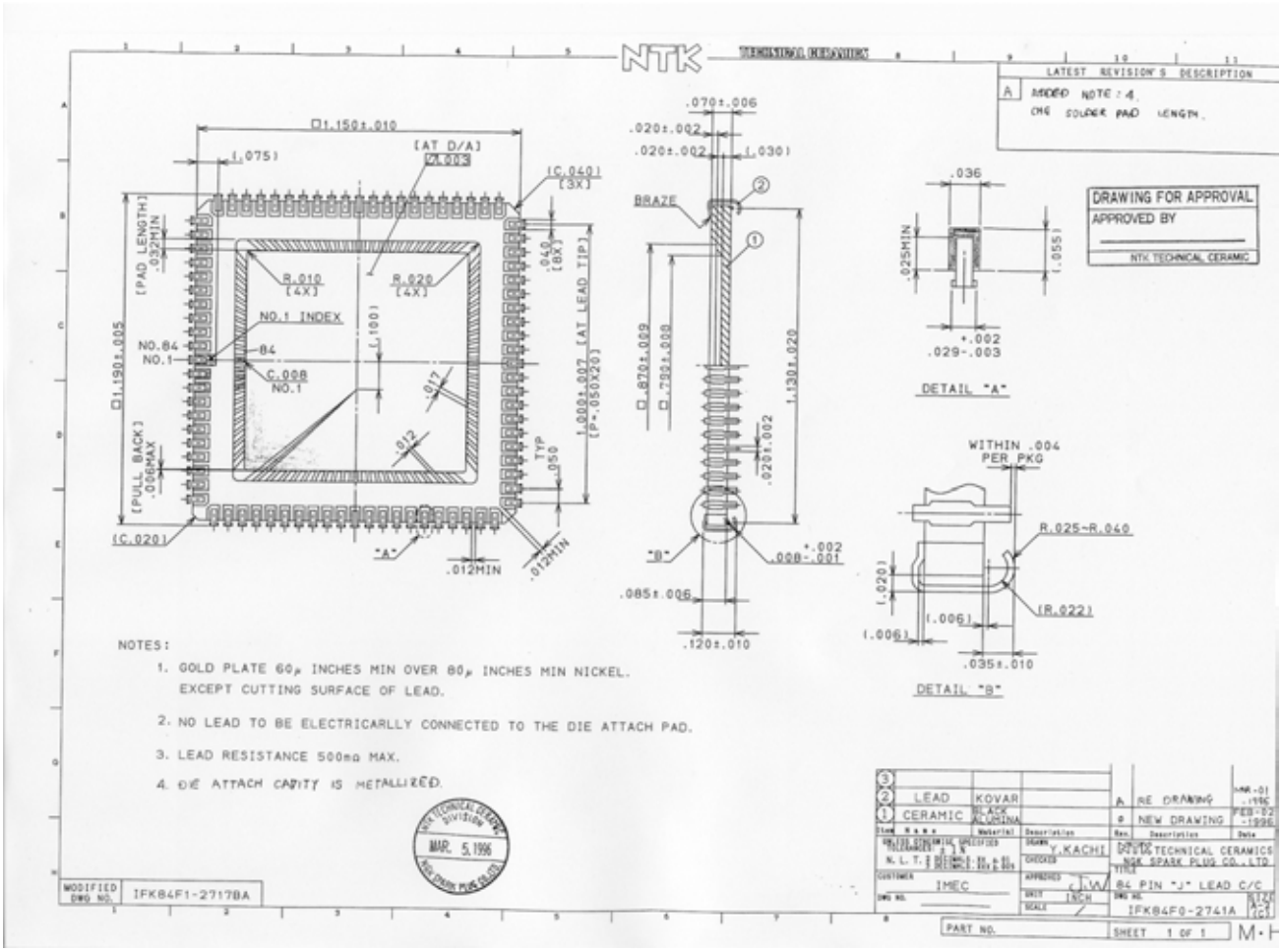



**Figure 9: Package dimensions**

**Table 17: Package specifications**

| | |
|---|---|
| Type | JLCC-84 |
| Material: | Black Alumina<br>BA-914 |
| Thermal expansion coefficient | 7.6 x $10^{-6}$ /K |

## 6.2 Die alignment

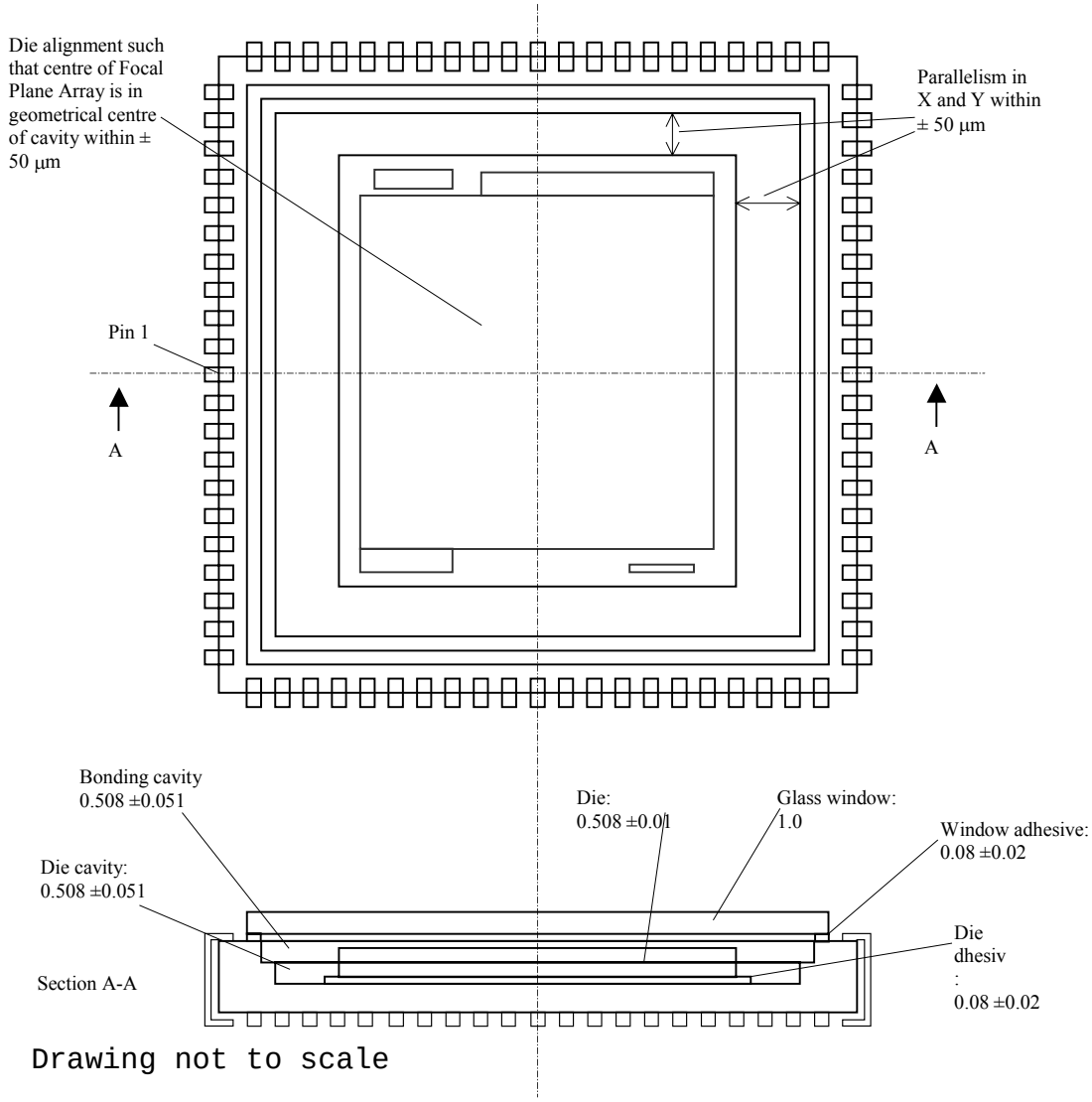



**Figure 10: Die alignment**

The die is aligned manually in the package to a tolerance of ±50µm and the alignment is verified after hardening the die adhesive.

## 6.3 Window specifications

In the standard processing flow the following window is mounted:

**Table 18: Glass cover specification**

| | |
|---|---|
| Material: | D263 |
| Dimensions: | 25 x 25 mm +- 0.2 |

| | mm |
|---|---|
| Thickness: | 0.55 mm +- 0.05 mm |

(EOD)