DATEL®
INNOVATION and EXCELLENCE

PC-414

High-Speed Analog Input Board for ISA Computers

FEATURES

- **Up to 10 MHz A/D sample rate**
- **Very low harmonic distortion**
- **Analog input comparator trigger**
- **Choice of 12, 14, or 16-bit A/D resolution**
- **Optional 2 to 8-channel simultaneous sampling**
- **On-board FIFO memory up to 16,384 samples**
- **Ideal for FFT's, DSP, or array processor "front ends"**
- **Non-bus burst parallel port for seamless recording**

NEW
Now with
LabVIEW® VI's

Offering very high system speed, the PC-414 is a multi-channel analog input board for ISA compatible computers. Input bandwidth is available up to 5 MHz and may be sampled at up to 10 MHz. A common motherboard is used, with the analog section contained in a pluggable 2" by 4" module. This allows for a family of several different Sample/Hold - A/D Converter speed and resolution options by exchanging analog modules.

The analog input ranges of the A/D converter are selectable as unipolar 0 to +10 V, or bipolar ±5 V, or ±10 V depending on the model. Model PC-414E offers 16 single-ended or 8 differential high speed channels.

Models PC-414F, G, J, K, L, M, and P include a simultaneous sampling section. This function acquires signals on parallel channels at the same time. This prevents phase errors and skewing of multichannel correlated signals. Applications include high speed cross-channel computation, beam-former coherency for sonar or acoustics, telemetry, multiple carrier demodulation, and highly concurrent system testing.

A/D data passes to an on-board First-In, First-Out (FIFO) data memory and then to the host computer bus interface under software control. The FIFO acts to uncouple the precise timing of the A/D section from the block-oriented data transfers on the bus. The design can continuously collect analog data with non-stop converter triggering while data is simultaneously read from the FIFO. This allows the collection of "seamless" wide-bandwidth signals of millions of samples or greater. Functions such as FFT sampling cannot tolerate lost samples without increases in "arithmetic" noise during computation processing.

Data can be transferred to mass storage peripherals such as disk or magnetic tape. Applications include long-baseline studies in astrophysics, component life testing, and anomalous pattern search.

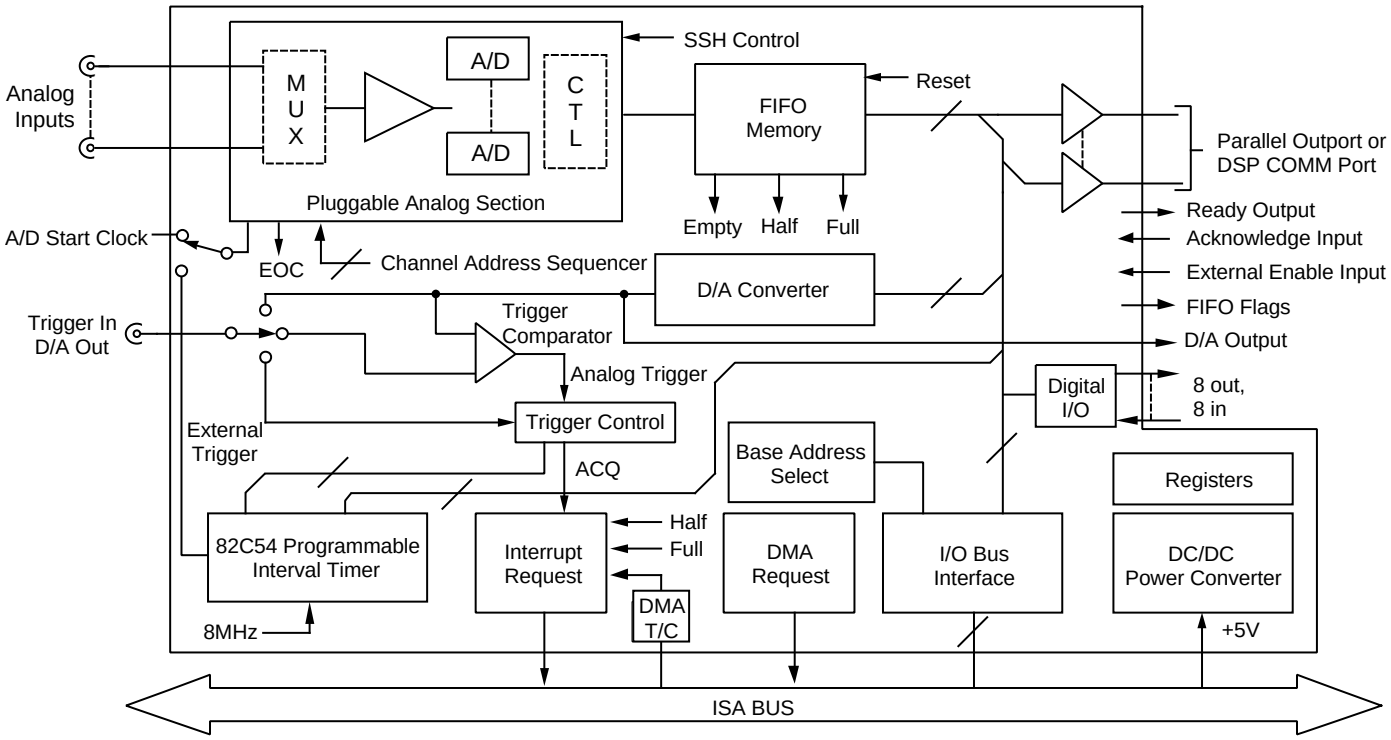

Figure 1. Functional Block Diagram

The FIFO data output may also be routed under host software control to an on-board parallel data port instead of being sent to the computer bus. This parallel burst channel data may be read by an external processor at very high speeds and avoids possible speed restrictions of the computer bus. The outport uses a very simple ready/acknowledge transfer handshake which is adaptable to any remote parallel port including DT Connect®. See model PC-414COM using a DSP COMM port interface.

The analog section of the PC-414 is optimized for high signal quality and very low dynamic noise. The PC-414 is ideal as an FFT "front-end" or DSP quantizer for array processors.

The A/D conversion timing section is designed for accurate multi-scan data acquisition. Software programmable timers control the interval between each conversion and each multichannel scan. A programmable sample counter allows sample blocks of specified length independent of FIFO length. The timer/counter section uses a precision on-board crystal clock. Timeout and sample count activities may be monitored using I/O status registers and/or programmable interrupts. The interrupt method may be fully synchronized with software programmable DMA transfers directly to host computer memory.

S/H - A/D triggering can originate from several sources under software control. The internal timebase is the normal trigger source although single conversions or scans may be directly commanded by host I/O register writes. An external trigger clock may also be used to precisely synchronize sampling with external events. This external trigger may start a single multichannel scan or "N" multiple scans separated by programmable delays.

Analog sampling can also be level-triggered using an on-board analog comparator and an external level input. The reference trigger level to the comparator is derived from an on-board 12-bit D/A converter. If preferred, the D/A converter may also be used as a general purpose analog output channel.

The PC-414B, D, F, G, H, K, M, N, and P versions contain five SMA coaxial signal connectors. Four connectors are for the sampled analog channels. The fifth connector is used for external timebase clock input, external analog trigger signal, or for the analog output. The PC-414E, J, and L versions contain 25-pin "D" connectors (DB-25S). The burst channel parallel port uses an internal dual row header.

The computer interface conforms to the PC-AT bus structure. All data transfers (control, status, and A/D data) use 16-bit transfers. Interrupt level selection is done via software. Interrupt servicing is generated for a variety of reasons such as A/D data read, DMA terminal count, sample count reached, FIFO half-full, or FIFO full.

A/D output data coding is right-justified two's complement with sign extension, if desired, straight binary coding can also be selected making it directly compatible with high level computer languages such as "C", Visual C++, Borland C Builder, Visual Basic, and others.

Software

The PC-414 can be controlled via optional DOS or Windows NT or 95/98 Control panels, third party software such as LabVIEW, or user written code in languages such as Visual C++, Borland C Builder, Visual Basic, etc.

PC-414SET An MS-DOS based menu driven acquisition program. Includes setup and configuration functions, data acquisition via interrupt and DMA, D/A and counter timer control. Software also includes A/D and D/A calibration procedures.

- Automatically configures to the display adapter, CPU, and mouse
- Sets the I/O base address
- Initializes the interrupt and DMA systems and D/A output
- Allocates base or extended memory
- Performs self-test and A/D-D/A calibration
- Configures A/D sample rate, frame rate, and sample counter
- Selects trigger mode and DMA or I/O block transfer
- Selects disk file output format to integer binary, float binary, or ASCII float
- Saves data to base memory, extended memory, or disk
- Full source code in "C" and assembly is available
- MS-DOS or WINDOWS version (visual "C" interface)

PC-414SRC Source code for PC-414SET, written in C.

PC-414WIN
PC-414NT A Windows 95/98 or NT GUI control panel incorporates all the functions of the PC-414. Functions include configuration and setup, analog input to file or disk, analog output, analog and digital triggering, digital I/O, and calibration.

PC-414WINS Source code for PC-414WIN written in Borland C Builder.

PC-414LV Bridge driver software to LabVIEW 4.0 and 3.1.

PC-414LVS Source code for PC-414LV allows users to reduce high level VI's to lower level VI's.

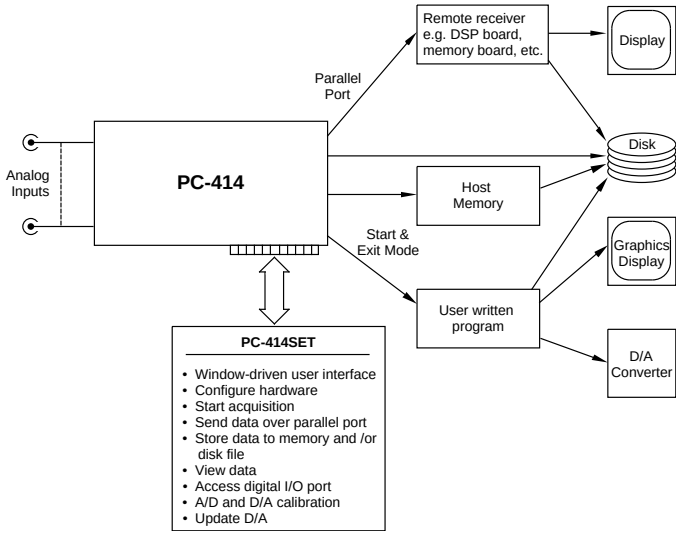

Figure 2. PC-414SET Software Operation

FUNCTIONAL SPECIFICATIONS

(Typical at +25 °C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	PC-414B	PC-414D	PC-414E	PC-414F
Number of Channels	4 (single A/D)	1 (single A/D)	16SE/8D [Note 8] (single A/D)	2 Simultaneous (two A/D's)
Input Configuration (non-isolated) [Note 19]	Single Ended	Differential	SE or Diff.	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1) [Notes 1 & 16]	0 to +10 V ±10 V ±5 V	±5 V	0 to +10 V ±10 V ±5 V	0 to +10 V ±5 V
Input Overvoltage (no damage, power on)	±15 V	±15 V	±15 V	±15 V
Overvoltage Recovery Time, maximum	2 µs	2 µs	2 µs	2 µs
Common Mode Voltage Range, maximum	—	±1 V	±10 V	—
Input Impedance [Notes 6 &10]	10 MΩ	2 kΩ	100 MΩ	1 kΩ
SAMPLE/HOLD				
Acquisition Time (FSR step to 0.01% of FSR, max.)	750 ns	50 ns	750 ns	165 ns
Aperture Delay	20 ns	10 ns	20 ns	20 ns
Aperture Delay Uncertainty	±100 ps	±7 ps	±40 ps	±40 ps
A/D CONVERTER				
Resolution	14 bits	12 bits	12 bits	12 bits
Conversion Period	1.6 µs	200 ns	500 ns	400 ns
SYSTEM DC CHARACTERISTICS [Note 7]				
Integral Non-linearity (LSB of FSR)	±1.5	±2	±1	±1
Differential Non-linearity (LSB of FSR)	±1	±1	±0.75	±1
Full Scale Temperature Coefficient (LSB per °C)	±0.3	±0.1	±0.1	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.3	±0.3	±0.1	±0.1
SYSTEM DYNAMIC PERFORMANCE [Note 2]				
Throughput to FIFO (single channel, gain = 1)	500 kHz	5 MHz [Note 9]	2 MHz	2 MHz
Throughput to FIFO (sequential channels, gain = 1)	330 kHz	—	500 kHz [Note 4]	2 MHz/chan. (2 chans.)
Total Harmonic Distortion [Note 3]	–75 dB	–68 dB	–72 dB	–70 dB

The PC-414J in short-cycled addressing is recommended in place of the PC-414A. Model PC-414E can substitute for the PC-414C.

ANALOG INPUTS	
Programmable Gains	See Note 1
Common Mode Rejection (DC - 60 Hz)	-80 dB (g = 100) (414E)
Addressing Modes	1. Single channel 2. Simultaneous sampling 3. Sequential with autosequenced addressing 4. Random addressing by host software

A/D CONVERTER	
Output Coding	Positive-true, right justified, straight bin. (unipolar) or right-justified 2's complement (bipolar) with sign extension thru bit 15
Trigger Sources (Software selectable)	1. Local Pacer frame clock 2. External TTL frame clock 3. Analog threshold comp.
A/D Sample Clock (software selectable)	1. Internal programmable 82C54 timer 2. Ext. TTL input, active low

Please read all notes carefully.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	PC-414G	PC-414H	PC-414J	PC-414K
Number of Channels	2 Simultaneous (two A/D's)	1 (single A/D)	8 Simultaneous A/D's [Note 8]	2 Simultaneous (two A/D's)
Input Configuration (non-isolated) [Note 19]	Single Ended	Differential	Single Ended	Limited Differential
Full Scale Input Ranges (user-selectable) (gain = 1) [Notes 1 & 16]	±5 V or 0 to +10 V (separate models)	±5 V (other ranges special order)	±5 V, ±10 V [Note 13]	0 to +10 V, ±5 V (separate models)
Input Overvoltage (no damage, power on)	±15 V	±15 V	±15 V	±15 V
Overvoltage Recovery Time, maximum	2 µs	1 µs	3 µs	—
Common Mode Voltage Range, maximum	—	±1 V	—	±1 V
Input Impedance [Notes 6 &10]	1 MΩ	2 kΩ	8 kΩ (bipolar)	1 kΩ
SAMPLE/HOLD				
Acquisition Time (FSR step to 0.01% of FSR, max.)	350 ns [Note 11]	35 ns	400 ns	50 ns
Aperture Delay	20 ns	±10 ns	—	10 ns
Aperture Delay Uncertainty	±70 ps	3 ps rms	—	±7 ps
A/D CONVERTER				
Resolution	14 bits	12 bits	12 bits	12 bits
Conversion Period	500 ns	100 ns	2 µs [Note 12]	200 ns
SYSTEM DC CHARACTERISTICS [Note 7]				
Integral Non-linearity (LSB of FSR)	±1.5	±1.5	±1	±2
Differential Non-linearity (LSB of FSR)	±1	±1	±1	±1
Full Scale Temperature Coefficient (LSB per °C)	±0.3	±1	[Footnote 10]	±0.1
Zero or Offset Temperature Coefficient (LSB per °C)	±0.3	±1	[Footnote 10]	±0.3
SYSTEM DYNAMIC PERFORMANCE [Note 2]				
Throughput to FIFO (single channel, gain = 1)	1 MHz	10 MHz	400 kHz	5 MHz
Throughput to FIFO (sequential channels, gain = 1)	1 MHz/chan. (2 chans.)	—	250kHz/chan.**	5 MHz/ch.
Total Harmonic Distortion [Note 3]	–80 dB	–65 dB	–75 dB	–68 dB

**A 380 KHz per channel option is available on special order.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, gain = 1, unless noted)

ANALOG INPUTS	PC-414L	PC-414M	PC-414N	PC-414P
Number of Channels	16 Simultaneous A/D's	4 Simultaneous A/D's	2 Simultaneous A/D's	4 Simultaneous A/D's
Input Configuration (non-isolated) [Note 19]	Single Ended	Single Ended	Single Ended	Single Ended
Full Scale Input Ranges (user-selectable) (gain = 1) [Notes 1 & 16]	±5 V, ±10 V, (user selectable) [Note 13]	±10 V	±2.5 V	±2.5 V or 0 to +5 V (user selectable)
Input Overvoltage (no damage, power on)	±15 V	±12 V	±15V	±7 V
Overvoltage Recovery Time, maximum	—	—	—	—
Common Mode Voltage Range, maximum	—	—	—	—
Input Impedance [Notes 6 &10]	8 kΩ	10 MΩ	10 MΩ or 50 Ω	1000 Ω
SAMPLE/HOLD				
Acquisition Time (FSR step to 0.01% of FSR, max.)	400 ns	—	35 ns	—
Aperture Delay	—	—	±10 ns	—
Aperture Delay Uncertainty	—	—	5 ps	—
A/D CONVERTER				
Resolution	12 bits	16 bits	14 bits	14 bits
Conversion Period	2 µs [Note 12]	5 µs [Note 12]	200 ns [Note 12]	400 ns [Note 12]
SYSTEM DC CHARACTERISTICS [Note 7]				
Integral Non-linearity (LSB of FSR)	±2	±4	±1	±3
Differential Non-linearity (LSB of FSR)	±1	±3	±1	±1.5
Full Scale Temperature Coefficient (LSB per °C)	[Note 10]	±1	±0.5	±0.5
Zero or Offset Temperature Coefficient (LSB per °C)	[Note 10]	±1	±0.5	±0.5
SYSTEM DYNAMIC PERFORMANCE [Note 2]				
Throughput to FIFO (single channel, gain = 1)	400 kHz	200 kHz	5 MHz	3 MHz* min.
Throughput to FIFO (sequential channels, gain = 1)	190 kHz/chan.	200 kHz/chan.	5 MHz/chan.	2.5 MHz/chan.
Total Harmonic Distortion [Note 3]	-75 dB	-83 dB	-75 dB	-75 dB

* The sample rate to published specifications is 3 MHz. The A/D is functional to 5 MHz. Valid data output per channel is delayed by 4 samples after the start of the sample clock. Please make note of this for products such as the PC-414P, PC-430P, and DVME-614P which use non-continuous A/D sampling. Data output is pipelined meaning that the first four samples per channel should be discarded. For all 4 channels, discard 16 samples. The design is intended for semi-continuous sampling of wideband signals and is less suitable for low speed data acquisition. Approximately 5 dB SFDR improvement can be achieved by directly connecting an external A/D sample clock. Contact DATEL for details.

SPECIFICATIONS, CONTINUED

(Typical @ +25°C, dynamic conditions, unless noted)

A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024, 4096, or 16,384 A/D samples. 64 K on request.
TRIGGER CONTROL	
Programmable Interval Timer Type	82C54
Functions	1. A/D sample count reached 2. A/D start rate (16 bit divisor) 3. SSH sample counter (414A)
Pacer Sample Counter	3 to 65,536 samples. Drives the Acquire flag/interrupt gate for A/D start pulses.
82C54 Clock Source	Internal 8 MHz crystal clock
Scan Trigger Clock	125, 250, or 500 KHz
Analog Trigger Input Range [Note 5]	±10 V (not avail. 414D)
Analog Trigger Response	2 µs to set status flag
Analog Trigger Hysteresis	40 mV
ANALOG OUTPUT	
Number of Channels	One
Function (user-selectable) [Note 5]	1. General purpose analog output 2. Threshold comparator for A/D trigger
Resolution	12 bits
Output Voltage Range (user-selectable)	0 to +10 V, ±5 V and ±10 V at 5 mA max.
Linearity	±0.05% of FSR
Settling Time (10 V step)	5 microseconds to 0.05%
Input Coding (user-selectable)	Same as A/D section
ISA BUS INTERFACE	
Architecture	I/O mapped, pluggable to IBM-PC/AT, and compatibles. Decodes eight 16-bit I/O registers.
I/O Mapping	Decodes I/O address lines A9 - A0
Data Transfer	I/O transfer or host DMA, software selectable
Data Bus	16 bits
Direct Memory Access	1 channel, selectable on channels 5, 6, or 7, set by software
DMA Request Conditions (software selectable)	FIFO full, half full, not empty, scan acquire flag (sample count reached)
Control/Status Functions	Board reset, FIFO flags, interrupt select and status, DMA select and status, trigger source, timer control and period, sample count load, parallel outport enable, A/D enable, MUX auto-sequence
Number of Interrupts (software selectable)	1 interrupt, software selectable on level 7, 9 thru 11, or 15.
Bus Interrupt Sources	Scan acquire flag (sample count), FIFO full or half full, DMA terminal count from bus.
PARALLEL DATA PORT	
Outport Type	16 data output lines, TTL levels from A/D FIFO. Includes handshake signals and FIFO flags. The outport does not provide addressing.
Operating Modes	Asynchoronous master to external slave receiver. 4 modes are included, offering internal/external clocking (to 10 MHz), synchronous/ asynchronous handshaking. Sequencing is compatible with DT Connect®.
Parallel Port Loading	24 mA out, 1.6 mA in. The data outputs may be tri-stated for shared bus connection.
Parallel Port Connector	2-row 26-pin header type mounted on board interior. 0.100" pin spacing suitable for flat cable. Pinout is compatible with DT Connect® and existing 414 format.
Port Data Rate	4 MHz max. Data may be transferred up to 10 MHz with external clocking.
DIGITAL I/O PORT	
Connector	Dual row, 26-pin header mounted on board interior. Uses 0.100" pin spacing suitable for flat cable. Includes +5 Vdc and digital ground connections.
Configuration	8 digital outputs, 8 digital inputs (unlatched)
Levels	Buffered, TTL levels. 10 output loads.
Outport Settling Time	50 ns max. after write operation
MISCELLANEOUS	
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on PC-414F, G, H, K, M, N, and P. A single offset and gain pot is provided on PC-414B, D, and E. Recommended recalibration interval is 90 days in stable conditions.
Analog Input Connectors	Four SMA miniature coaxial, mounted on rear slot. [Note 8]

Multipurpose Connector [Note 8]	5th SMA user-selectable for: 1. Pacer trigger input 2. Analog threshold comparator input
Operating Temp. Range	0 to +60°C, forced cooling recommended.
Storage Temp. Range	-25 to +85°C
Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Power Required	+5V @ 3.5A max. from ISA bus
Outline Dimensions	4.5 x 10.5 x 0.625 inches, compatible to PC/ISA bus

NOTES

1. Resistor-programmed gain from x1 to x100 is available on PC-414E with increased settling delay at higher gain.

2. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion, and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

3. THD test conditions are:
   A. Input freq. 500 kHz (414F) 200 kHz (414B,E,G) 50 kHz (414J,L,M) 1 MHz (414D,K,N,P) 2 MHz (414H)
   B. Generator/filter THD is -90 dB minimum.
   C. THD computed by FFT to 5th harmonic.
   $$THD = 20 \left(\log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{Vin} \right)$$
   D. Inputs are half full scale less 0.5 dB. No channel advance.
   E. A/D sample rate = 500 kHz (414B,E,G), 4 MHz (414D,K), 2 MHz (414F), 10 MHz (414H), 250 kHz (414J), 190 kHz (414L,M), 2.5 MHz (414P)

4. The rates shown for sequential sampling are the maximum A/D converter start rates and include MUX sequencing and settling. For example, if four channels of the PCI-414E were scanned, the maximum sample rate on any one channel would be 2 µs x 4 channels = 8 µs (125 kHz per channel).

5. For fastest response on the analog comparator trigger, keep the reference voltage near the trip input voltage. To avoid overload recovery delays, do not let the trip input (or any other analog input) exceed ±10V.

6. The input impedance of 10 MΩ minimum avoids attenuation errors from external input source resistance. For many applications, an in-line coaxial 50 Ω shunt, inserted adjacent to the front connectors, is recommended to reduce reflections and standing wave errors.

7. Allow 20 minutes warmup time to rated specifications for models PC-414B,G,M,N.

8. A 25-pin DB-25S connector is used for the PC-414E, J, and L.

9. 5 MHz sampling on PC-414D requires an external clock. Maximum on-board sampling is 4 MHz.

10. Input impedance is shown with power on. Impedance with power off is 1.5 kΩ or less.

11. PC-414G acquisition time is 350 ns to ±0.01% of FSR.

12. All channels in simultaneous sampling.

13. PC-414J and L bipolar input is user-selectable ±5 V or ±10 V per channel (default). Total full scale error over temperature range is ±4 LSB maximum. Total zero/offset error over temperature range is ±2 LSB maximum. Monotonicity: no missing codes over temperature range.

14. Avoid mixing external triggers which are a close submultiple of the internal A/D start clock to prevent lost samples.

15. Models PC-414D, H, K, and M use a single channel 12-bit A/D converter with ±5 V inputs. An external A/D clock is required above 4 MHz and the 82C54 timer must be bypassed. 10 MHz sampling may continue until the FIFO memory is full.

16. Input polarity. Some models are fixed as bipolar only whereas others are user-selectable unipolar or bipolar. Still others require separate model numbers.

17. Models F, G, J, K, L, M, N, and P use one A/D converter per channel.

18. The customer must use shielded cables to insure EMC compliance.

19. A/D-per-channel boards (models F, G, J, K, L, M, N, P) may be operated in “software differential” mode. Two A/D’s are applied to the high and low legs of a single differential input channel. The two data values are then algebraically subtracted, either on the fly in real time or after all samples have been stored. Channel capacity in “software differential” is one-half the number of single-ended channels.

    This technique offers excellent bandwidth, high common mode rejection and optional mix of single-ended and differential channels.

I/O Register Mapping

The base address may be selected anywhere up to 3F0h on 16-byte boundaries.

I/O Address (hex)	Direction	Description
Base + 0	Write	Command Register
Base + 0	Read	Status Register
Base + 2	Write	Channel Address/Digital Output [Note 12]
Base + 2	Read	Digital Input Register [Note 12]
Base + 4	Write	D/A Data Register
Base + 6	Write	FIFO Reset Register
Base + 6	Read	FIFO A/D Data Register
Base +8	Read/Write	Counter #0 (82C54)
Base + 0Ah	Read/Write	Counter #1 (82C54)
Base + 0Ch	Read/Write	Counter #2 (82C54)
Base + 0Eh	Read/Write	Control Register (82C54)

Transfer Speeds

ISA bus transfer rates are host-dependent and should be determined by testing. For example, a Compaq computer achieved 800 nanoseconds instantaneous sample-to-sample timing to base memory using the REP INSW instruction. A faster CPU will not increase the ISA bus speed. To optimize throughput, disable all possible interrupts. For higher speed continuous (non-stop) A/D sampling, consider using a parallel port.

FIFO Data Format

A/D data is delivered as a stream from the FIFO memory. For multichannel inputs, this means that data is multiplexed. For example, for 4-channel inputs, the output channel sequence is 0, 1, 2, 3, 0, 1, . . . Some applications may need this data de-multiplexed by software so that each channel's data is placed in its own separate buffer.

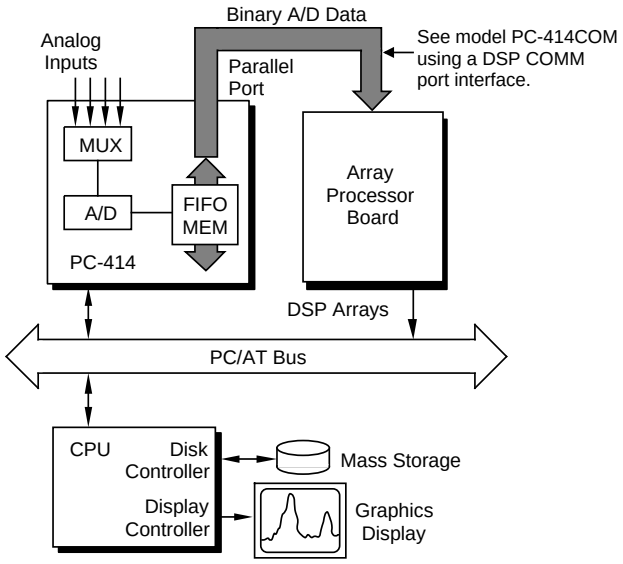

Figure 3. Array Preprocessing

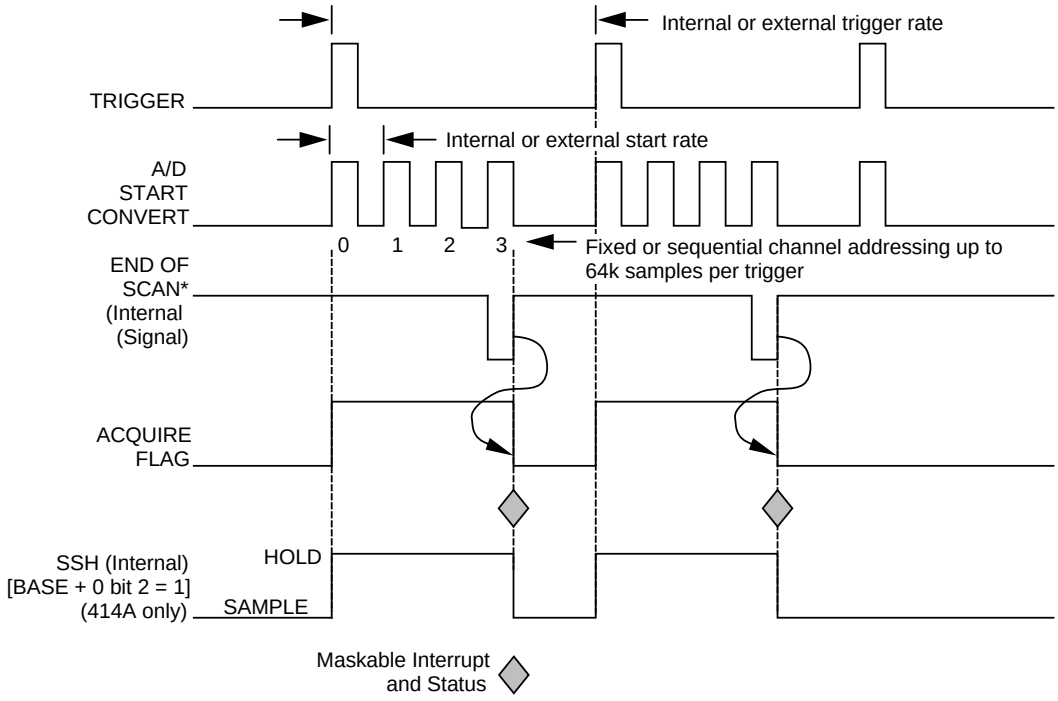

Figure 4. PC-414 Timing Diagram

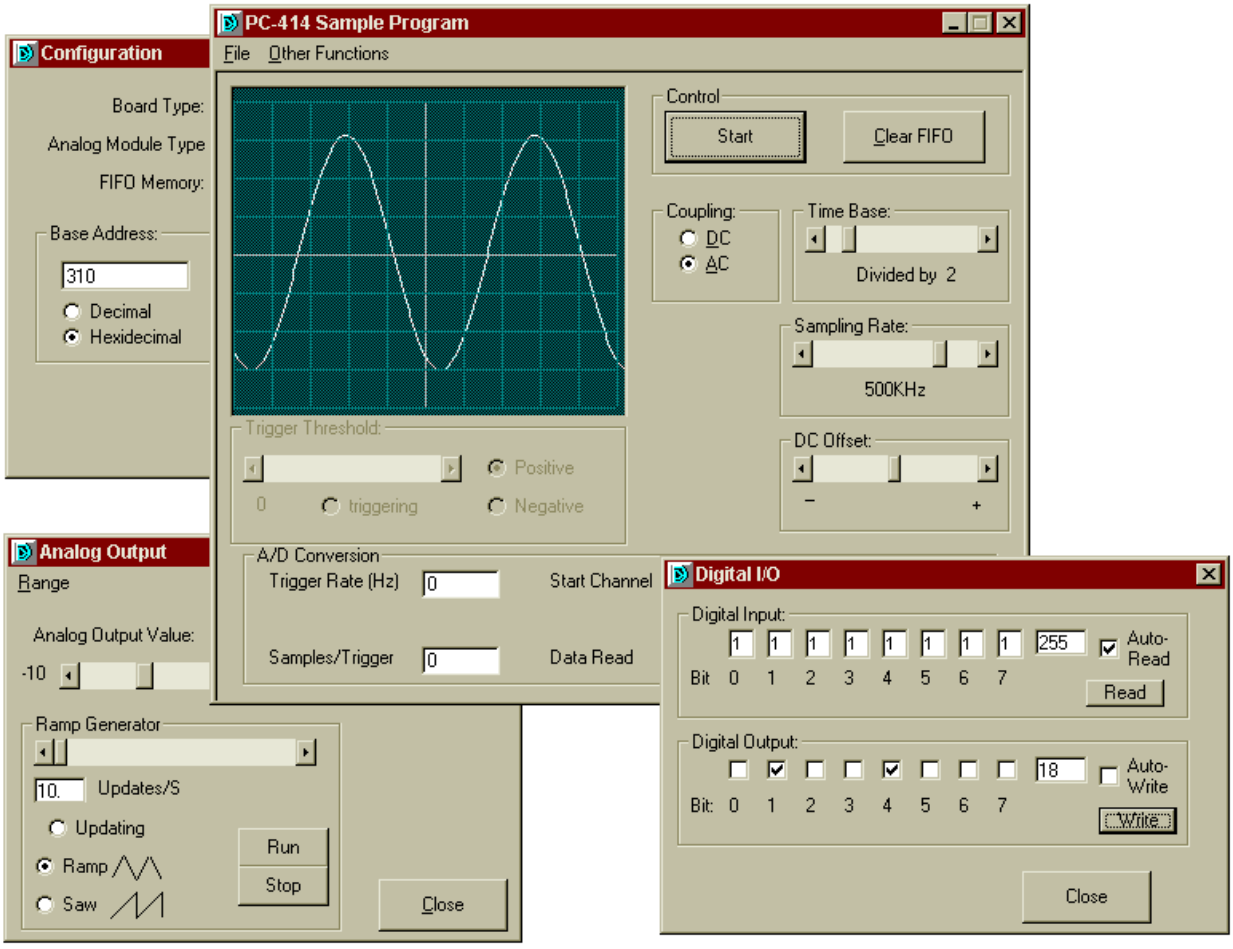

Figure 5. PC-414VB-CONSOLE

PC-414VB CONSOLE

This example application was written in Visual Basic 5.0, using the PC-414LVS as the callable DLL. Created by Eiichi Itagaki, Software Engineer of DATEL KK Technical and Jeffrey Greenberg, Marketing Applications Engineer DATEL, Inc. USA.

For users preferring to create applications in Visual Basic, the DLL and source code found in the PC-414LVS offers the Visual Basic programmer a wealth of information and tools in creating applications quickly and easily. The PC-414VB-CONSOLE is a sample program showing how to implement most of the functions of the PC-414 Series. Included is the source code for all the forms and the code modules.

To receive your ***FREE*** copy of **PC-414VB-CONSOLE**, purchase PC-414LVS with any PC-414 Series board and contact DATEL at 1-800-233-2765.

Example Declarations:

```
Declare Sub SetIOBase Lib “P414LV32.DLL” (ByVal io_base_address As Integer)
Declare Sub init_414 Lib “P414LV32.DLL” (ByVal fsize As Integer, ByVal port As Integer, ByVal trigger_src As Integer,
                ByVal trigger_pol As Integer, ByVal clock_src As Integer, ByVal md As Integer)
Declare Sub set_mode Lib “P414LV32.DLL” (ByVal samples_trigger As Integer, ByVal scan_enable As Integer, ByVal scan_count
                As Integer, ByVal auto_incr As Integer, ByVal cahnnel As Integer, ByVal sample_rate As Long,
                ByVal trigger_rate As Long)
Declare Sub StartAD Lib “P414LV32.DLL” ()
Declare Sub StopAD Lib “P414LV32.DLL”()
Declare Function read_status_reg Lib “P414LV32.DLL” () As Integer
Declare Sub get_status_flags Lib “P414LV32.DLL” (half_full_f As Long, full_f As Long, empty_f As Long, acquire_f As Long)
Declare Sub reset_fifo_reg Lib “P414LV32.DLL” ()
Declare Sub read_FIFO Lib “P414LV32.DLL” (ByVal count As Integer, buffer As Integer)
```

PC-414LV FEATURES

- **Supports DATEL's PC-414 family of high-speed analog input boards**
- **Runs under Microsoft Windows®, uses Dynamic Data Exchange (DDE)**
- **Adaptable to all LabVIEW applications**
- **Easy-to-use visual programming eliminates low level software**
- **Interactive, customizable front panel controls**
- **Integrates data acquisition, processing, display, and storage**
- **A/D sampling rates to 10 MHz**
- **Optional multi-channel simultaneous sampling**

PC-414LV GENERAL DESCRIPTION

National Instruments' LabVIEW transforms the PC-414 family of high speed analog input boards into easy-to-use virtual instruments (VI's) that acquire, analyze, display, and store analog signals in real time. Low level software development is replaced by an intuitive visual programming system that harnesses all the power of Microsoft Windows - graphic user interface (GUI), access to more host memory (16 megabytes), multi-tasking, and inter-process communications using DDE. Applications include highly concurrent system testing, process monitoring and control, telemetry, radar, sonar, acoustics, DSP front end quantizer, education, and research.

The PC-414 LabVIEW package from DATEL consists of a set of inexpensive VI's for low level control of the board. These integrate into the LabVIEW package which the user must purchase from National Instruments. Once installed, these VI's appear as icons on the LabVIEW menues. DATEL's VI's are offered in two versions. Model PC-414LV is the executable binary-only configuration which can be fully integrated into the user-written block diagram. Model PC-414LVS is the full source to model PC-414LV and also includes all binaries. The source code should be considered by a programmer who wishes to extend or modify the existing VI's or just wants to more fully understand their operation.

LabVIEW's feature-rich program development system combined with DATEL's library of VI functions for the PC-414 provide the essential building blocks to create any conceivable LabVIEW applications.

Graphical programming works like a flowchart - when the flowchart is accurate and complete, the program is done. PC-414LV off-loads as much programming as possible into the LabVIEW environment so the user has maximum control. It creates a library of fast, simple, highly modular VI functions for the PC-414 that do not sacrifice board performance. The user builds VI's to configure the data acquisition hardware, process the data, and ultimately display and store that data without writing programs. Similar VI's can be created to update the analog output and to read and write the digital I/O port.

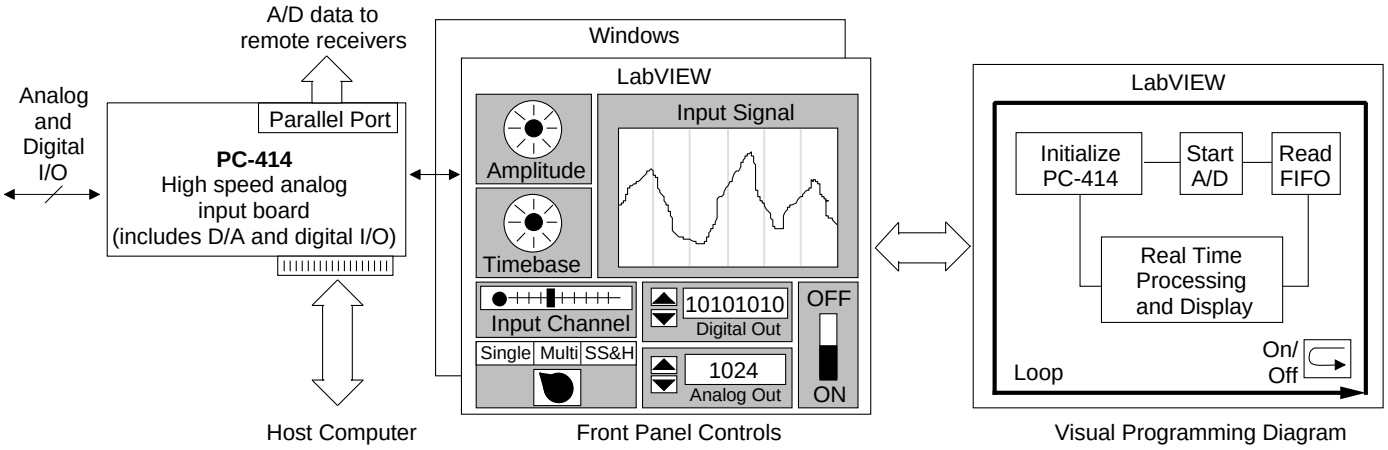

Figure 6. PC-414LV LabVIEW System Diagram

All VI's are assembled graphically using a mouse and can be edited at any time to modify functionality or appearance. Non-stop, seamless data acquisition continues on the PC-414 while LabVIEW simultaneously maintains the GUI and handles the A/D data stream in real time. Easily customized, interactive user interfaces can be created from the vast library of front panel controls and displays offered by LabVIEW.

The PC-414LV includes extensive Dynamic Linked Library (DLL) functions that perform the PC-414 low level hardware control and monitor operations transparently. The software provides VI functions that poll PC-414 status flags independent of, and simultaneous with, data acquisition and data transfer. Control is retained by the user as long as LabVIEW continues to execute correctly. The multi-window, visual programming environment facilitates building and accessing hierarchical VI programs. Multi-tasking allows context switches to other concurrent Windows applications without disrupting PC-414 operation or control.

The PC-414/LabVIEW system optimizes two concurrent processes - the PC-414 acquiring data while LabVIEW further processes or stores the uploaded data stream. The entire PC-414/LabVIEW combination uses only a few VI functions that are easy to understand and incorporate into a "block diagram" program. The basic concept is to initialize the PC-414 hardware, reset the FIFO memory, start data acquisition, and upload blocks of data from the FIFO to LabVIEW memory buffers on the host - or to remote receivers over the DT Connect I compatible output port. These data blocks can then be further processed as screen displays, indicators, graphs, sent to printers or plotters, or simply archived to disk file for later analysis. The A/D continues running and no data will be lost as long as LabVIEW uploads the A/D data faster than the data is being acquired.

Virtual Instrument Library

In summary, PC-414LV includes the following VI functions:

PC-414 Initialize	Initialize the PC-414 hardware - board model, I/O base address, etc.
Operating Mode	Specify A/D trigger rate, A/D sample rate, and analog input channel.
Clear FIFO	Reset the FIFO memory
Start/Stop A/D	Enable and disable the A/D.
Read Status	Read hardware status flags - FIFO flags, acquisition done, oversampling.
Read FIFO	Read blocks of A/D data from the FIFO on the PC-414 and fill a LabVIEW buffer on the host.
Write DAC	Update the analog output channel.
Inport/Outport	Read/write the 8-bit digital I/O port.
PC-414 Demo	Complete data acquisition demonstration VI, includes real time signal display.
Demultiplex Buffers	Unravel a multi-channel data buffer and extract data from one channel only.

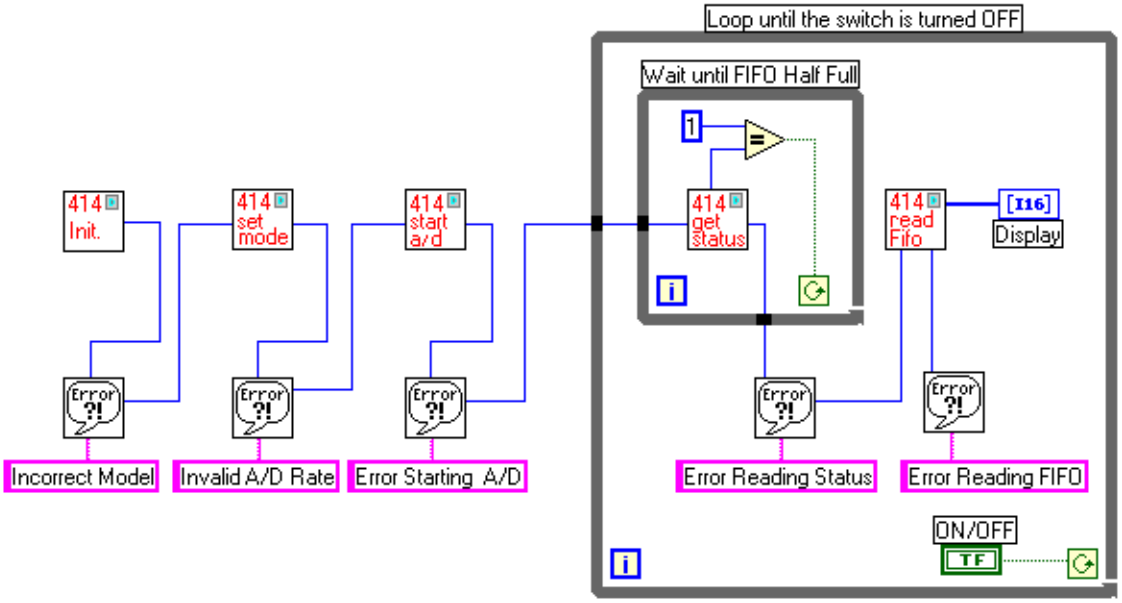

Figure 7. PC-414LV Visual Program

ORDERING INFORMATION

Hardware:

PC-414 ____ ____ ____

Input Channels, A/D Resolution

B = 4SE chans., 14 bits	J = 8SE simul. chans., 12 bits
D = 1D chan., 12 bits	K = 2SE simul. chans., 12 bits
E = 16SE/8D chans., 12 bits	L = 16SE simul. chans., 12 bits
F = 2SE simul. chans., 12 bits	M = 4SE simul. chans., 16 bits
G = 2SE simul. chans., 14 bits	N = 2SE simul. chans., 14 bits
H = 1D chan., 12 bits	P = 4SE simul. chans., 14 bits

FIFO Memory Size

1 = 1,024 A/D samples
2 = 4,096 A/D samples
3 = 16,384 A/D samples

Input Polarity

A = Bipolar or selectable
B = Unipolar
For models with user-selectable polarity use the "A" designator. CAUTION: Read the input range specifications carefully.

Example: PC-414F3 Two simultaneous A/D's, 2 MHz, 12-bit resolution, 16,384 FIFO samples.

61-7342340	SMA male to BNC male coaxial cable, 1 meter length. One cable required per channel.
PC-490B	DB-25 screw termination adapter (cable not included). Not recommended for high-frequency signals.
PC-414xCOMx	PC-414 with DSP COMM port interface. See PC-414COM data sheet.

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. An example program disk is available on request at no charge.

Software:

PC-414SET	Setup/configuration data-collection program for MS-DOS. Executables only.
PC-414SRC	Source code for setup and configuration program on MS-DOS disks. Includes "C" and assembly source code and window driver library. Documentation is on disk.
PC-414WIN	Setup/configuration program for Microsoft Windows 3.1. Executables only.
PC-414WINS	Source code for PC-414WIN, written with Borland Delphi.
PC-414LV	Bridge driver software to National Instruments' LabVIEW®. See PC-414LV data sheet.
PC-414LVS	Source code for PC-414LV
PC-414NT	Setup/configuration program for Microsoft Windows NT. Executables only.
PC-414NTS	Source code for PC-414NT, written with Borland Delphi.
Call DATEL	Free example programs for the PC-414, written in Visual Basic 5. Contact Systems Application Dept.
Call DATEL	Free example programs for the PC-414, written in Microsoft QuickBASIC. Contact System Application Dept.