élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2140C/2141C

150 MHz Differential Twisted Pair Driver

Features

- Fully differential inputs, outputs, and feedback
- Differential input range ±2.3V
- 150 MHz 3 dB bandwidth
- 800 V/μs slew rate
- −55 dB distortion at 3 MHz
- −75 dB distortion at 100 kHz
- ±5V supplies or +6V single supply
- 50 mA minimum output current
- Output swing (200Ω load) to within 1.5V of supplies (14V pk-pk differential)
- Low power-11 mA typical supply current

Applications

- Twisted pair driver
- Differential line driver
- VGA over twisted pair
- ADSL/HDSL driver
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2140CN	−40°C to +85°C	8-pin PDIP	MDP0031
EL2140CS	−40°C to +85°C	8-pin SOIC	MDP0027
EL2141CN	−40°C to +85°C	8-pin PDIP	MDP0031
EL2141CS	−40°C to +85°C	8-pin SOIC	MDP0027

General Description

The EL2140C/2141C is a very high bandwidth amplifier whose output is in differential form, and is thus primarily targeted for applications such as driving twisted pair lines, or any application where common mode injection is likely to occur. The input signal can be in either single-ended or differential form, but the output is always in differential form.

On the EL2141C, two feedback inputs provide the user with the ability to set the device gain, (stable at minimum gain of two), whereas the EL2140C comes with a fixed gain of two.

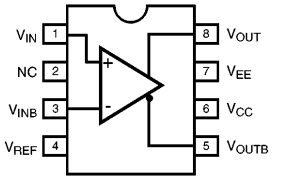
The output common mode level is set by the reference pin (V_{REF}), which has a −3 dB bandwidth of over 100 MHz. Generally, this pin is grounded, but it can be tied to any voltage reference.

The transmission of ADSL/HDSL signals requires very low distortion amplification, so this amplifier was designed with this as a primary goal. The actual signal distortion levels depend upon input and output signal amplitude, as well as the output load impedance. (See distortion data inside.)

Both outputs (V_{OUT}, V_{OUTB}) are short circuit protected to withstand temporary overload condition.

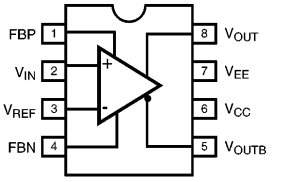
Connection Diagrams

EL2140C



2140-1

EL2141C



2140-2

Absolute Maximum Ratings

Supply Voltage (V_{CC}–V_{EE})	0V–12.6V	Recommended Operating Temperature	−40°C to 85°C
Maximum Output Current	±60 mA	V_{IN}, V_{INB}, V_{REF}	V_{EE} + 0.8V (MIN) to V_{CC} − 0.8V (MAX)
Storage Temperature Range	−65°C to +150°C	V_{IN}–V_{INB}	±5V
Operating Junction Temperaure	+150°C		

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics

V_{CC} = +5V, V_{EE} = −5V, T_A = 25°C, V_{IN} = 0V, R_L = 200, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
V_{supply}	Supply Operating Range (V_{CC}–V_{EE})	±3.0	±5.0	±6.3	I	V
I_S	Power Supply Current (No Load)		11	14	I	mA
V_{OS}	Input Referred Offset Voltage	−25	10	40	I	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB}, V_{REF})	−20	6	20	I	µA
Z_{IN}	Differential Input Impedance		400		V	kΩ
V_{DIFF}	Differential Input Range	±2.0	±2.3		I	V
A_V	Voltage Gain (EL2140C) V_{IN} = $2V_{pk-pk}$	1.95	1.985	2.02	I	V/V
A_{VOL}	Open Loop Voltage Gain (EL2141C)		75		V	dB
V_{CM}	Input Common Mode Voltage Range (EL2140C)	−2.6		+4.0	I	V
V_{OUT}(200)	Output Voltage Swing (200Ω load, V_{OUT} to V_{OUTB}) (EL2141C)	±3.4	±3.6		I	V
V_{OUT}(100)	Output Voltage Swing (100Ω Load, V_{OUT} to V_{OUTB}) (EL2141C)	±2.9	±3.1		I	V
V_N	Input Referred Voltage Noise		36		V	nV/√ Hz
V_{REF}	Output Voltage Control Range (EL2140C)	−2.5		+3.3	I	V
V_{REFOS}	Output Offset Relative to V_{REF}	−60	−25	+60	I	mV
PSRR	Power Supply Rejection Ratio	60	70		I	dB
I_{OUT}(min)	Minimum Output Current	50	60		I	mA
CMRR	Input Common Mode Rejection Ratio (EL2140C) V_{CM} = ± 2V	60	70		I	dB
R_{OUT}	(V_{OUT} = V_{OUTB} = 0V) Output Impedence		0.1		V	Ω

TD is 0.3in

TD is 3.7in

AC Electrical Characteristics

V_{CC} = +5V, V_{EE} = −5V, T_A = 25°C, V_{IN} = 0V, R_{LOAD} = 200, unless otherwise specified

Parameter	Description	Min	Typ	Max	Test Level	Units
BW(−3 dB)	−3 dB Bandwidth (EL2140C and EL2141C @ gain of 2)		150		V	MHz
SR	Differential Slewrate		800		V	V/µs
Tstl	Settling Time to 1%		15		V	ns
GBW	Gain Bandwidth Product		400		V	MHz
V_{REFBW}(−3 dB)	V_{REF} −3 dB Bandwidth		130		V	MHz
V_{REFSR}	V_{REF} Slewrate		100		V	V/µs
THDf1	Distortion at 100 kHz (Note 1)		−75		V	dB
dP	Differential Phase @ 3.58 MHz		0.16		V	°
dG	Differential Gain @ 3.58 MHz		0.24		V	%

Note 1: Distortion measurement quoted for V_{OUT}–V_{OUTB} = 12V pk-pk, R_{LOAD} = 200Ω, Vgain = 8.

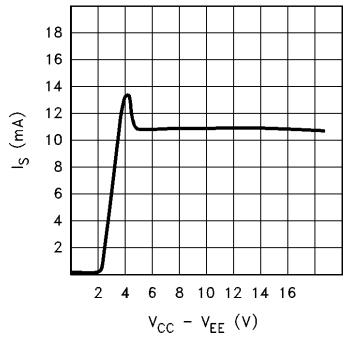
Pin Description

Pin No. EL2140C	Pin No. EL2141C	Pin Name	Function
1	2	V_{IN}	Non-inverting Input
3		V_{INB}	Inverting Input (EL2140C only)
	1	FBP	Non-inverting Feedback Input. Resistor R1 must be Connected from this Pin to V_{OUT}. (EL2141C only)
	4	FBN	Inverting Feedback Input. Resistor R3 must be Connected from this pin to V_{OUTB}. (EL2141C only)
4	3	V_{REF}	Output Common-mode Control. The Common-mode Voltage of V_{OUT} and V_{OUTB} will Follow the Voltage on this Pin. Note that on the EL2141, this pin is also the V_{INB} pin.
5	5	V_{OUTB}	Inverting Output
6	6	V_{CC}	Positive Supply
7	7	V_{EE}	Negative Supply
8	8	V_{OUT}	Non-inverting Output

TD is 2.0in

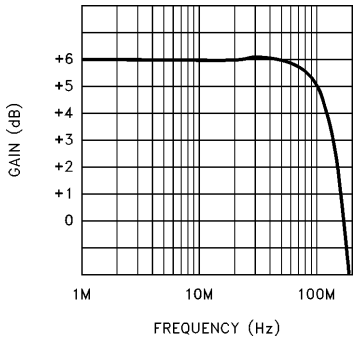
Typical Performance Curves

I_S vs Supply Voltage



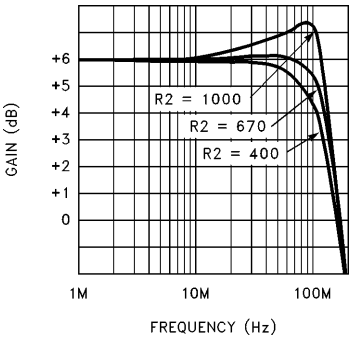
2140-3

EL2140 Frequency Response



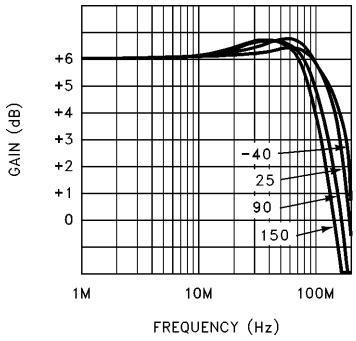
2140-4

EL2141 Frequency Response vs Resistor R2 (GAIN = 2)



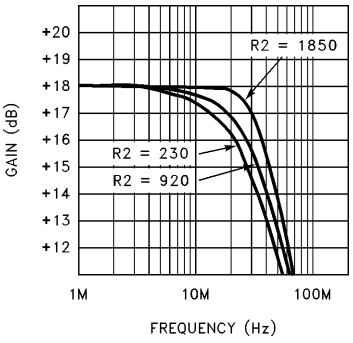
2140-5

Frequency Response vs Temperature



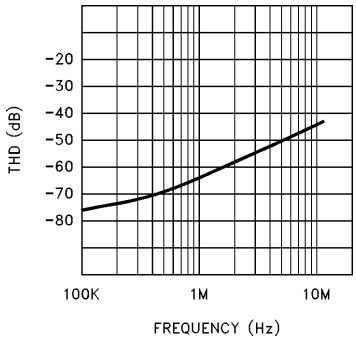
2140-6

EL2141 Frequency Response vs Resistor R2 (GAIN = 8)



2140-7

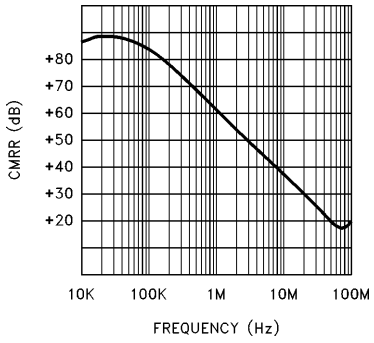
EL2141 Distortion vs Frequency (GAIN = 6, R_{LOAD} = 200Ω) V_{IN} = 2V pk/pk



2140-8

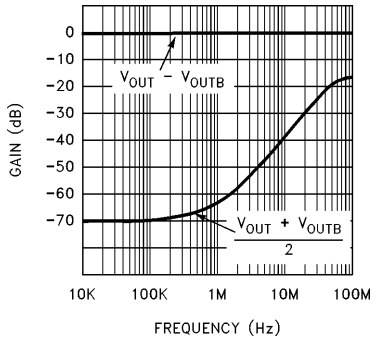
Typical Performance Curves — Contd.

EL2140 CMRR vs Frequency



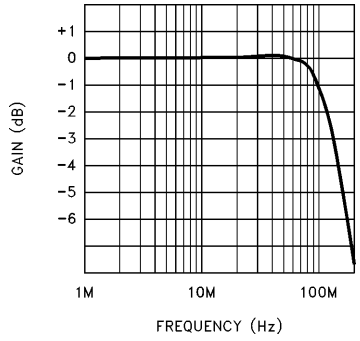
2140-9

EL2141 Output Signal and Common Mode Signal vs Frequency

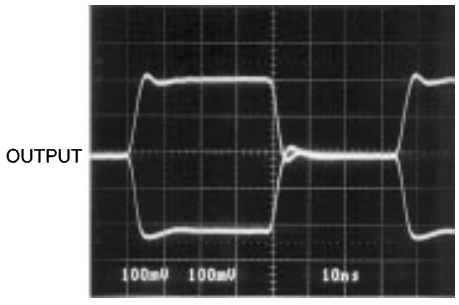


2140-10

EL2140 V_{REF} Frequency Response



2140-11



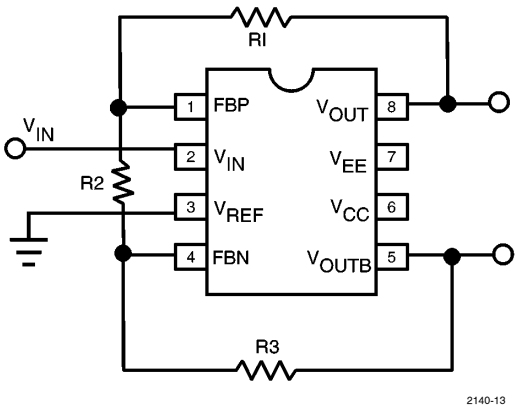
2140-12

EL2140 Small Signal Response (Note 1)

Note 1: Photo shows voltages on a 100Ω transmission line terminated at both ends, so voltages at V_{OUT}, V_{OUTB} are twice the values shown.

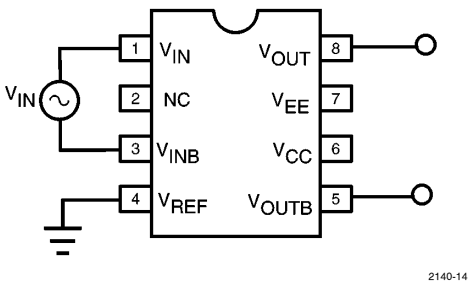
Applications Information

EL2141C



$$\text{GAIN} = \frac{R1 + R2 + R3}{R2}$$

EL2140C



GAIN = 2

$$\frac{V_{OUT} + V_{OUTB}}{2} = V_{REF}$$

(common mode)

Choice of feedback resistor

There is little to be gained from choosing resistor R2 values below 400Ω and, in fact, it would only result in increased power dissipation and signal distortion. Above 400Ω, the bandwidth response will develop some peaking (for a gain of two), but substantially higher resistor R2 values may be used for higher voltage gains, such as up to 2 kΩ at a gain of eight before peaking will develop. R1 and R3 are selected as needed to set the voltage gain, and while R1 = R3 is suggested, the gain equation above holds for any values (see distortion for further suggestions).

Capacitance considerations

As with many high bandwidth amplifiers, the EL2140C/2141C prefer not to drive highly capacitive loads. It is best if the capacitance on V_{OUT} and V_{OUTB} is kept below 10 pF if the user does not want gain peaking to develop.

In addition, on the EL2141C, the two feedback nodes FBP and FBN should be laid out so as to minimize stray capacitance, else an additional pole will potentially develop in the response with possible gain peaking.

The amount of capacitance tolerated on any of these nodes in an actual application will also be dependent on the gain setting and the resistor values in the feedback network.

Distortion considerations

The harmonics that these amplifiers will potentially produce are the 2nd, 3rd, 5th, and 6th. Their amplitude is application dependent. All other harmonics should be negligible by comparison. Each should be considered separately:

H2 The second harmonic arises from the input stage, and the lower the applied differential signal amplitude, the lower the magnitude of the second harmonic. For practical considerations of required output signal and input noise levels, the user will end up choosing a circuit gain. Referring to Figure 1, it is best if the voltage at the negative feedback node tracks the V_{REF} node, and the voltage at the positive feedback node tracks the V_{IN} node respectively. This would theoretically require that R1 + R2 = R3, although the lowest distortion is found at about R3 = R1 + (0.7*R2). With this arrangement, the second harmonic should be suppressed well below the value of the third harmonic.

Applications Information — Contd.

H3 The third harmonic should be the dominant harmonic and is primarily affected by output load current which, of course, is unavoidable. However, this should encourage the user not to waste current in the gain setting resistors, and to use values that consume only a small proportion of the load current, so long as peaking does not occur. The more load current, the worse the distortion, but depending on the frequency, it may be possible to reduce the amplifier gain so that there is more internal gain left to cancel out any distortion.

H5 The fifth harmonic should always be below the third, and will not become significant until heavy load currents are drawn. Generally, it should respond to the same efforts applied to reducing the third harmonic.

H6 The sixth harmonic should not be a problem and is the result of poor power supply decoupling. While 100 nF chip capacitors may be sufficient for some applications, it would be insufficient for driving full signal swings into a twisted pair line at 100 kHz. Under these conditions, the addition of 4.7 μF tantalum capacitors would cure the problem.

Typical Applications Circuits

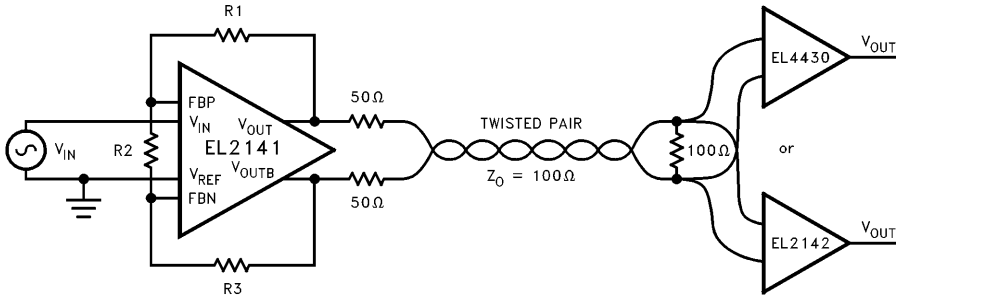


Figure 1. Typical Twisted Pair Application

Typical Applications Circuits — Contd.

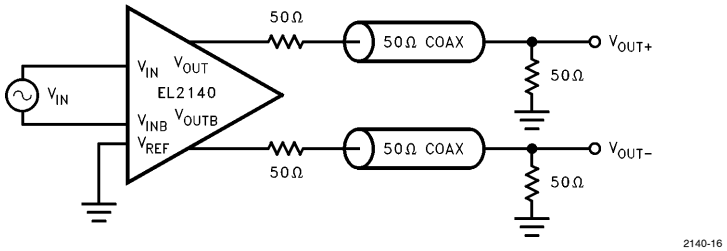


Figure 2. Dual Coaxial Cable Driver

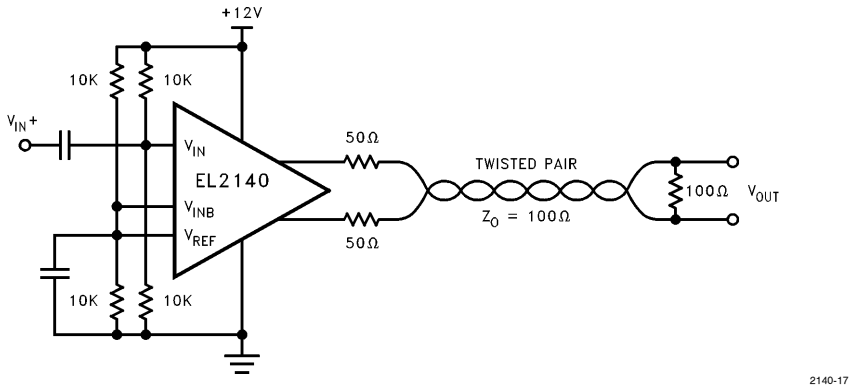


Figure 3. Single Supply Twisted Pair Driver

Typical Applications Circuits — Contd.

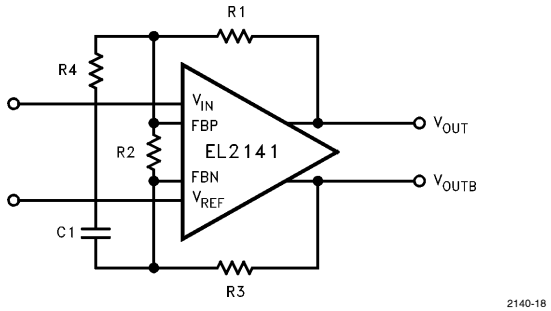


Figure 4. Differential Line Driver with Equalization

$$\text{DC Gain} = \frac{R1 + R2 + R3}{R2} \text{ (See Figure 5)}$$

$$\text{HF Gain} = \frac{R1 + (R2//R4) + R3}{(R2//R4)} \text{ (See Figure 5)}$$

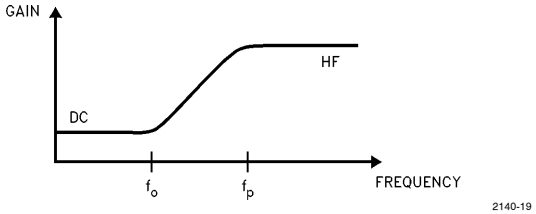


Figure 5

$$\text{where } f_o = \frac{1}{2\,\pi\,C_1\,R_2}$$

$$\text{and } f_p = \frac{1}{2\,\pi\,C_1\,R_4}$$

Typical Applications Circuits — Contd.

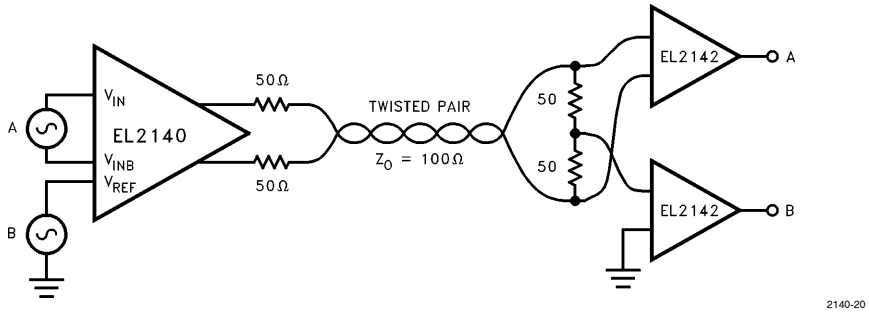


Figure 6. Dual Signal Transmission Circuit

BLANK

EL2140C/2141C

150 MHz Differential Twisted Pair Driver

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