Elan Microelectronics Crop.

CONFIDENTIAL

EM65566

82COM/ 128SEG 4096 Color STN LCD Driver

February 21, 2003

Version 0.1 (Preliminary)

EM65566 Specification Revision History		
Version	**Content**	**Date**
0.1	Initial version	February 21, 2003

Caution: The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.

Contents

1. General description

EM65566 is one of the industry's most advanced wide-screen STN-LCD drivers for 4096-color display. The industry's first sub-screen display function makes it possible to display different images and data in a sub-screen inside the main LCD screen. It also has a built-in display RAM, a power supply circuit for LCD drive, and an LCD controller circuit, therefore contributing to compact system design. Its partial display function realizes low power consumption.

*Partial display function: A function that utilizes only part of the screen, thus reducing power consumption.

2. Feature

- 4096-color display
- Outputs Segment: 384 outputs, Common: 82 outputs
- Display RAM capacity: 125952 bits
- Built-in display RAM and power supply circuit
- Partial display functions
- Switchable display in black and white mode
- Bus connection with 80-family/68-family MPU
- Logic power supply voltage: 1.7 to 3.3 V
- LCD driving voltage: 5.0 to 15.0 V
- Booster: 2 to 5 times
- Write system cycle: 200 ns
- Package(Ordering information):

Part Number	Package	Description	Package information
EM65566AGH	Gold bumped chip	NA	Page 5
EM65566AF	COF	80x104RGB (Version A)	Page126

Note: The EM65566 series has the following sub-codes depending on their shapes.

H: Bare chip (Aluminum pad without bumped); **GH**: Gold bumped chip;

F: COF package; **T**: TAB (TCP) package

Example EM65566AF → EM65566: Elan number ; A: Package Version ; F: COF package

3. Applications

- Mobile phone
- Small PDA

4. Pin configurations (package)

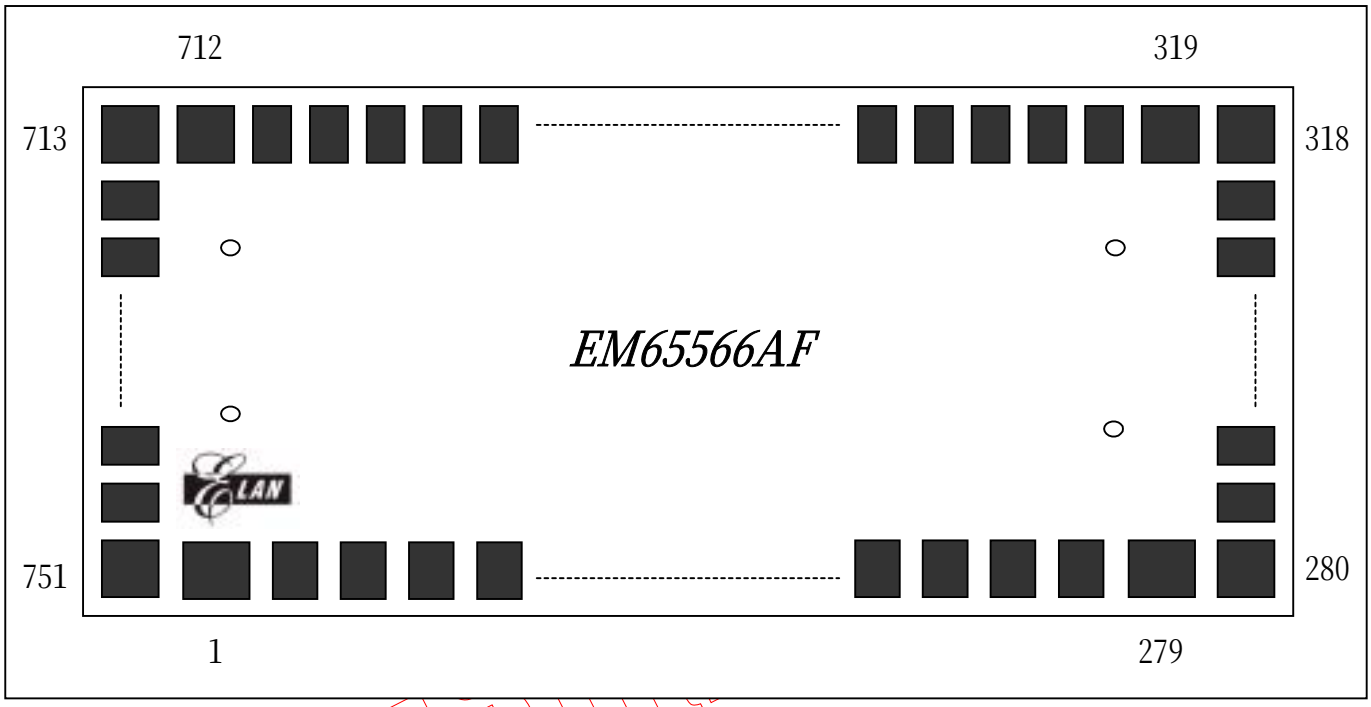


Figure 1. Pin configuration

Note: With the Elan logo in down left the pin 1 is in the down left corner

Mark	Coordinate (X,Y)	Mark	Coordinate (X,Y)
U-Left	536.3,1512.25	U-Right	20113.7,1512.25
D-Left	536.3,747.2	D-Right	20113.7,747.2

Pad configuration

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	20760	2290	μm
Bump Size	320~711	36	63	
	281~317,714~750	63	36	
	2~278,712	46	63	
	319	48	63	
	280,318,712,751	63	48	
	1,279	70	63	
Pad Pitch	50 (min.)			
Die thickness (excluding bumps)	525 +/- 29			
Bump Height	All Pad 17 +/- 3 (within die)			
Minimum Bump Gap	14			
Coordinate Origin	Chip center			

Recommended COG ITO Traces Resistor

Interface	ITO Traces resistances
V0~V4	Max=300Ω
CAP1+,CAP1-,CAP2+,CAP2-,CAP3+,CAP3- CAP4+,CAP4-,Vout	Max=100Ω
VDD,VEE	Max=100Ω
VSSL,VSSH	Max=50Ω
WRB,RDB,CSB,…,D0~D7	Max=3KΩ

PAD Coordinates Table

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
1	DUMMY	-9880.0 ,-1016.8	51	VSSL	-6479.5 ,-1016.8
2	DUMMY	-9805.0 ,-1016.8	52	VSSL	-6416.5 ,-1016.8
3	DUMMY	-9742.1 ,-1016.8	53	VSSL	-6353.5 ,-1016.8
4	DUMMY	-9679.0 ,-1016.8	54	VSSL	-6290.5 ,-1016.8
5	DUMMY	-9616.1 ,-1016.8	55	TEST	-6227.5 ,-1016.8
6	DUMMY	-9553.0 ,-1016.8	56	TEST	-6164.5 ,-1016.8
7	V0	-9490.1 ,-1016.8	57	TEST	-6101.5 ,-1016.8
8	V0	-9427.1 ,-1016.8	58	RESB	-6038.5 ,-1016.8
9	V0	-9364.1 ,-1016.8	59	RESB	-5975.5 ,-1016.8
10	V0	-9301.0 ,-1016.8	60	RESB	-5912.5 ,-1016.8
11	V0	-9238.0 ,-1016.8	61	CSB	-5849.5 ,-1016.8
12	V0	-9175.0 ,-1016.8	62	CSB	-5786.5 ,-1016.8
13	V1	-9112.0 ,-1016.8	63	CSB	-5723.5 ,-1016.8
14	V1	-9049.0 ,-1016.8	64	RS	-5660.5 ,-1016.8
15	V1	-8986.1 ,-1016.8	65	RS	-5597.5 ,-1016.8
16	V1	-8923.1 ,-1016.8	66	RS	-5534.5 ,-1016.8
17	V1	-8860.1 ,-1016.8	67	VSSA	-5471.5 ,-1016.8
18	V1	-8797.0 ,-1016.8	68	VSSA	-5408.5 ,-1016.8
19	V2	-8734.0 ,-1016.8	69	VSSA	-5345.5 ,-1016.8
20	V2	-8671.1 ,-1016.8	70	VSSA	-5282.5 ,-1016.8
21	V2	-8608.0 ,-1016.8	71	VSSA	-5219.5 ,-1016.8
22	V2	-8545.1 ,-1016.8	72	VSSA	-5156.5 ,-1016.8
23	V2	-8482.0 ,-1016.8	73	MS	-4860.2 ,-1016.8
24	V2	-8419.1 ,-1016.8	74	MS	-4797.3 ,-1016.8
25	V3	-8356.0 ,-1016.8	75	MS	-4734.3 ,-1016.8
26	V3	-8293.1 ,-1016.8	76	VDDA	-4671.2 ,-1016.8
27	V3	-8230.1 ,-1016.8	77	VDDA	-4608.2 ,-1016.8
28	V3	-8167.0 ,-1016.8	78	VDDA	-4545.3 ,-1016.8
29	V3	-8104.1 ,-1016.8	79	VDDA	-4482.3 ,-1016.8
30	V3	-8041.0 ,-1016.8	80	VDDA	-4419.2 ,-1016.8
31	V4	-7978.1 ,-1016.8	81	VDDA	-4356.3 ,-1016.8
32	V4	-7915.0 ,-1016.8	82	PS	-4293.3 ,-1016.8
33	V4	-7852.1 ,-1016.8	83	PS	-4230.2 ,-1016.8
34	V4	-7789.1 ,-1016.8	84	PS	-4167.2 ,-1016.8
35	V4	-6937.4 ,-1016.8	85	M86	-4104.3 ,-1016.8
36	V4	-6874.4 ,-1016.8	86	M86	-4041.3 ,-1016.8
37	VSSH	-6811.4 ,-1016.8	87	M86	-3978.2 ,-1016.8
38	VSSH	-6748.4 ,-1016.8	88	VSSA	-3915.2 ,-1016.8
39	VSSH	-6685.4 ,-1016.8	89	VSSA	-3852.2 ,-1016.8
40	VSSH	-6605.5 ,-1016.8	90	VSSA	-3789.3 ,-1016.8
41	VSSH	-6542.5 ,-1016.8	91	VSSA	-3726.3 ,-1016.8
42	VSSH	-6937.4 ,-1016.8	92	VSSA	-3663.2 ,-1016.8
43	DUMMY	-6874.4 ,-1016.8	93	VSSA	-3600.2 ,-1016.8
44	DUMMY	-6811.4 ,-1016.8	94	WRB	-3537.3 ,-1016.8
45	DUMMY	-6748.4 ,-1016.8	95	WRB	-3474.3 ,-1016.8
46	DUMMY	-6685.4 ,-1016.8	96	WRB	-3411.2 ,-1016.8
47	DUMMY	-6605.5 ,-1016.8	97	RDB	-3348.2 ,-1016.8
48	DUMMY	-6542.5 ,-1016.8	98	RDB	-3285.3 ,-1016.8
49	VSSL	-6937.4 ,-1016.8	99	RDB	-3222.2 ,-1016.8
50	VSSL	-6874.4 ,-1016.8	100	VDDA	-3159.2 ,-1016.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
101	VDDA	-3096.3 ,-1016.8	151	D15	804.2 ,-1016.8
102	VDDA	-3033.3 ,-1016.8	152	D15	867.2 ,-1016.8
103	VDDA	-2970.2 ,-1016.8	153	D15	930.2 ,-1016.8
104	VDDA	-2907.2 ,-1016.8	154	LP	993.2 ,-1016.8
105	VDDA	-2844.3 ,-1016.8	155	LP	1056.2 ,-1016.8
106	D0	-2498.3 ,-1016.8	156	LP	1119.2 ,-1016.8
107	D0	-2435.3 ,-1016.8	157	FLM	1182.2 ,-1016.8
108	D0	-2372.3 ,-1016.8	158	FLM	1245.2 ,-1016.8
109	D1	-2075.6 ,-1016.8	159	FLM	1308.2 ,-1016.8
110	D1	-2012.5 ,-1016.8	160	M	1371.2 ,-1016.8
111	D1	-1949.5 ,-1016.8	161	M	1434.2 ,-1016.8
112	D2	-1886.6 ,-1016.8	162	M	1497.2 ,-1016.8
113	D2	-1823.6 ,-1016.8	163	CLK	1560.2 ,-1016.8
114	D2	-1760.5 ,-1016.8	164	CLK	1623.2 ,-1016.8
115	D3	-1697.5 ,-1016.8	165	CLK	1686.2 ,-1016.8
116	D3	-1634.6 ,-1016.8	166	VSSA	1749.2 ,-1016.8
117	D3	-1571.5 ,-1016.8	167	VSSA	1812.2 ,-1016.8
118	D4	-1508.5 ,-1016.8	168	VSSA	1875.2 ,-1016.8
119	D4	-1445.6 ,-1016.8	169	VSSA	1938.2 ,-1016.8
120	D4	-1382.6 ,-1016.8	170	VSSA	2001.2 ,-1016.8
121	D5	-1319.5 ,-1016.8	171	VSSA	2064.2 ,-1016.8
122	D5	-1256.5 ,-1016.8	172	CK	2127.2 ,-1016.8
123	D5	-1193.6 ,-1016.8	173	CK	2190.2 ,-1016.8
124	D6	-1130.6 ,-1016.8	174	CK	2253.2 ,-1016.8
125	D6	-1067.5 ,-1016.8	175	CKS	2316.2 ,-1016.8
126	D6	-1004.6 ,-1016.8	176	CKS	2379.2 ,-1016.8
127	D7	-941.6 ,-1016.8	177	CKS	2442.2 ,-1016.8
128	D7	-878.5 ,-1016.8	178	VDD	2788.1 ,-1016.8
129	D7	-815.5 ,-1016.8	179	VDD	2851.1 ,-1016.8
130	D8	-752.6 ,-1016.8	180	VDD	2914.1 ,-1016.8
131	D8	-689.6 ,-1016.8	181	VDD	2977.1 ,-1016.8
132	D8	-626.5 ,-1016.8	182	VDD	3040.1 ,-1016.8
133	D9	-563.5 ,-1016.8	183	VDD	3103.1 ,-1016.8
134	D9	-500.6 ,-1016.8	184	DUMMY	3398.7 ,-1016.8
135	D9	-437.5 ,-1016.8	185	DUMMY	3461.7 ,-1016.8
136	D10	-374.5 ,-1016.8	186	DUMMY	3524.7 ,-1016.8
137	D10	-311.6 ,-1016.8	187	DUMMY	3587.7 ,-1016.8
138	D10	-248.6 ,-1016.8	188	DUMMY	3650.7 ,-1016.8
139	D11	-185.5 ,-1016.8	189	DUMMY	3713.7 ,-1016.8
140	D11	-122.5 ,-1016.8	190	VBA	3776.7 ,-1016.8
141	D11	-59.6 ,-1016.8	191	VBA	3839.7 ,-1016.8
142	D12	3.5 ,-1016.8	192	VBA	3902.7 ,-1016.8
143	D12	66.5 ,-1016.8	193	VBA	3965.7 ,-1016.8
144	D12	129.4 ,-1016.8	194	VBA	4028.7 ,-1016.8
145	D13	426.2 ,-1016.8	195	VBA	4091.7 ,-1016.8
146	D13	489.2 ,-1016.8	196	VREF	4154.7 ,-1016.8
147	D13	552.2 ,-1016.8	197	VREF	4217.7 ,-1016.8
148	D14	615.2 ,-1016.8	198	VREF	4280.7 ,-1016.8
149	D14	678.2 ,-1016.8	199	VREF	4343.7 ,-1016.8
150	D14	741.2 ,-1016.8	200	VREF	4406.7 ,-1016.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
201	VREF	4469.7 ,-1016.8	251	CAP3-	8084.9 ,-1016.8
202	VEE	4532.7 ,-1016.8	252	CAP3-	8147.9 ,-1016.8
203	VEE	4595.7 ,-1016.8	253	CAP3-	8210.9 ,-1016.8
204	VEE	4658.7 ,-1016.8	254	CAP3-	8273.9 ,-1016.8
205	VEE	4721.7 ,-1016.8	255	CAP3-	8336.9 ,-1016.8
206	VEE	4784.7 ,-1016.8	256	CAP3+	8399.9 ,-1016.8
207	VEE	4847.7 ,-1016.8	257	CAP3+	8462.9 ,-1016.8
208	VREG	4910.7 ,-1016.8	258	CAP3+	8525.9 ,-1016.8
209	VREG	4973.7 ,-1016.8	259	CAP3+	8588.9 ,-1016.8
210	VREG	5036.7 ,-1016.8	260	CAP3+	8651.9 ,-1016.8
211	VREG	5099.7 ,-1016.8	261	CAP3+	8714.9 ,-1016.8
212	VREG	5162.7 ,-1016.8	262	CAP4-	8777.9 ,-1016.8
213	VREG	5225.7 ,-1016.8	263	CAP4-	8840.9 ,-1016.8
214	VSSH	5521.3 ,-1016.8	264	CAP4-	8903.9 ,-1016.8
215	VSSH	5584.3 ,-1016.8	265	CAP4-	8966.9 ,-1016.8
216	VSSH	5647.3 ,-1016.8	266	CAP4-	9029.9 ,-1016.8
217	VSSH	5710.3 ,-1016.8	267	CAP4-	9092.9 ,-1016.8
218	VSSH	5773.3 ,-1016.8	268	CAP4+	9155.9 ,-1016.8
219	VSSH	5836.3 ,-1016.8	269	CAP4+	9218.9 ,-1016.8
220	VOUT	5899.3 ,-1016.8	270	CAP4+	9281.9 ,-1016.8
221	VOUT	5962.3 ,-1016.8	271	CAP4+	9344.9 ,-1016.8
222	VOUT	6025.3 ,-1016.8	272	CAP4+	9407.9 ,-1016.8
223	VOUT	6088.3 ,-1016.8	273	CAP4+	9470.9 ,-1016.8
224	VOUT	6151.3 ,-1016.8	274	DUMMY	9552.3 ,-1016.8
225	VOUT	6214.3 ,-1016.8	275	DUMMY	9615.3 ,-1016.8
226	CAP1-	6277.3 ,-1016.8	276	DUMMY	9678.3 ,-1016.8
227	CAP1-	6340.3 ,-1016.8	277	DUMMY	9741.3 ,-1016.8
228	CAP1-	6403.3 ,-1016.8	278	DUMMY	9804.3 ,-1016.8
229	CAP1-	6466.3 ,-1016.8	279	DUMMY	9879.3 ,-1016.8
230	CAP1-	6529.3 ,-1016.8	280	COM39	10251.9 ,-946.0
231	CAP1-	6592.3 ,-1016.8	281	COM38	10251.9 ,-890.0
232	CAP1+	6655.3 ,-1016.8	282	COM37	10251.9 ,-840.0
233	CAP1+	6718.3 ,-1016.8	283	COM36	10251.9 ,-790.0
234	CAP1+	6781.3 ,-1016.8	284	COM35	10251.9 ,-740.0
235	CAP1+	6844.3 ,-1016.8	285	COM34	10251.9 ,-690.0
236	CAP1+	6907.3 ,-1016.8	286	COM33	10251.9 ,-640.0
237	CAP1+	6970.3 ,-1016.8	287	COM32	10251.9 ,-590.0
238	CAP2-	7033.3 ,-1016.8	288	COM31	10251.9 ,-540.0
239	CAP2-	7096.3 ,-1016.8	289	COM30	10251.9 ,-490.0
240	CAP2-	7159.3 ,-1016.8	290	COM29	10251.9 ,-440.0
241	CAP2-	7222.3 ,-1016.8	291	COM28	10251.9 ,-390.0
242	CAP2-	7285.3 ,-1016.8	292	COM27	10251.9 ,-340.0
243	CAP2-	7348.3 ,-1016.8	293	COM26	10251.9 ,-290.0
244	CAP2+	7411.3 ,-1016.8	294	COM25	10251.9 ,-240.0
245	CAP2+	7474.3 ,-1016.8	295	COM24	10251.9 ,-190.0
246	CAP2+	7537.3 ,-1016.8	296	COM23	10251.9 ,-140.0
247	CAP2+	7600.3 ,-1016.8	297	COM22	10251.9 ,-90.0
248	CAP2+	7663.3 ,-1016.8	298	COM21	10251.9 ,-40.0
249	CAP2+	7726.3 ,-1016.8	299	COM20	10251.9 ,10.0
250	CAP3-	8021.9 ,-1016.8	300	COM19	10251.9 ,60.0

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
301	COM18	10251.9 ,110.0	351	SEGA9	8334.6 ,1016.8
302	COM17	10251.9 ,160.0	352	SEGB9	8284.6 ,1016.8
303	COM16	10251.9 ,210.0	353	SEGC9	8234.6 ,1016.8
304	COM15	10251.9 ,260.0	354	SEGA10	8184.6 ,1016.8
305	COM14	10251.9 ,310.0	355	SEGB10	8134.6 ,1016.8
306	COM13	10251.9 ,360.0	356	SEGC10	8084.6 ,1016.8
307	COM12	10251.9 ,410.0	357	SEGA11	8034.6 ,1016.8
308	COM11	10251.9 ,460.0	358	SEGB11	7984.6 ,1016.8
309	COM10	10251.9 ,510.0	359	SEGC11	7934.6 ,1016.8
310	COM9	10251.9 ,560.0	360	SEGA12	7884.6 ,1016.8
311	COM8	10251.9 ,610.0	361	SEGB12	7834.6 ,1016.8
312	COM7	10251.9 ,660.0	362	SEGC12	7784.6 ,1016.8
313	COM6	10251.9 ,710.0	363	SEGA13	7734.6 ,1016.8
314	COM5	10251.9 ,760.0	364	SEGB13	7684.6 ,1016.8
315	COM4	10251.9 ,810.0	365	SEGC13	7634.6 ,1016.8
316	COM3	10251.9 ,860.0	366	SEGA14	7584.6 ,1016.8
317	COM2	10251.9 ,910.0	367	SEGB14	7534.6 ,1016.8
318	COM1	10251.9 ,966.0	368	SEGC14	7484.6 ,1016.8
319	COM0	9940.6 ,1016.8	369	SEGA15	7434.6 ,1016.8
320	COMA	9884.6 ,1016.8	370	SEGB15	7384.6 ,1016.8
321	DSEGA0	9834.6 ,1016.8	371	SEGC15	7334.6 ,1016.8
322	DSEGB0	9784.6 ,1016.8	372	SEGA16	7284.6 ,1016.8
323	DSEGC0	9734.6 ,1016.8	373	SEGB16	7234.6 ,1016.8
324	SEGA0	9684.6 ,1016.8	374	SEGC16	7184.6 ,1016.8
325	SEGB0	9634.6 ,1016.8	375	SEGA17	7134.6 ,1016.8
326	SEGC0	9584.6 ,1016.8	376	SEGB17	7084.6 ,1016.8
327	SEGA1	9534.6 ,1016.8	377	SEGC17	7034.6 ,1016.8
328	SEGB1	9484.6 ,1016.8	378	SEGA18	6984.6 ,1016.8
329	SEGC1	9434.6 ,1016.8	379	SEGB18	6934.6 ,1016.8
330	SEGA2	9384.6 ,1016.8	380	SEGC18	6884.6 ,1016.8
331	SEGB2	9334.6 ,1016.8	381	SEGA19	6834.6 ,1016.8
332	SEGC2	9284.6 ,1016.8	382	SEGB19	6784.6 ,1016.8
333	SEGA3	9234.6 ,1016.8	383	SEGC19	6734.6 ,1016.8
334	SEGB3	9184.6 ,1016.8	384	SEGA20	6684.6 ,1016.8
335	SEGC3	9134.6 ,1016.8	385	SEGB20	6634.6 ,1016.8
336	SEGA4	9084.6 ,1016.8	386	SEGC20	6584.6 ,1016.8
337	SEGB4	9034.6 ,1016.8	387	SEGA21	6534.6 ,1016.8
338	SEGC4	8984.6 ,1016.8	388	SEGB21	6484.6 ,1016.8
339	SEGA5	8934.6 ,1016.8	389	SEGC21	6434.6 ,1016.8
340	SEGB5	8884.6 ,1016.8	390	SEGA22	6384.6 ,1016.8
341	SEGC5	8834.6 ,1016.8	391	SEGB22	6334.6 ,1016.8
342	SEGA6	8784.6 ,1016.8	392	SEGC22	6284.6 ,1016.8
343	SEGB6	8734.6 ,1016.8	393	SEGA23	6234.6 ,1016.8
344	SEGC6	8684.6 ,1016.8	394	SEGB23	6184.6 ,1016.8
345	SEGA7	8634.6 ,1016.8	395	SEGC23	6134.6 ,1016.8
346	SEGB7	8584.6 ,1016.8	396	SEGA24	6084.6 ,1016.8
347	SEGC7	8534.6 ,1016.8	397	SEGB24	6034.6 ,1016.8
348	SEGA8	8484.6 ,1016.8	398	SEGC24	5984.6 ,1016.8
349	SEGB8	8434.6 ,1016.8	399	SEGA25	5934.6 ,1016.8
350	SEGC8	8384.6 ,1016.8	400	SEGB25	5884.6 ,1016.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
401	SEGC25	5834.6 ,1016.8	451	SEGB42	3334.6 ,1016.8
402	SEGA26	5784.6 ,1016.8	452	SEGC42	3284.6 ,1016.8
403	SEGB26	5734.6 ,1016.8	453	SEGA43	3234.6 ,1016.8
404	SEGC26	5684.6 ,1016.8	454	SEGB43	3184.6 ,1016.8
405	SEGA27	5634.6 ,1016.8	455	SEGC43	3134.6 ,1016.8
406	SEGB27	5584.6 ,1016.8	456	SEGA44	3084.6 ,1016.8
407	SEGC27	5534.6 ,1016.8	457	SEGB44	3034.6 ,1016.8
408	SEGA28	5484.6 ,1016.8	458	SEGC44	2984.6 ,1016.8
409	SEGB28	5434.6 ,1016.8	459	SEGA45	2934.6 ,1016.8
410	SEGC28	5384.6 ,1016.8	460	SEGB45	2884.6 ,1016.8
411	SEGA29	5334.6 ,1016.8	461	SEGC45	2834.6 ,1016.8
412	SEGB29	5284.6 ,1016.8	462	SEGA46	2784.6 ,1016.8
413	SEGC29	5234.6 ,1016.8	463	SEGB46	2734.6 ,1016.8
414	SEGA30	5184.6 ,1016.8	464	SEGC46	2684.6 ,1016.8
415	SEGB30	5134.6 ,1016.8	465	SEGA47	2634.6 ,1016.8
416	SEGC30	5084.6 ,1016.8	466	SEGB47	2584.6 ,1016.8
417	SEGA31	5034.6 ,1016.8	467	SEGC47	2534.6 ,1016.8
418	SEGB31	4984.6 ,1016.8	468	SEGA48	2484.6 ,1016.8
419	SEGC31	4934.6 ,1016.8	469	SEGB48	2434.6 ,1016.8
420	SEGA32	4884.6 ,1016.8	470	SEGC48	2384.6 ,1016.8
421	SEGB32	4834.6 ,1016.8	471	SEGA49	2334.6 ,1016.8
422	SEGC32	4784.6 ,1016.8	472	SEGB49	2284.6 ,1016.8
423	SEGA33	4734.6 ,1016.8	473	SEGC49	2234.6 ,1016.8
424	SEGB33	4684.6 ,1016.8	474	SEGA50	2184.6 ,1016.8
425	SEGC33	4634.6 ,1016.8	475	SEGB50	2134.6 ,1016.8
426	SEGA34	4584.6 ,1016.8	476	SEGC50	2084.6 ,1016.8
427	SEGB34	4534.6 ,1016.8	477	SEGA51	2034.6 ,1016.8
428	SEGC34	4484.6 ,1016.8	478	SEGB51	1984.6 ,1016.8
429	SEGA35	4434.6 ,1016.8	479	SEGC51	1934.6 ,1016.8
430	SEGB35	4384.6 ,1016.8	480	SEGA52	1884.6 ,1016.8
431	SEGC35	4334.6 ,1016.8	481	SEGB52	1834.6 ,1016.8
432	SEGA36	4284.6 ,1016.8	482	SEGC52	1784.6 ,1016.8
433	SEGB36	4234.6 ,1016.8	483	SEGA53	1734.6 ,1016.8
434	SEGC36	4184.6 ,1016.8	484	SEGB53	1684.6 ,1016.8
435	SEGA37	4134.6 ,1016.8	485	SEGC53	1634.6 ,1016.8
436	SEGB37	4084.6 ,1016.8	486	SEGA54	1584.6 ,1016.8
437	SEGC37	4034.6 ,1016.8	487	SEGB54	1534.6 ,1016.8
438	SEGA38	3984.6 ,1016.8	488	SEGC54	1484.6 ,1016.8
439	SEGB38	3934.6 ,1016.8	489	SEGA55	1434.6 ,1016.8
440	SEGC38	3884.6 ,1016.8	490	SEGB55	1384.6 ,1016.8
441	SEGA39	3834.6 ,1016.8	491	SEGC55	1334.6 ,1016.8
442	SEGB39	3784.6 ,1016.8	492	SEGA56	1284.6 ,1016.8
443	SEGC39	3734.6 ,1016.8	493	SEGB56	1234.6 ,1016.8
444	SEGA40	3684.6 ,1016.8	494	SEGC56	1184.6 ,1016.8
445	SEGB40	3634.6 ,1016.8	495	SEGA57	1134.6 ,1016.8
446	SEGC40	3584.6 ,1016.8	496	SEGB57	1084.6 ,1016.8
447	SEGA41	3534.6 ,1016.8	497	SEGC57	1034.6 ,1016.8
448	SEGB41	3484.6 ,1016.8	498	SEGA58	984.6 ,1016.8
449	SEGC41	3434.6 ,1016.8	499	SEGB58	934.6 ,1016.8
450	SEGA42	3384.6 ,1016.8	500	SEGC58	884.6 ,1016.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
501	SEGA59	834.6 ,1016.8	551	SEGC75	-1884.6 ,1016.8
502	SEGB59	784.6 ,1016.8	552	SEGA76	-1934.6 ,1016.8
503	SEGB59	734.6 ,1016.8	553	SEGB76	-1984.6 ,1016.8
504	SEGA60	684.6 ,1016.8	554	SEGC76	-2034.6 ,1016.8
505	SEGB60	634.6 ,1016.8	555	SEGA77	-2084.6 ,1016.8
506	SEGC60	584.6 ,1016.8	556	SEGB77	-2134.6 ,1016.8
507	SEGA61	534.6 ,1016.8	557	SEGC77	-2184.6 ,1016.8
508	SEGB61	484.6 ,1016.8	558	SEGA78	-2234.6 ,1016.8
509	SEGC61	434.6 ,1016.8	559	SEGB78	-2284.6 ,1016.8
510	SEGA62	384.6 ,1016.8	560	SEGC78	-2334.6 ,1016.8
511	SEGB62	334.6 ,1016.8	561	SEGA79	-2384.6 ,1016.8
512	SEGC62	284.6 ,1016.8	562	SEGB79	-2434.6 ,1016.8
513	SEGA63	234.6 ,1016.8	563	SEGC79	-2484.6 ,1016.8
514	SEGB63	184.6 ,1016.8	564	SEGA80	-2534.6 ,1016.8
515	SEGC63	134.6 ,1016.8	565	SEGB80	-2584.6 ,1016.8
516	SEGA64	-134.6 ,1016.8	566	SEGC80	-2634.6 ,1016.8
517	SEGB64	-184.6 ,1016.8	567	SEGA81	-2684.6 ,1016.8
518	SEGC64	-234.6 ,1016.8	568	SEGB81	-2734.6 ,1016.8
519	SEGA65	-284.6 ,1016.8	569	SEGC81	-2784.6 ,1016.8
520	SEGB65	-334.6 ,1016.8	570	SEGA82	-2834.6 ,1016.8
521	SEGC65	-384.6 ,1016.8	571	SEGB82	-2884.6 ,1016.8
522	SEGA66	-434.6 ,1016.8	572	SEGC82	-2934.6 ,1016.8
523	SEGB66	-484.6 ,1016.8	573	SEGA83	-2984.6 ,1016.8
524	SEGC66	-534.6 ,1016.8	574	SEGB83	-3034.6 ,1016.8
525	SEGA67	-584.6 ,1016.8	575	SEGC83	-3084.6 ,1016.8
526	SEGB67	-634.6 ,1016.8	576	SEGA84	-3134.6 ,1016.8
527	SEGC67	-684.6 ,1016.8	577	SEGB84	-3184.6 ,1016.8
528	SEGA68	-734.6 ,1016.8	578	SEGC84	-3234.6 ,1016.8
529	SEGB68	-784.6 ,1016.8	579	SEGA85	-3284.6 ,1016.8
530	SEGC68	-834.6 ,1016.8	580	SEGB85	-3334.6 ,1016.8
531	SEGA69	-884.6 ,1016.8	581	SEGC85	-3384.6 ,1016.8
532	SEGB69	-934.6 ,1016.8	582	SEGA86	-3434.6 ,1016.8
533	SEGC69	-984.6 ,1016.8	583	SEGB86	-3484.6 ,1016.8
534	SEGA70	-1034.6 ,1016.8	584	SEGC86	-3534.6 ,1016.8
535	SEGB70	-1084.6 ,1016.8	585	SEGA87	-3584.6 ,1016.8
536	SEGC70	-1134.6 ,1016.8	586	SEGB87	-3634.6 ,1016.8
537	SEGA71	-1184.6 ,1016.8	587	SEGC87	-3684.6 ,1016.8
538	SEGB71	-1234.6 ,1016.8	588	SEGA88	-3734.6 ,1016.8
539	SEGC71	-1284.6 ,1016.8	589	SEGB88	-3784.6 ,1016.8
540	SEGA72	-1334.6 ,1016.8	590	SEGC88	-3834.6 ,1016.8
541	SEGB72	-1384.6 ,1016.8	591	SEGA89	-3884.6 ,1016.8
542	SEGC72	-1434.6 ,1016.8	592	SEGB89	-3934.6 ,1016.8
543	SEGA73	-1484.6 ,1016.8	593	SEGC89	-3984.6 ,1016.8
544	SEGB73	-1534.6 ,1016.8	594	SEGA90	-4034.6 ,1016.8
545	SEGC73	-1584.6 ,1016.8	595	SEGB90	-4084.6 ,1016.8
546	SEGA74	-1634.6 ,1016.8	596	SEGC90	-4134.6 ,1016.8
547	SEGB74	-1684.6 ,1016.8	597	SEGA91	-4184.6 ,1016.8
548	SEGC74	-1734.6 ,1016.8	598	SEGB91	-4234.6 ,1016.8
549	SEGA75	-1784.6 ,1016.8	599	SEGC91	-4284.6 ,1016.8
550	SEGB75	-1834.6 ,1016.8	600	SEGA92	-4334.6 ,1016.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
601	SEGB92	-4384.6 ,1016.8	651	SEGA109	-6884.6 ,1016.8
602	SEGC92	-4434.6 ,1016.8	652	SEGB109	-6934.6 ,1016.8
603	SEGA93	-4484.6 ,1016.8	653	SEGC109	-6984.6 ,1016.8
604	SEGB93	-4534.6 ,1016.8	654	SEGA110	-7034.6 ,1016.8
605	SEGC93	-4584.6 ,1016.8	655	SEGB110	-7084.6 ,1016.8
606	SEGA94	-4634.6 ,1016.8	656	SEGB110	-7134.6 ,1016.8
607	SEGB94	-4684.6 ,1016.8	657	SEGA111	-7184.6 ,1016.8
608	SEGC94	-4734.6 ,1016.8	658	SEGB111	-7234.6 ,1016.8
609	SEGA95	-4784.6 ,1016.8	659	SEGC111	-7284.6 ,1016.8
610	SEGB95	-4834.6 ,1016.8	660	SEGA112	-7334.6 ,1016.8
611	SEGC95	-4884.6 ,1016.8	661	SEGB112	-7384.6 ,1016.8
612	SEGA96	-4934.6 ,1016.8	662	SEGC112	-7434.6 ,1016.8
613	SEGB96	-4984.6 ,1016.8	663	SEGA113	-7484.6 ,1016.8
614	SEGC96	-5034.6 ,1016.8	664	SEGB113	-7534.6 ,1016.8
615	SEGA97	-5084.6 ,1016.8	665	SEGC113	-7584.6 ,1016.8
616	SEGB97	-5134.6 ,1016.8	666	SEGA114	-7634.6 ,1016.8
617	SEGC97	-5184.6 ,1016.8	667	SEGB114	-7684.6 ,1016.8
618	SEGA98	-5234.6 ,1016.8	668	SEGC114	-7734.6 ,1016.8
619	SEGB98	-5284.6 ,1016.8	669	SEGA115	-7784.6 ,1016.8
620	SEGC98	-5334.6 ,1016.8	670	SEGB115	-7834.6 ,1016.8
621	SEGA99	-5384.6 ,1016.8	671	SEGB115	-7884.6 ,1016.8
622	SEGB99	-5434.6 ,1016.8	672	SEGA116	-7934.6 ,1016.8
623	SEGC99	-5484.6 ,1016.8	673	SEGB116	-7984.6 ,1016.8
624	SEGA100	-5534.6 ,1016.8	674	SEGC116	-8034.6 ,1016.8
625	SEGB100	-5584.6 ,1016.8	675	SEGA117	-8084.6 ,1016.8
626	SEGC100	-5634.6 ,1016.8	676	SEGB117	-8134.6 ,1016.8
627	SEGA101	-5684.6 ,1016.8	677	SEGC117	-8184.6 ,1016.8
628	SEGB101	-5734.6 ,1016.8	678	SEGA118	-8234.6 ,1016.8
629	SEGC101	-5784.6 ,1016.8	679	SEGB118	-8284.6 ,1016.8
630	SEGA102	-5834.6 ,1016.8	680	SEGC118	-8334.6 ,1016.8
631	SEGB102	-5884.6 ,1016.8	681	SEGA119	-8384.6 ,1016.8
632	SEGC102	-5934.6 ,1016.8	682	SEGB119	-8434.6 ,1016.8
633	SEGA103	-5984.6 ,1016.8	683	SEGC119	-8484.6 ,1016.8
634	SEGB103	-6034.6 ,1016.8	684	SEGA120	-8534.6 ,1016.8
635	SEGC103	-6084.6 ,1016.8	685	SEGB120	-8584.6 ,1016.8
636	SEGA104	-6134.6 ,1016.8	686	SEGC120	-8634.6 ,1016.8
637	SEGB104	-6184.6 ,1016.8	687	SEGA121	-8684.6 ,1016.8
638	SEGC104	-6234.6 ,1016.8	688	SEGB121	-8734.6 ,1016.8
639	SEGA105	-6284.6 ,1016.8	689	SEGC121	-8784.6 ,1016.8
640	SEGB105	-6334.6 ,1016.8	690	SEGA122	-8834.6 ,1016.8
641	SEGC105	-6384.6 ,1016.8	691	SEGB122	-8884.6 ,1016.8
642	SEGA106	-6434.6 ,1016.8	692	SEGC122	-8934.6 ,1016.8
643	SEGB106	-6484.6 ,1016.8	693	SEGA123	-8984.6 ,1016.8
644	SEGC106	-6534.6 ,1016.8	694	SEGB123	-9034.6 ,1016.8
645	SEGA107	-6584.6 ,1016.8	695	SEGB123	-9084.6 ,1016.8
646	SEGB107	-6634.6 ,1016.8	696	SEGA124	-9134.6 ,1016.8
647	SEGC107	-6684.6 ,1016.8	697	SEGB124	-9184.6 ,1016.8
648	SEGA108	-6734.6 ,1016.8	698	SEGC124	-9234.6 ,1016.8
649	SEGB108	-6784.6 ,1016.8	699	SEGA125	-9284.6 ,1016.8
650	SEGC108	-6834.6 ,1016.8	700	SEGB125	-9334.6 ,1016.8

Pin NO	*Pad Name*	*Coordinate* (X,Y)	*Pin NO*	*Pad Name*	*Coordinate* (X,Y)
701	SEGC125	-9384.6 ,1016.8	751	COMB	-10251.8 ,-946.0
702	SEGA126	-9434.6 ,1016.8			
703	SEGB126	-9484.6 ,1016.8			
704	SEGC126	-9534.6 ,1016.8			
705	SEGA127	-9584.6 ,1016.8			
706	SEGB127	-9634.6 ,1016.8			
707	SEGC127	-9684.6 ,1016.8			
708	DSEGA1	-9734.6 ,1016.8			
709	DSEGB1	-9784.6 ,1016.8			
710	DSEGB1	-9834.6 ,1016.8			
711	COM40	-9884.6 ,1016.8			
712	COM41	-9940.6 ,1016.8			
713	COM42	-10251.8 ,966.0			
714	COM43	-10251.8 ,910.0			
715	COM44	-10251.8 ,860.0			
716	COM45	-10251.8 ,810.0			
717	COM46	-10251.8 ,760.0			
718	COM47	-10251.8 ,710.0			
719	COM48	-10251.8 ,660.0			
720	COM49	-10251.8 ,610.0			
721	COM50	-10251.8 ,560.0			
722	COM51	-10251.8 ,510.0			
723	COM52	-10251.8 ,460.0			
724	COM53	-10251.8 ,410.0			
725	COM54	-10251.8 ,360.0			
726	COM55	-10251.8 ,310.0			
727	COM56	-10251.8 ,260.0			
728	COM57	-10251.8 ,210.0			
729	COM58	-10251.8 ,160.0			
730	COM59	-10251.8 ,110.0			
731	COM60	-10251.8 ,60.0			
732	COM61	-10251.8 ,10.0			
733	COM62	-10251.8 ,-40.0			
734	COM63	-10251.8 ,-90.0			
735	COM64	-10251.8 ,-140.0			
736	COM65	-10251.8 ,-190.0			
737	COM66	-10251.8 ,-240.0			
738	COM67	-10251.8 ,-290.0			
739	COM68	-10251.8 ,-340.0			
740	COM69	-10251.8 ,-390.0			
741	COM70	-10251.8 ,-440.0			
742	COM71	-10251.8 ,-490.0			
743	COM72	-10251.8 ,-540.0			
744	COM73	-10251.8 ,-590.0			
745	COM74	-10251.8 ,-640.0			
746	COM75	-10251.8 ,-690.0			
747	COM76	-10251.8 ,-740.0			
748	COM77	-10251.8 ,-790.0			
749	COM78	-10251.8 ,-840.0			
750	COM79	-10251.8 ,-890.0			

Note : For PCB layout, IC substrate must be connected to VSS

5. *Functional block diagram*

5.1 System Block Diagram

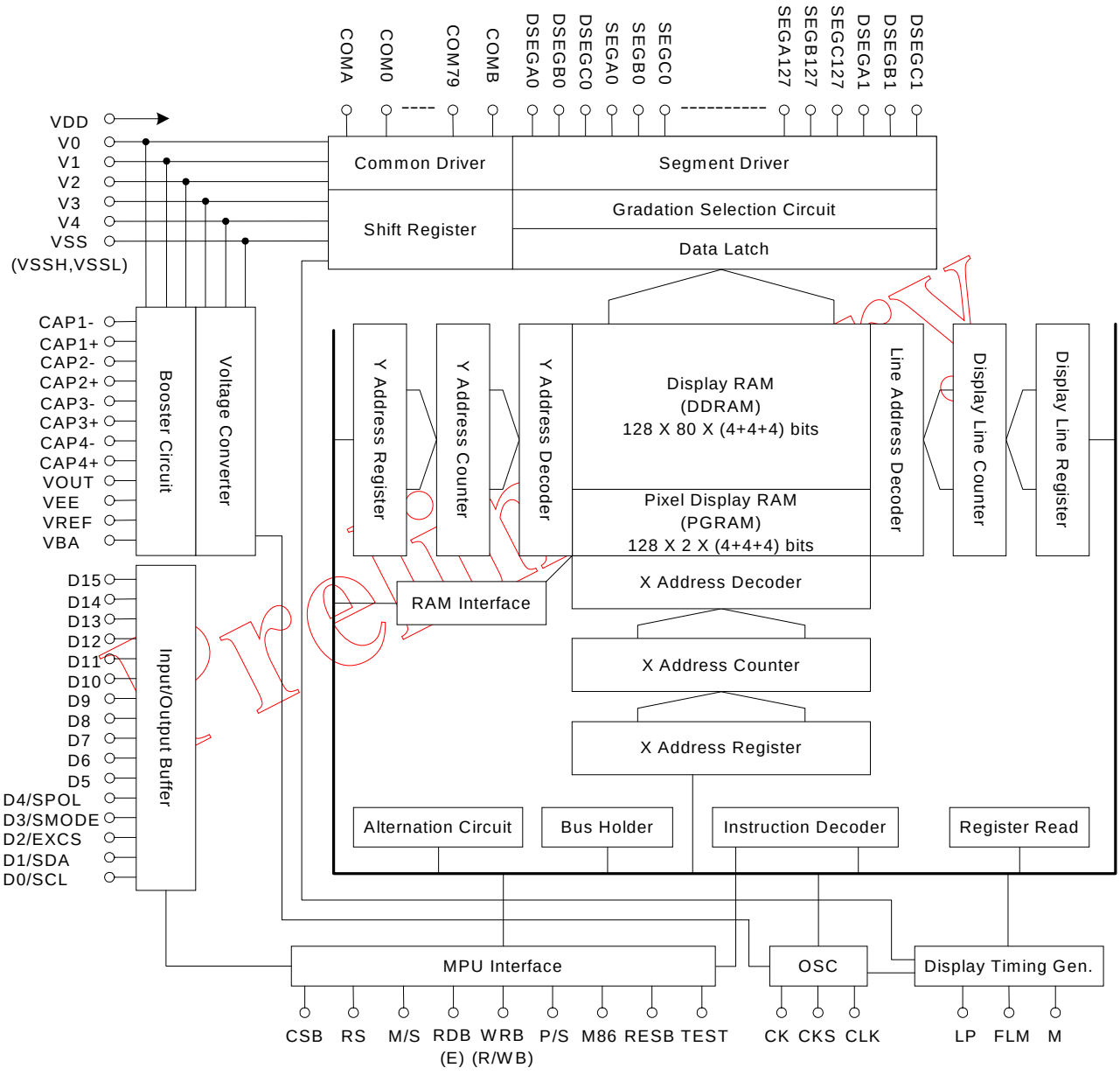


Figure 2. System Block Diagram

5.2 Power Circuit Block Diagram

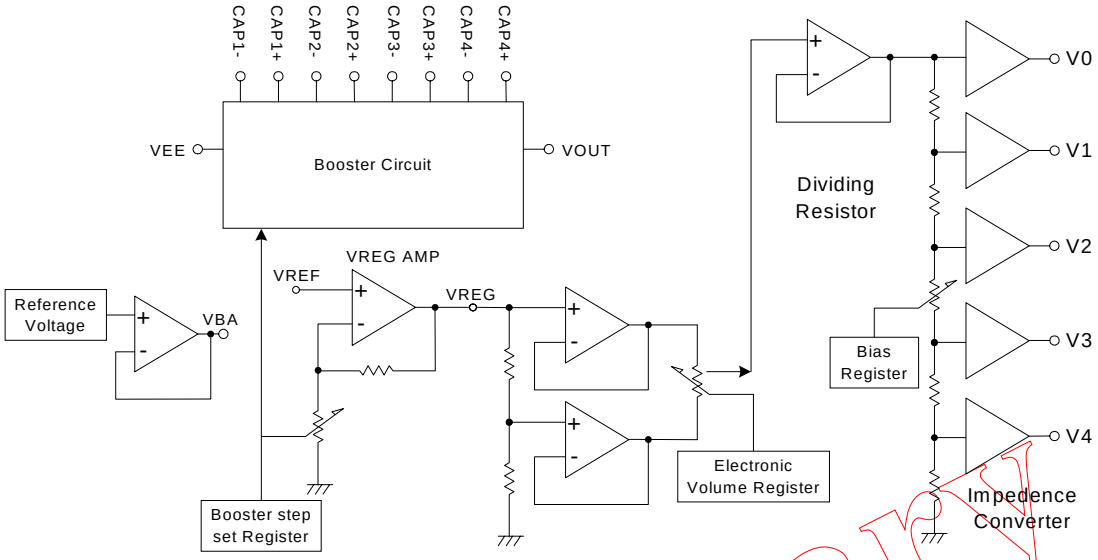


Figure 3. Power Circuit Block Diagram

6. Pin Description

6.1 Power Supply Pins

Symbol	*I/O*	*Description*
VDD	Power Supply	Power supply pin for logic circuit to +2.4 to 3.3V
VSSL	Power Supply	Ground pin for logic circuit, connect to 0V
VSSH	Power Supply	Ground pin for high voltage circuit, connected to 0V
V0 V1 V2 V3 V4	Power Supply	Bias power supply pin for LCD drive voltage When using an external power supply, convert impedance by using resistance-division of LCD drive power supply or operation amplifier before adding voltage to the pins. These voltages should have following relationship: VSS<V4<V3<V2<V1<V0 When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. Then, must connect capacitor each to VSS.

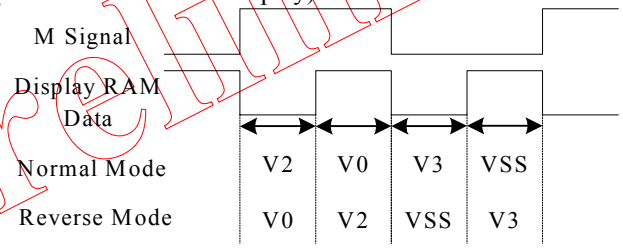
6.2 LCD Power Supply Circuit Pins

Symbol	*I/O*	*Description*
CAP1+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP1- and CAP1+.
CAP1-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP1- and CAP1+.
CAP2+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP2- and CAP2+.
CAP2	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP2- and CAP2+.
CAP3+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP3- and CAP3+.
CAP3-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP3- and CAP3+.
CAP4+	O	Connecting pin for the built in booster's capacitor + side. The capacitor is connected between CAP4- and CAP4+.
CAP4-	O	Connecting pin for the built in booster's capacitor - side. The capacitor is connected between CAP4- and CAP4+.
VBA	O	0.9 times VDD voltage output pin
VREF	I	Voltage input pin for generating reference power source
VEE	Power Supply	Voltage supply pin for booster circuit. Usually the same voltage level as VDD. In the case of TCP, draw it as a separate terminal.
VOUT	O	Output pin of boosted voltage in the built-in booster. The capacitor must be connected between this pin and VSS.
VREG	O	Output pin for regulated voltage of VREG AMP. The capacitor must be connected between this pin and VSS.

6.3 System Bus Pins

Symbol	*I/O*	*Description*
RESB	I	Reset input pin. When RESB is "L", initialization is executed.
D0/SCL D1/SDA D2/EXCS D3/SMODE D4/SPOL D5-D7	I/O	Data bus / Signal interface related pins. When parallel interface is selected (P/S = "H"), The D7-D0 are 8-bits bi-directional data bus, connect to MPU data bus. When serial interface is selected (P/S = "L"), D0 and D1 (SCL, SDA) are used as serial interface pins. SCL: Input pin for data transfer clock SDA: Serial data input pin EXCS: Extended Chip Select I/O pin SMODE: Serial transfer mode select pin SPOL: RS pole select pin when 3-wires serial interface is selected. SDA data is latched at the rising edge of SCL. Internal serial/parallel conversion into 8-bit data occurs at the rising edge of 8th clock of SCL After completing data transferring, or when making no access, be sure to set SCL to "L".
D8-D15	I/O	8-bit bi-directional bus. Connected to MPU data bus. Used as data bus for upper 8-pins in the 16-bits access mode.
CSB	I	Chip Select input pin. CSB = "L": accepts access from MPU CSB = "H": denies access from MPU
RS	I	RAM/Register select input pin. RS = "0": D7-D0 are display RAM data RS = "1": D7-D0 are control register data
RDB (E)	I	Read/Write control pin Select 80-family MPU type (M86 = "L") The RDB is a data read signal. When RDB is "L", D7-D0 are in an output status. Select 68-family MPU type (M86 = "H") R/WB = "H": When E is "H", D7-D0 are in an output status. R/WB = "L": The data on D7-D0 are latched at falling edge fo the E signal.
WRB (R/WB)	I	Read/Write control pin Select 80-family MPU type (M86 = "L") The WRB is a data write signal. The data on D7-D0 are latched at rising edge of the WRB signal. Select 68-family MPU type (M86 = "H") Read/Write control input pin. R/W = "H": Read R/W = "L": Write
M86	I	MPU interface type selecting input pin. M86 = "H": 68-family interface M86 = "L": 80-family interface Fixed at either "H" or "L"
P/S	I	Parallel/Serial interface select pin. *P/S* | *Chip select* | *Data identification* | *Data* | *Read/Write* | *Serial clock* H | CSB | RS | D0-D7 | RDB, WRB | - L | CSB | RS | SDA | Write only | SCL P/S = "H": For parallel interface. P/S = "L": For serial interface. Fix D15-D5 pins are Hi-Z, RDB and WRB pins to either "H" or "L".
TEST	I	For testing. Fix to "L".

6.4 LCD Drive Circuit Signals

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>LP</td><td>I/O</td><td>The LP is latch clock I/O pin.
At the rising edge, count the display line counter. At the falling edge output the LCD drive signal. This pin use in master/slave multi-chip system
M/S = “H”: LP is output
M/S = “L”: LP is input</td></tr>
<tr><td>FLM</td><td>I/O</td><td>I/O pin for LCD display synchronous signals (first line maker).
When FLM pin is set to “H”, the display start-line address is preset. This pin use in master/slave multi-chip system. In the display line counter
M/S = “H”: FLM is output
M/S = “L”: FLM is input</td></tr>
<tr><td>M</td><td>I/O</td><td>I/O pin for alternated signals of LCD drive output.
M/S = “H”: M is output
M/S = “L”: M is input
This pin use in master/slave multi-chip system.</td></tr>
<tr><td>M/S</td><td>I</td><td>Maser/Slave mode select input pin
<table>
<tr><th>M/S</th><th>State</th><th>OSC</th><th>Power Supply Circuit</th><th>LP</th><th>FLM</th><th>M</th><th>CLK</th></tr>
<tr><td>H</td><td>Master</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Slave</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Input</td><td>Input</td></tr>
</table>
Fix to “H” or “L” at this terminal.</td></tr>
<tr><td>SEGA0-A127
SEGB0-B127
SEGC0-C127</td><td>O</td><td>Segment output pins for LCD drives.
According to the data of the Display RAM data, non-lighted at “0”, lighted at “1” (Normal Mode). non-lighted at “1”, lighted at “0” (Reverse Mode) and, by a combination of M signal and display data, one signal level among V0,V2,V3 and VSS signal levels are selected.
(When Monochrome Display)
 
</td></tr>
<tr><td>DSEGA0, A1
DSEGB0, B1
DSEGC0, C1</td><td>O</td><td>Special segment output pins for LCD drivers.
All Common period output same data. Only for display frame.</td></tr>
<tr><td>COM0-
COM79</td><td>O</td><td>Common output pins for LCD drivers. By a combination of the scanning data and M signal, one signal level among V0, V1, V4 and VSS signal level is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
<tr><td>COMA</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
<tr><td>COMB</td><td>O</td><td>Common output pin for LCD drive exclusively for icons.</td></tr>
</table>

6.5 Oscillating Circuit Pin

Symbol	*I/O*	*Description*
CKS	I	Display timing clock source select input pin. CKS = "H": Use external clock from CK pin. CKS = "L": Use internal oscillated clock. In the slave mode, fix this pin at "L". In the case of TCP, draw it as a separate terminal.
CK	I	External clock input pin for display timing. In the slave mode, fix the CK pin at "L". In the case of TCP, draw it as a separate terminal.
CLK	I/O	I/O pin for display timing clock. To use this pin in the master/slave system. M/S = "H": Output display timing clock. M/S = "L": Input display timing clock from the master.

7. Functional Description

7.1 MPU Interface

7.1.1 Selection of Interface Type

The EM65566 transfers data through 8-bit parallel I/O (D7-D0), 16-bit parallel I/O (D15-D0) or serial data input (SDA, SCL). The parallel interface or serial interface can select by state of P/S pin. When select serial interface, data reading cannot be performed, only data writing can operate.

P/S	*I/F Type*	*CSB*	*RS*	*RDB*	*WRB*	*M86*	*SDA*	*SCL*	*Data*
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D7~D0 (D15~D0)
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

7.1.2 Parallel Input

When parallel interface is selected with the P/S pin, the EM65566 allows data to be transferred in parallel to an 8-bit/16-bit MPU through the data bus. For the 8-bit/16-bit MPU, either the 80-family MPU interface or the 68-family MPU interface can be selected with the m86 pin.

M86	*MPU Type*	*CSB*	*RS*	*RDB*	*WRB*	*Data*
H	68-family MPU	CSB	RS	E	R/WB	D7~D0 (D15~D0)
L	80-family MPU	CSB	RS	RDB	WRB	D0~D7 (D15~D0)

7.1.3 Read/Write functions of Register and display RAM

The EM65566 have four read/write functions at parallel interface mode. Each read/write function select by combinations of RS, RDB and WRB signals.

RS	*68-family R/WB*	*80-family*		*Function*
		RDB	*WRB*	
1	1	0	1	Read internal Register
1	0	1	0	Write internal Register
0	1	0	1	Read display data
0	0	1	0	Write display data

7.1.4 Serial Interface

EM65566 has two types serial interface. One is a 3-wires type serial interface; other one is a 4-wires type serial interface. The 3-wire or 4-wire is determined by SMODE pin.

SMODE = "L": 4-wires serial interface

SMODE = "H": 3-wires serial interface

7.1.5 4-Wires Serial Interface

When chip select is active (CSB = "L"), 4-wires type serial interface can work through the SDA and SCL input pins. When chip select is inactive (CSB = "H"), the internal shift register and counter are reset in the initial condition. Serial data SDA are input sequentially in order of D7 to D0 at the rising of serial clock (SCL) and are converted into 8-bit parallel data (by serial to parallel conversion) at the rising edge of the 8th serial clock, being processed in accordance with the data. The identification whether are serial data inputs (SDA) are display data or control register data is judged by input to RS pin.

RS = “L”: display RAM data

RS = “H”: control register data

After completing 8-bit data transferring, or when making no access, be sure to set serial clock input (SCL) to “L”. Cares of SDA and SCL signals against external noise should be taken in board writing. To prevent transfer error due to external noise, release chip select (CSB = “H”) every completion of 8-bit data transferring.

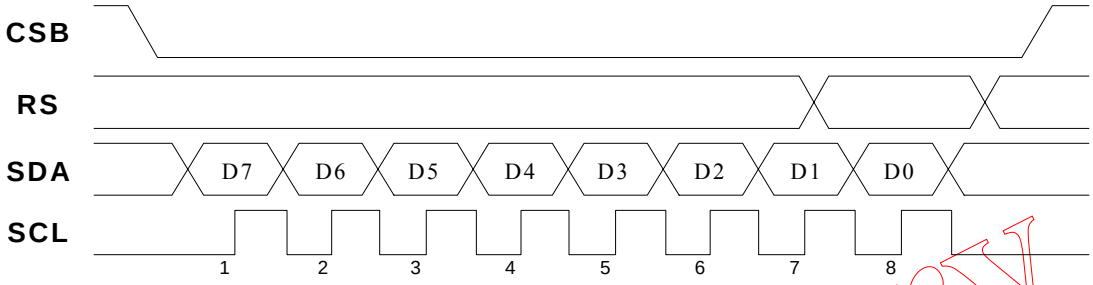


Figure 4. 4-Wires type Serial Interface

7.1.6 3-Wires Type Serial Interface

When chip select is active (CSB = “L”), 3-wires type serial interface can work through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset in the initial condition. Serial data SDA are input sequentially in order of RS, D7 to D0 at the rising edge of serial clock (SCL) and are converter into 9-bit parallel data (by serial to parallel conversion) at the rising edge of the 9th serial clock. The identification whether the serial data inputs (SDA) are display data or control register data is determined by first serial input data (RS) and SPOL pin as followed.

SPOL = “0”		*SPOL = “1”*	
RS	Display RAM/Register	RS	Display RAM/Register
0	Display RAM Data	0	Control Register Data
1	Control Register Data	1	Display RAM Data

After completing 9-bits data transferring, or when making no access, be sure to set serial clock input (SCL) to “L”. Cares of SDA and SCL signals against external noise should be taken in board wiring. To prevent transfer error due to external noise, release chip select (CSB = “H”) every completion of 9-bit data transferring.

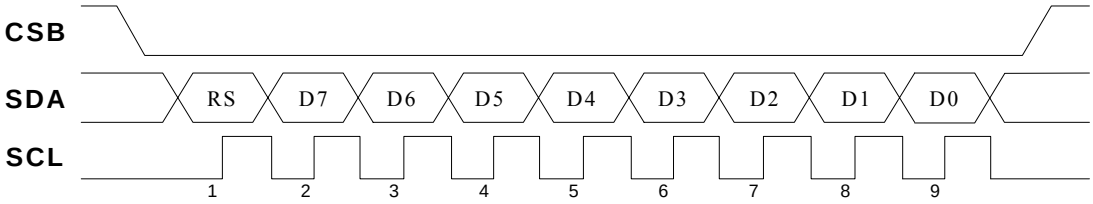
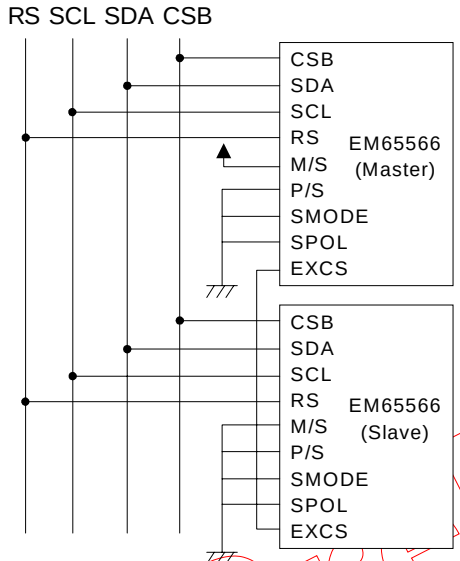


Figure 5. 3-Wires Type Serial Interface

7.1.7 Chip Select Connection in Serial Interface Mode

When serial interface use in 2 chips EM65566 system; one is a Master another is a slave, both EM65566 can control by only one chip select signal. For reduce the chip select signal, connect master chip EXCS pin and slave chip EXCS pin as following diagram. The EXCS pin output level can control by internal EXCS register in master chip. If EXCS register set to "0" in master chip, after that master chip only recognizes EXCS register access instruction and can access slave chip. The slave chip can only access at both EXCS and CSB input is "L".



EXCS: Extend Chip Select (I/O)
- Master device: Output
- Slave device: Input

P/S: Select parallel/serial interface (Input)
- P/S =0: Serial interface select.
- P/S=1: Parallel interface select

M/S: Select master/slave mode (Input)
- M/S=0: Slave mode select
- M/S=1: Master mode select

SMODE: Select 3/4-wires serial interface (Input)
- SMODE=0: 4-wires serial interface select
- SMODE=1: 3-wires serial interface select

SPOL: Select RS bit polarity (Input)
This pin can work only 3 wires serial interface mode.
- SPOL=0: If RS = "0", access to display RAM
- SPOL=1: If RS = "1", access to display RAM

7.2 Data write to Display RAM and Control Register

The data write to display RAM and Control Register use almost same procedure, only different setting of RS that select access object.

RS = "L": Display RAM data

RS = "H": Control register data

In the case of the 80-family MPU, the data is written at the rising edge of WRB. In the case of the 68-family MPU, the data is written at the falling edge of signal E.

Data write operation

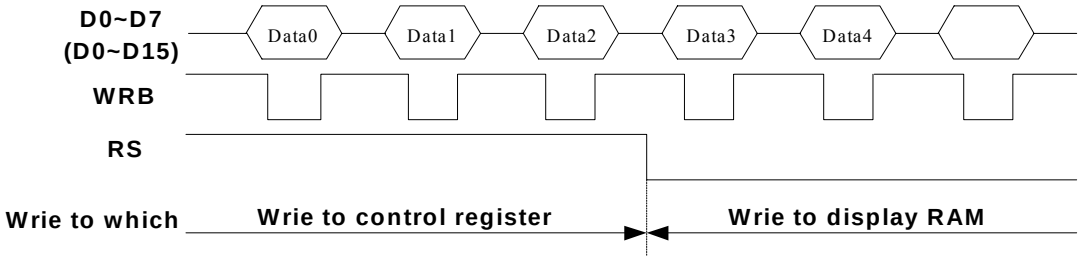


Figure 6. Data write operation

7.3 Internal Register Read

In the case of display RAM read operation, need dummy read one time. The designated address data are not output to read operation immediately after the address set to AX or AY register, but are output when the second data read. Dummy read is always required one time after address set and write cycle.

Read display RAM operation

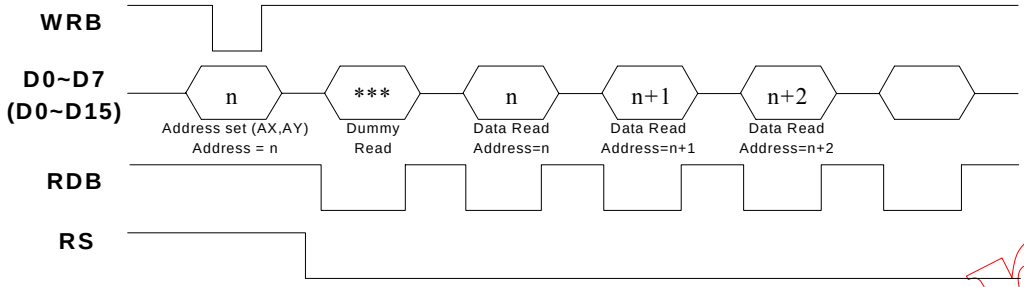


Figure 7. Read display RAM operation

The EM65566 can be read the control registers, in case of control register read operation, data bus upper nibble (D7-D4) use for register address(0 to FH). In maximum, 16 registers can access directly. But number of register is more than 16 registers. Therefore, EM65566 has register bank control. The RE register is set bank number to access. And the RE address is 0FH, in any bank can access RE register. It is need 4-steps to read the specific register in maximum case.

1.Write 04H to RE register for access to RA register.

2.Writes specific register address to RA register.

3.Write specific register bank to RE register.

4.Read specific register contents.

Register read operation

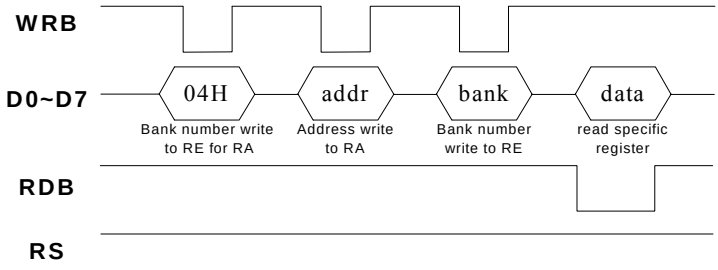


Figure 8. Register read operation

7.4 16-bit Data Access to Display RAM

The EM65566 correspond to 8-bits and 16-bits bus size access.

The data bus size can select by WLS register.

WLS = “0”: 8-bits bus size

WLS = “1”: 16-bits bus size

In the 16-bits access mode, access for control register use low-byte data bus (D7~D0). Then high byte data bus (D15~D8) are not used in internal circuit. When read control register using 16-bits bus. Register values output to D3-D0 and D15-D4 output “H”.

7.5 Display Start Address Register

This register determines the Y-address of the display RAM corresponding to the display start line. The display RAM data that addressed Display Start Address register output to common driver start line. The actual common start line of LCD panel depend on Display Start Common register and SHIFT bit of Display Control register. The register are preset every timing of FLM signal variation in the display line counter. The line counter counts up being synchronized with LP input and generates line addresses which read out sequentially 384 bits data from display RAM to LCD drive circuit.

7.6 Addressing of Display RAM

The EM65566 has built-in bit mapped display RAM. The display RAM consists of 1536 bits (12 bits*128) in the X-direction and 82 bits in the Y-direction. In the gradation display mode, the EM65566 provides segment driver output for 16-gradation display using 4 bits. The three outputs of the segment driver can be used for one pixel of RGB. When connected to an STN color LCD panel, the EM65566 can display 128*82 pixels with 4096 colors (16 gradation * 16 gradation * 16 gradation). The address area in the X-direction depends on the access bus size. In the X-direction, X Address register use to access; and in the Y-direction, Y Address register use to access. Do not specify any address outside the effective address area in each access mode because it is not permitted.

In Gradation Display Mode (MON=”0”)

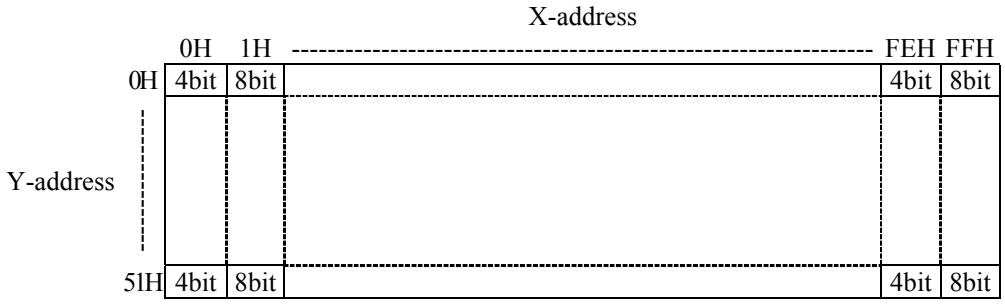
8-bits bus size access

ABS=0

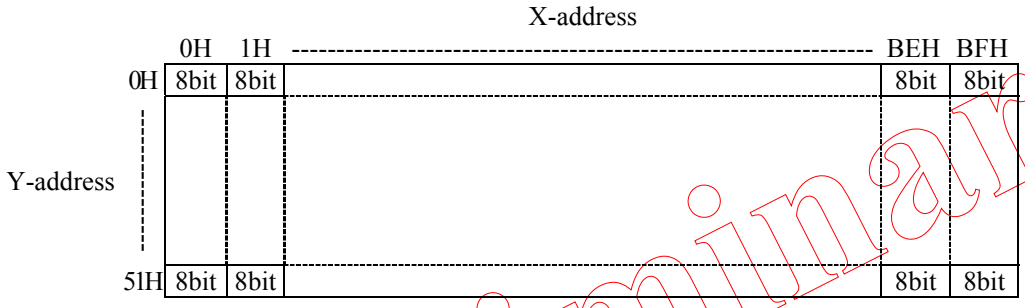
X-address

Y-address	0H	1H	----------	FEH	FFH
0H	7bit	5bit		7bit	5bit
51H	7bit	5bit		7bit	5bit

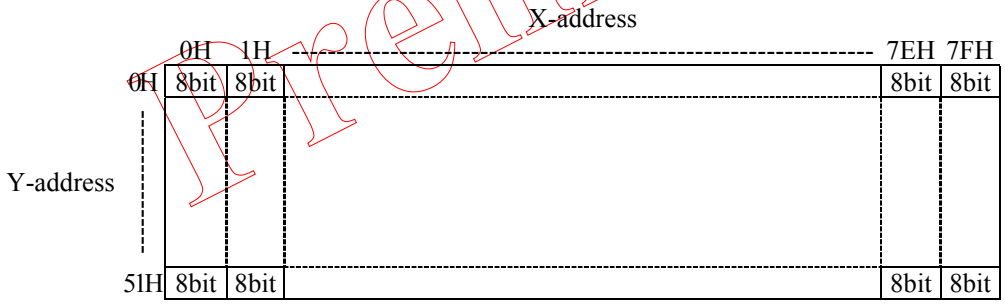
ABS=1



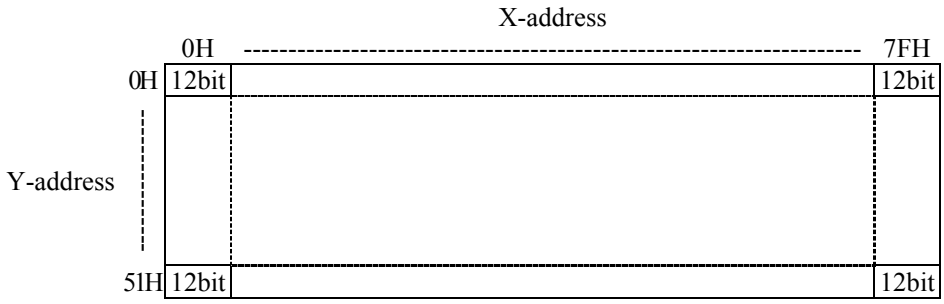
HSW=1



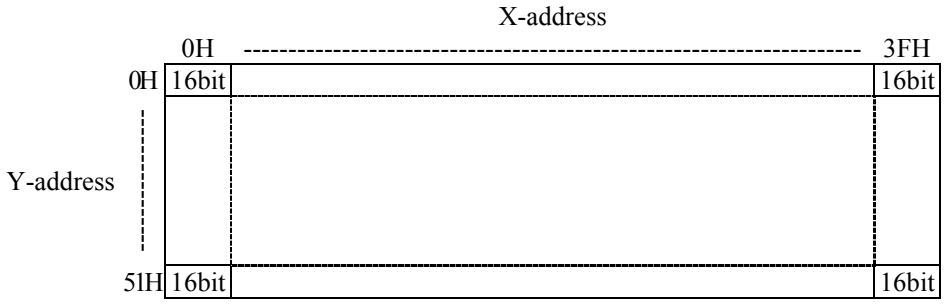
C256=1



16-bits bus size access



C256=1



The addresses, X Address and Y Address are possible to be set up so that they can increment automatically with the address control register. The increment is made every time display RAM is read or written from MPU. In the Y-direction, 384 bits of data are read out to the display data latch circuit by internal operation when the LP rises in a one-line cycle. They are output from the display data latch circuit when the LP fails. When FLM signals being output in one frame cycle are at "H", the values in the display starting line register are preset in the line counter and the line counter counts up at the falling of LP signals. The display line address counter is synchronized with each timing signal of the LCD system to operate and is independent of address counters X and Y.

7.7 Display RAM access using Windows Function

The EM65566 has window area setting command for specified display RAM area access. For use window function, need to set up two position's X and Y address. Also need set up auto increment mode (AXI="1", AYI="1"). Two position means window start position and window end position. The window start position's X and Y address set to normal X address(AX) and Y address(AY) registers. The window end position's X and Y address set to Window X End Address (EX) and Window Y Enc Address (EY) register. In window function access, can use modify write access with set to AIM="1". In case of using window function access, should be set following registers before access to RAM.

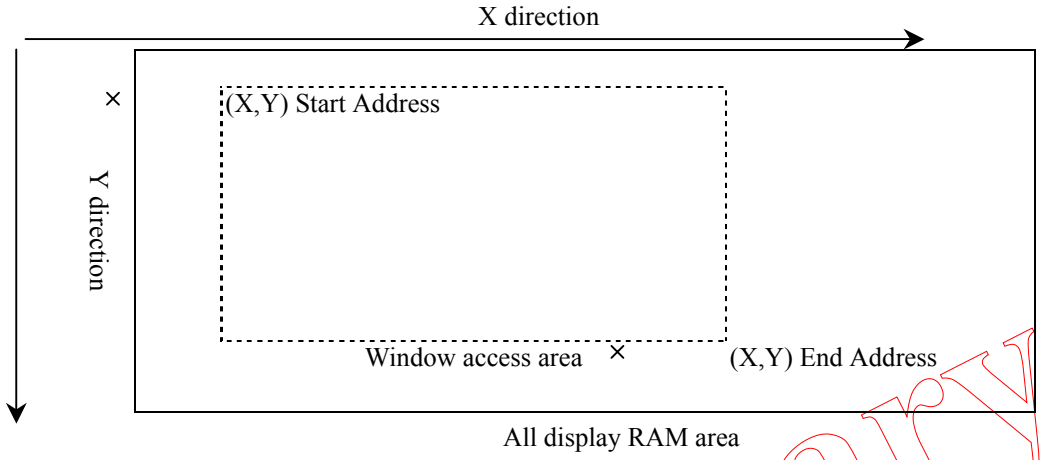
WIN = "1", AXI="1", AYI="1"

X Address, Y Address, Window X End Address, Window Y End Address

Moreover, should be keep following address condition.

Window end X address(EX) ≧ Window start X address (AX)

Window end Y address(EY) ≧ Window start X address (AY)



7.8 Display RAM Data and LCD (only monochrome mode)

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

Normal display (REV=0): RAM data = "0" not lighted

RAM data = "1" lighted

Reverse display (REV=1): RAM data = "0" lighted

RAM data = "1" not lighted

7.9 Segment Display Output Order/Reverse Set up

The order of display output, SEGA0, SEGB0, SEGC0 to SEGA127, SEGB127, and SEGC127 can be reversed. If REF control bit set to "1", display by reversing access to display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling an LCD panel module.

7.10 Relationship between Display RAM and Address

The Display RAM block diagram shows in the figure below:

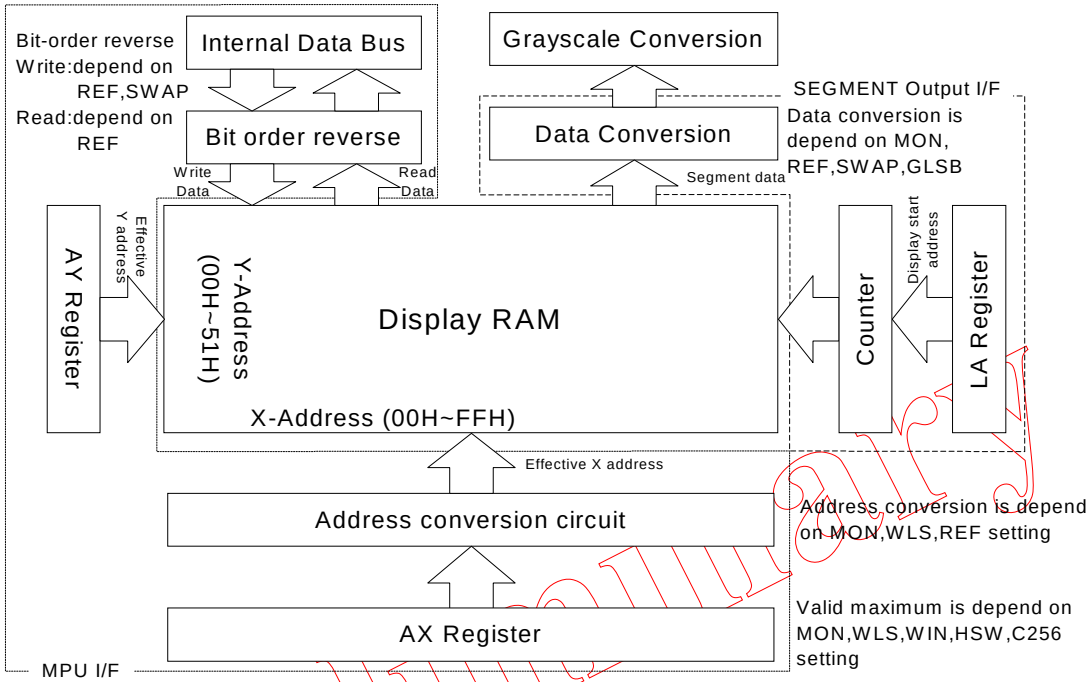


Figure 10. The Display RAM block diagram

The EM65566 execute address conversion that depends on control register setting. In case of auto increment mode, usually AX register is added one. For instance when REF and AXI are both “1”, AX register is added one, but effective X address seems decrement because of address conversion. The effective Y address use AY register values as it is.

(1) Monochrome mode, 8-bits Access mode

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
0	0	0	0	X=00H							X=01H						X=FEH							X=FFH							
0	0	1	1	X=FEH							X=FFH						X=00H							X=01H							
				D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7		D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7				
							SEGA0				SEGB0				SEGC0					SEGA127				SEGB127				SEGC127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
0	0	0	1	X=00H							X=01H						X=FEH							X=FFH							
0	0	1	0	X=FEH							X=FFH						X=00H							X=01H							
				D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7		D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7				
							SEGC0				SEGB0				SEGA0					SEGC127				SEGB127				SEGA127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
0	1	0	0	X=00H				X=01H									X=FEH				X=FFH										
0	1	1	1	X=FEH				X=FFH									X=00H				X=01H										
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7				
							SEGA0				SEGB0				SEGC0					SEGA127				SEGB127				SEGC127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
0	1	0	1	X=00H				X=01H									X=FEH				X=FFH										
0	1	1	0	X=FEH				X=FFH									X=00H				X=01H										
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7				
							SEGC0				SEGB0				SEGA0					SEGC127				SEGB127				SEGA127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
1	*	0	0	X=00H								X=01H									X=BEH								X=BFH			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
							SEGA0				SEGB0				SEGC0				SEGA1					SEGC126				SEGA127				SEGB127				SEGC127

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
1	*	0	1	X=00H								X=01H									X=BEH								X=BFH			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
							SEGC0				SEGB0				SEGA0				SEGC1					SEGA126				SEGC127				SEGB127				SEGA127

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
1	*	1	0	X=BEH				X=BFH								X=BDH								X=BEH				X=01H			
				D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
							SEGC0				SEGB0				SEGA0				SEGC1				SEGB1				SEGA1				SEGC126				

X=02H								X=00H								X=01H			
D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
			SEGB126								SEGA126								SEGC127								SEGB127								SEGA127

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
1	*	1	1	X=BEH				X=BFH								X=BDH								X=BEH				X=01H			
				D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
							SEGA0				SEGB0				SEGC0				SEGA1				SEGB1				SEGC1				SEGA126				

X=02H								X=00H								X=01H			
D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
			SEGB126								SEGC126								SEGA127								SEGB127								SEGC127

(2) Monochrome mode, 16-bits Access mode, Display Start Address = “00H”

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
*	0	0	0	X=00H													X=7FH															
*	0	1	1	X=7FH													X=00H															
				D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15		D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15				
							SEGA0				SEGB0				SEGC0					SEGA127				SEGB127				SEGC127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
*	0	0	1	X=00H													X=7FH															
*	0	1	0	X=7FH													X=00H															
				D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15		D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15				
							SEGC0				SEGB0				SEGA0					SEGC127				SEGB127				SEGA127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
*	1	0	0	X=00H													X=7FH															
*	1	1	1	X=7FH													X=00H															
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11				
							SEGA0				SEGB0				SEGC0					SEGA127				SEGB127				SEGC127			

HSW	ABS	REF	SWAP	X address / Data bus / Segment assign																											
*	1	0	1	X=00H													X=7FH															
*	1	1	0	X=7FH													X=00H															
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11				
							SEGC0				SEGB0				SEGA0					SEGC127				SEGB127				SEGA127			

(3) Gradation mode(4096 color), 8 bits access mode

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																								
0	0	0	0	X=00H							X=01H						X=FEH							X=FFH				
0	0	1	1	X=FEH							X=FFH						X=00H							X=01H				
				D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7		D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7
				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
				SEG A0				SEG B0				SEG C0					SEG A127				SEG B127				SEG C127			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																								
0	0	0	1	X=00H							X=01H						X=FEH							X=FFH				
0	0	1	0	X=FEH							X=FFH						X=00H							X=01H				
				D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7		D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7
				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
				SEG C0				SEG B0				SEG A0					SEG C127				SEG B127				SEG A127			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																								
0	1	0	0	X=00H				X=01H									X=FEH				X=FFH							
0	1	1	1	X=FEH				X=FFH									X=00H				X=01H							
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
				SEG A0				SEG B0				SEG C0					SEG A127				SEG B127				SEG C127			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																			
0	1	0	1	X=00H				X=01H								X=FEH				X=FFH			
0	1	1	0	X=FEH				X=FFH								X=00H				X=01H			
				D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
				SEG C0				SEG B0				SEG A0				SEG C127				SEG B127				SEG A127			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																			
1	*	0	0	X=00H								X=01H				X=BEH				X=BFH			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B				Palette C				Palette A				Palette C				Palette A			
				SEG A0				SEG B0				SEG C0				SEG A1				SEG C126				SEG A127			
				Palette B				Palette C																			
				SEG B127				SEG C127																			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																			
1	*	1	1	X=00H								X=01H				X=BEH				X=BFH			
				D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7
				Palette A				Palette B				Palette C				Palette A				Palette C				Palette A			
				SEG C0				SEG B0				SEG A0				SEG C1				SEG A126				SEG C127			
				Palette B				Palette C																			
				SEG B127				SEG A127																			

HSW	ABS	REF	SWAP
1	*	1	0

X address / Data bus / Palette / Segment assign																							
X=BEH				X=BFH								X=BDH								X=BEH			
D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
SEG C0				SEG B0				SEG A0				SEG C1				SEG B1				SEG A1			

X=01H				X=02H								X=00H								X=01H			
D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3
Palette A				Palette B				Palette C				Palette A				Palette B				Palette C			
SEG C126				SEG B126				SEG A126				SEG C127				SEG B127				SEG A127			

HSW	ABS	REF	SWAP
1	*	1	1

X address / Data bus / Palette / Segment assign												
X=BEH	X=BFH		X=BDH		X=BEH		X=01H	X=02H		X=00H		X=01H
D4 D5 D6 D7	D0 D1 D2 D3	D4 D5 D6 D7	D0 D1 D2 D3	D4 D5 D6 D7	D0 D1 D2 D3		D4 D5 D6 D7	D0 D1 D2 D3	D4 D5 D6 D7	D0 D1 D2 D3	D4 D5 D6 D7	D0 D1 D2 D3
Palette A	Palette B	Palette C	Palette A	Palette B	Palette C		Palette A	Palette B	Palette C	Palette A	Palette B	Palette C
SEG A0	SEG B0	SEG C0	SEG A1	SEG B1	SEG C1		SEG A126	SEG B126	SEG C126	SEG A127	SEG B127	SEG C127

(4) Gradation mode(4096 color), 16 bits access mode

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign						
*	0	0	0	X=00H				X=7FH		
*	0	1	1	X=7FH				X=00H		
				D1 D2 D3 D4	D7 D8 D9 D10	D12 D13 D14 D15		D1 D2 D3 D4	D7 D8 D9 D10	D12 D13 D14 D15
				Palette A	Palette B	Palette C		Palette A	Palette B	Palette C
				SEG A0	SEG B0	SEG C0		SEG A127	SEG B127	SEG C127

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign						
*	0	0	1	X=00H				X=7FH		
*	0	1	0	X=7FH				X=00H		
				D1 D2 D3 D4	D7 D8 D9 D10	D12 D13 D14 D15		D15 D14 D13 D12	D10 D9 D8 D7	D4 D3 D2 D1
				Palette A	Palette B	Palette C		Palette A	Palette B	Palette C
				SEG C0	SEG B0	SEG A0		SEG C127	SEG B127	SEG A127

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																							
*	1	0	0	X=00H												X=7FH											
*	1	1	1	X=7FH												X=00H											
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
				SEG A0				SEG B0				SEG C0					SEG A127				SEG B127				SEG C127			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / Segment assign																							
*	1	0	1	X=00H												X=7FH											
*	1	1	0	X=7FH												X=00H											
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
				Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
				SEG C0				SEG B0				SEG A0					SEG C127				SEG B127				SEG A127			

(5)Gradation mode(256 Color) ,(C256=1)

8-bit mode(WLS=0)

HSW	ABS	REF	SWAP	X address / Data bus / Palette / palette bit / Segment assign																							
*	*	0	0	X=00H												X=7FH											
*	*	1	1	X=7FH												X=00H											
				D0	D1	D2	D3	D4	D5	D6	D7						D0	D1	D2	D3	D4	D5	D6	D7				
				Palette A		Palette B			Palette C								Palette A		Palette B			Palette C						
				A2	A3	B1	B2	B3	C1	C2	C3						A2	A3	B1	B2	B3	C1	C2	C3				
				SEG A0		SEG B0			SEG C0								SEG A127		SEG B127			SEG C127						

HSW	ABS	REF	SWAP	X address / Data bus / Palette / palette bit / Segment assign																											
*	*	0	1	X=00H														X=7FH													
*	*	1	0	X=7FH														X=00H													
				D0	D1	D2	D3	D4	D5	D6	D7							D0	D1	D2	D3	D4	D5	D6	D7						
				Palette A			Palette B			Palette C								Palette A			Palette B			Palette C							
				A2	A3	B1	B2	B3	C1	C2	C3							A2	A3	B1	B2	B3	C1	C2	C3						
				SEG C0			SEG B0			SEG A0								SEG C127			SEG B127			SEG A127							

16-bit mode(WLS=1)

HSW	ABS	REF	SWAP	X address / Data bus / Palette / palette bit / Segment assign																											
*	*	0	0	X=00H														X=3FH													
*	*	1	1	X=3FH														X=00H													
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				Palette A		Palette B		Palette C		Palette A		Palette B		Palette C						Palette A		Palette B		Palette C		Palette A		Palette B		Palette C			
				A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3
				SEG A0		SEG B0		SEG C0		SEG A1		SEG B1		SEG C1						SEG A126		SEG B126		SEG C126		SEG A127		SEG B127		SEG C127			

HSW	ABS	REF	SWAP	X address / Data bus / Palette / palette bit / Segment assign																											
*	*	0	1	X=00H														X=3FH													
*	*	1	0	X=3FH														X=00H													
				D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
				Palette A		Palette B		Palette C		Palette A		Palette B		Palette C						Palette A		Palette B		Palette C		Palette A		Palette B		Palette C			
				A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3	A2	A3	B1	B2	B3	C1	C2	C3
				SEG A1		SEG B1		SEG C1		SEG A0		SEG B0		SEG C0						SEG A127		SEG B127		SEG C127		SEG A126		SEG B126		SEG C126			

(6)Data read and write bit assignment

In 16-bit data bus mode

ABS=0	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Read	D15	D14	D13	D12	1	D10	D9	D8	D7	1	1	D4	D3	D2	D1	1

ABS=1	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Read	1	1	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ABS=*	C256=1	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		Read	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

In 8-bit data bus mode

ABS=0	HSW=0	C256=0	Address	00,02,04……FC,FEH								01,03,05……FD,FFH						
			Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D7	D6	D5	D4	1	D2	D1	D0	D7	1	1	D4	D3	D2	D1	1

ABS=1	HSW=0	C256=0	Address	00,02,04……FC,FEH								01,03,05……FD,FFH						
			Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
			Read	1	1	1	1	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

ABS=0	HSW=1	C256=0	Address	00,01,02……BD,BE,BFH					
			Write	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D7	D6	D5	D4	D3	D2	D1	D0

ABS=0	HSW=0	C256=1	Address	00,01,02……7D,7E,7FH					
			Write	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D7	D6	D5	D4	D3	D2	D1	D0

7.11 Display Data Structure and Gradation Control

For the purpose of gradation control, one pixel requires multiple bits of display RAM. The EM65566 has 4-bit data per output to achieve the gradation display.

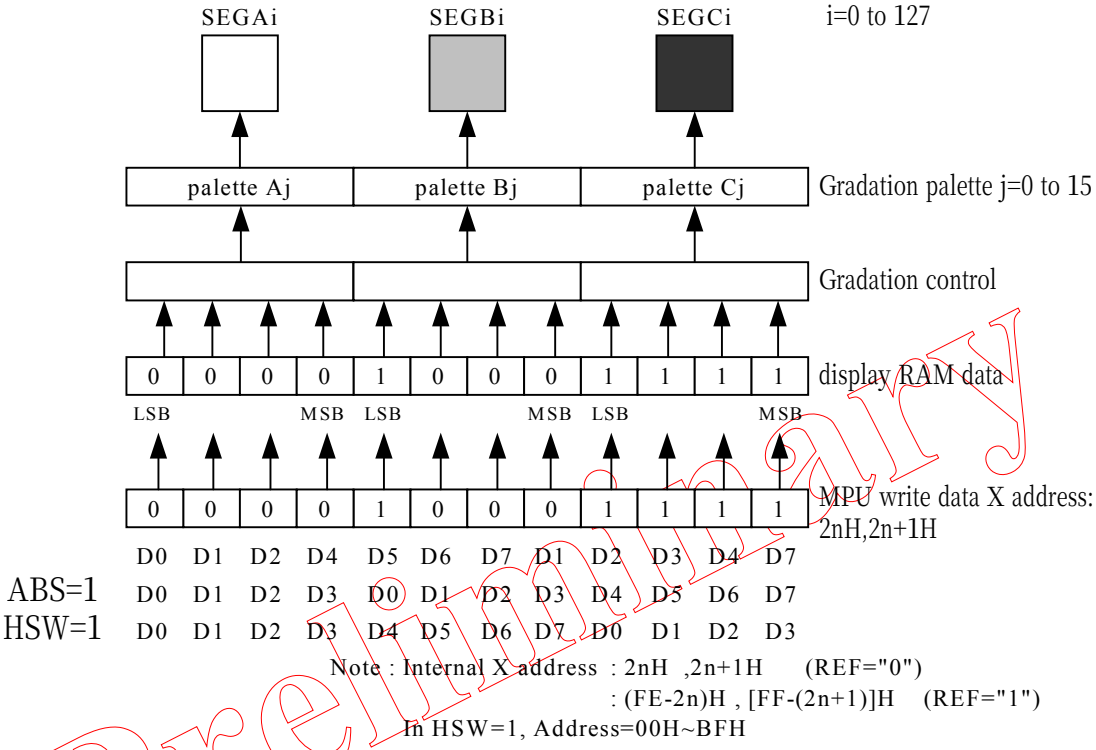
The three outputs of the segment driver are used for one pixel of RGB, and the EM65566 is connected to an STN color LCD panel. It can display 128*82 pixels with 4096 colors (4 bits * 4 bits * 4 bits). In this case, since the gradation display data is processed by a single access to the memory, the data can be rewritten fast and naturally.

The weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM.

(1) Gradation mode (4096 color)

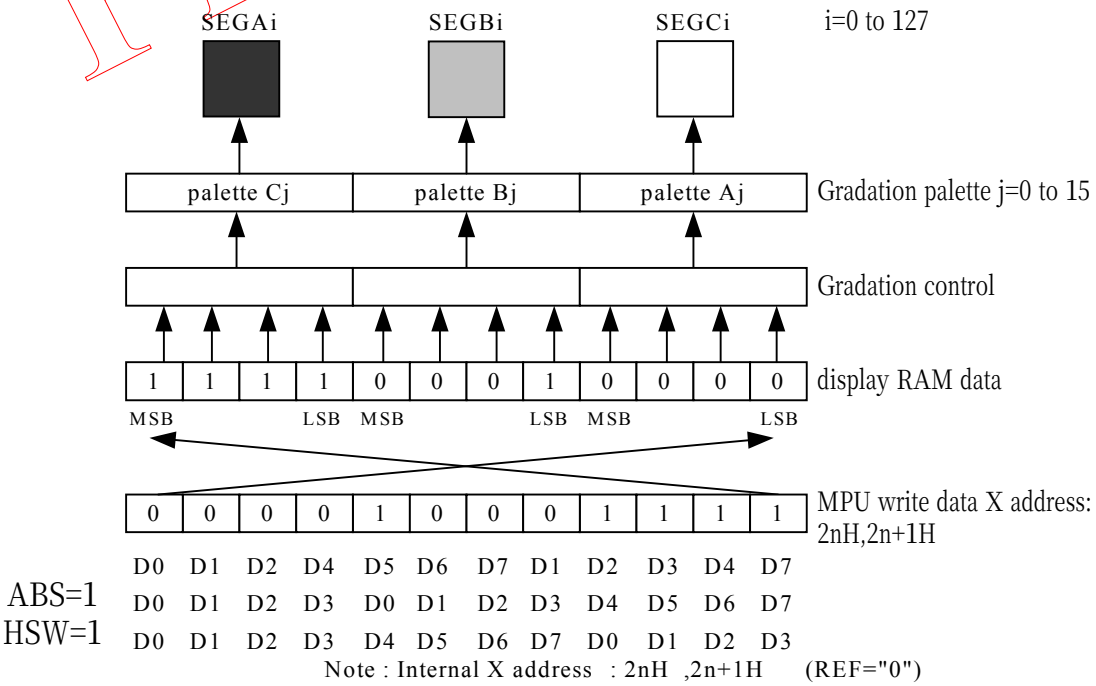
8-bit mode

- (REF, SWAP)=(0,0) or (1,1)



Note : Internal X address : 2nH ,2n+1H (REF="0")
: (FE-2n)H , [FF-(2n+1)]H (REF="1")
In HSW=1, Address=00H~BFH

- (REF, SWAP)=(0,1) or (1,0)

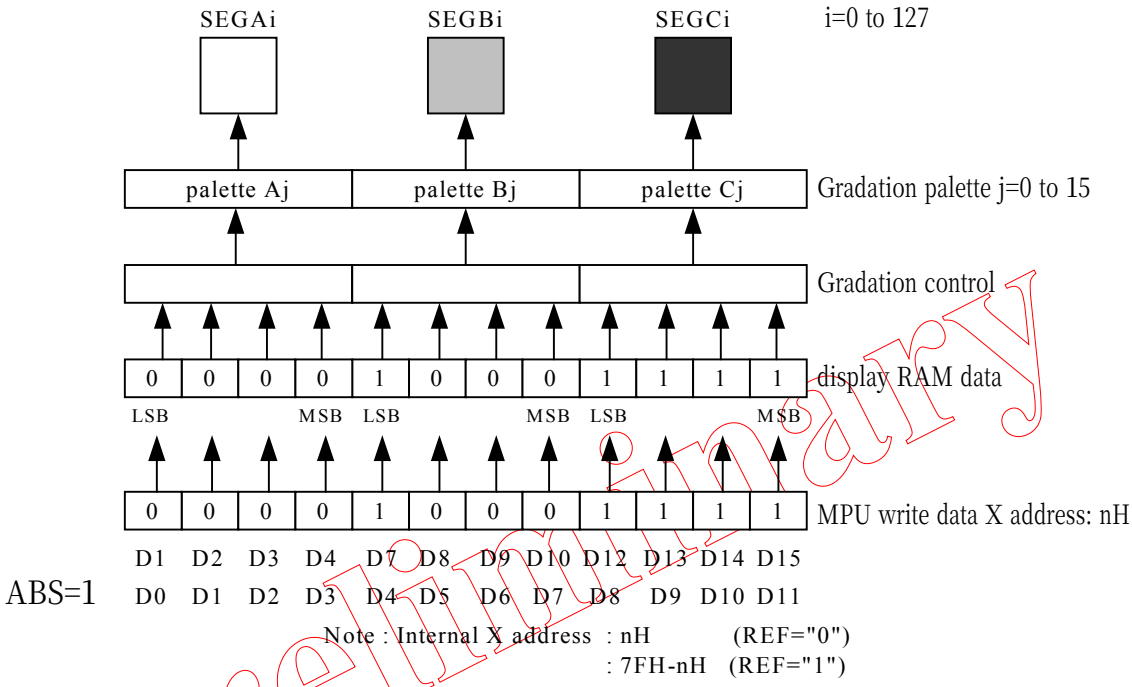


Note : Internal X address : 2nH ,2n+1H (REF="0")
: (FE-2n)H , [FF-(2n+1)]H (REF="1")
In HSW=1, Address=00H~BFH

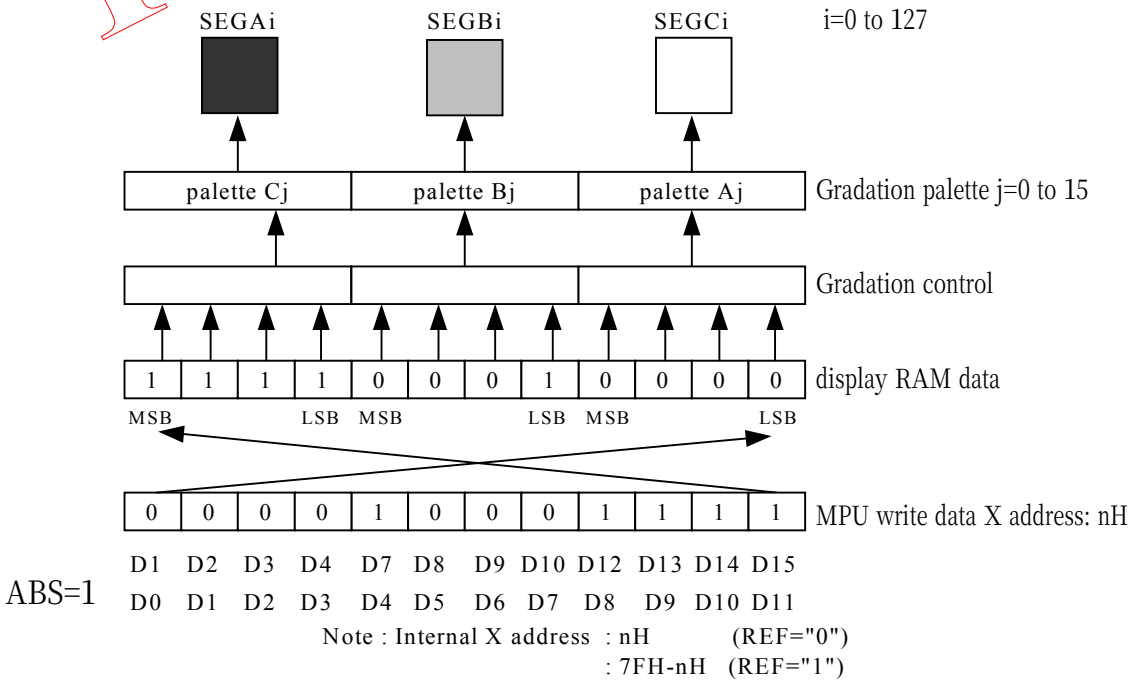
16-bit mode

In 16-bits access, the weighting for each data bit is dependent on the status of the SWAP bit and the REF bit that is selected when data is written to the display RAM, as in the case with 8-bits access.

- (REF, SWAP)=(0,0) or (1,1)



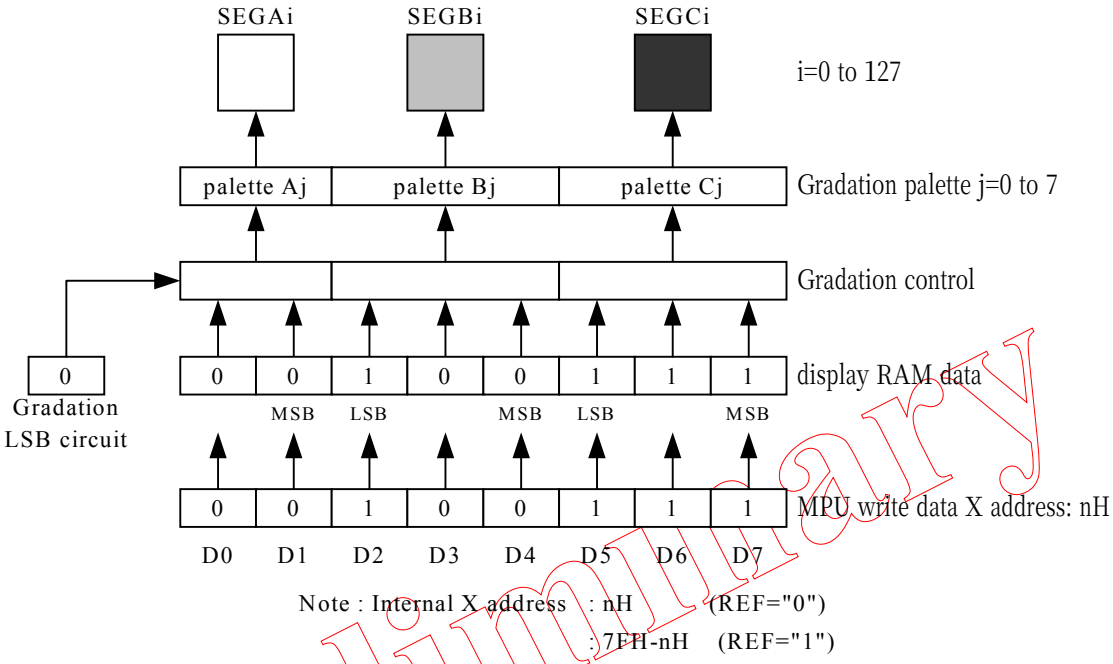
- (REF, SWAP)=(0,1) or (1,0)



(2)Gradation mode (256 color) ,C256=1

8-bit mode(WLS=0)

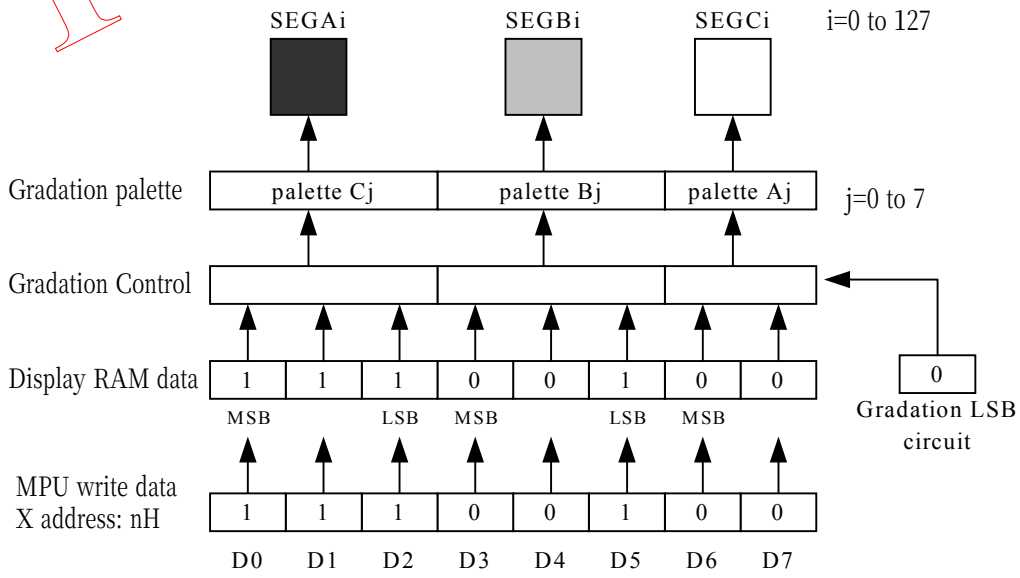
(REF, SWAP)=(0,0) or (1,1)



Note : Internal X address : nH (REF="0")

: 7FH-nH (REF="1")

(REF, SWAP)=(0,1) or (1,0)

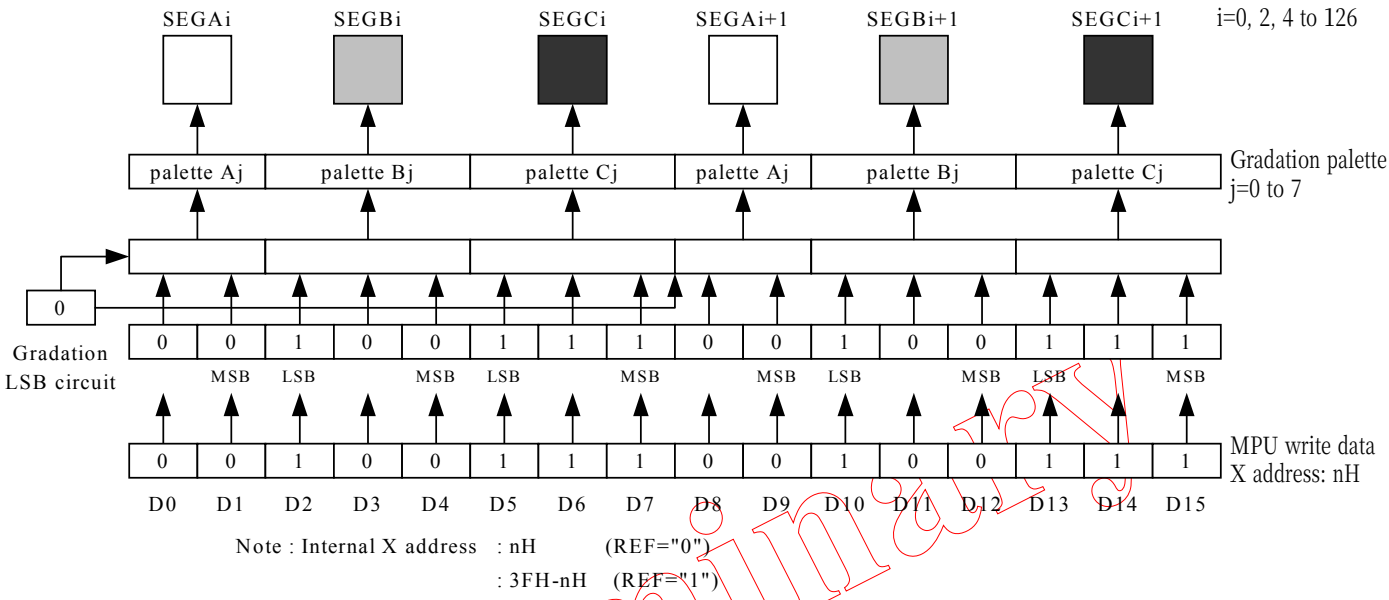


Note : Internal X address : nH (REF="0")

: 7FH-nH (REF="1")

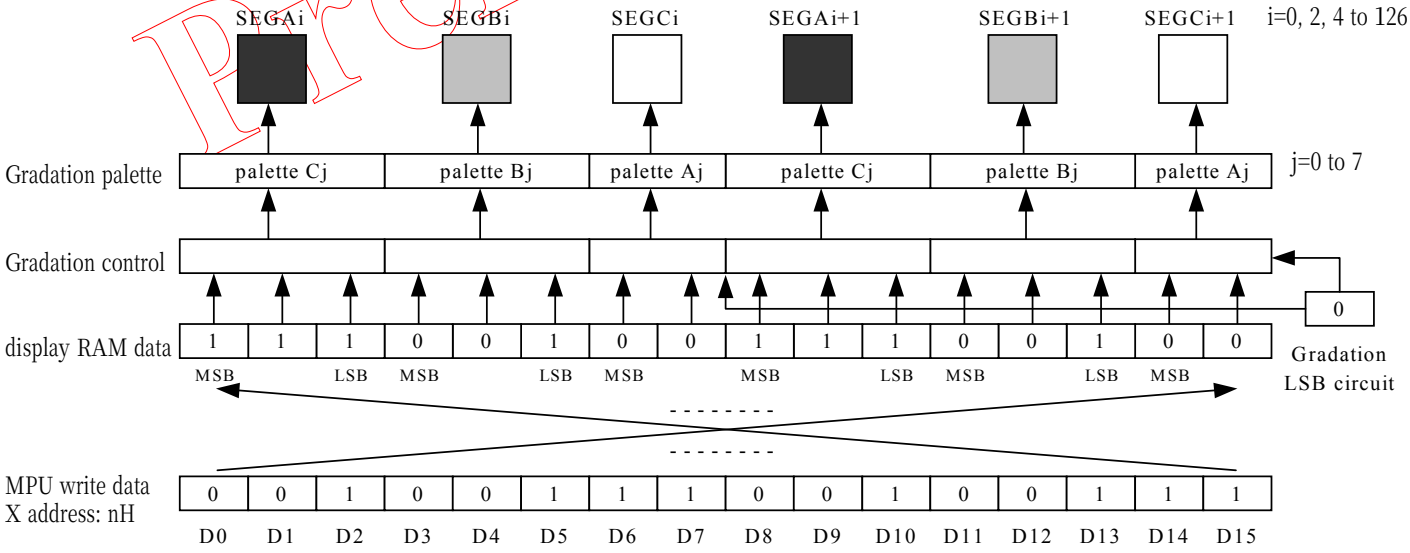
16-bit mode(WLS=1)

(REF, SWAP)=(0,0) or (1,1)



Note : Internal X address : nH (REF="0")
: 3FH-nH (REF="1")

(REF, SWAP)=(0,1) or (1,0)

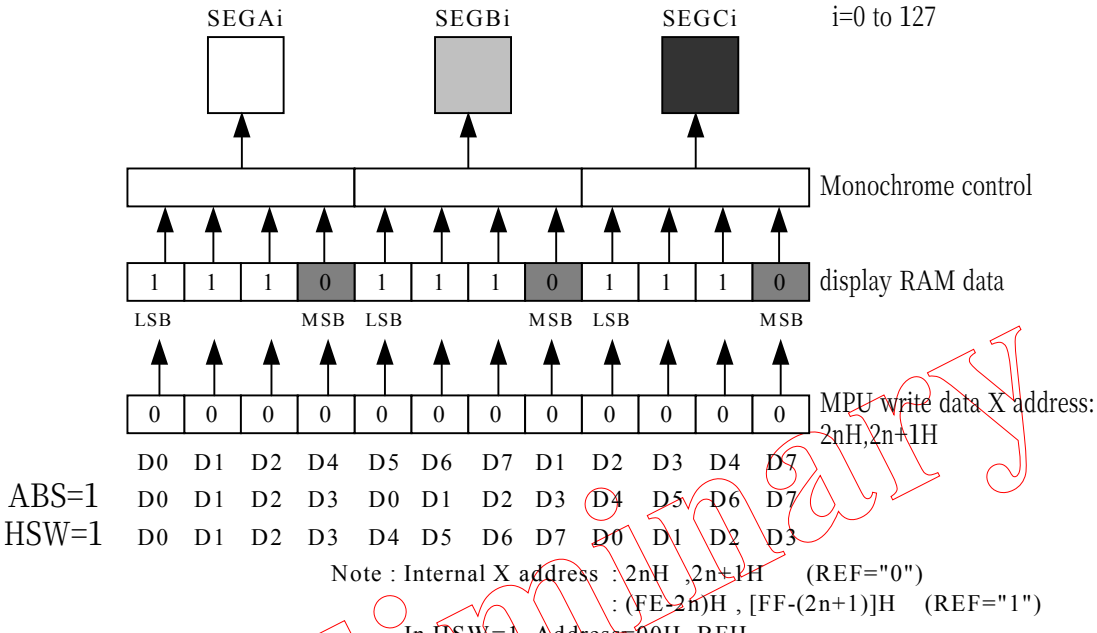


Note : Internal X address : nH (REF="0")
: 3FH-nH (REF="1")

(3)Monochrome mode

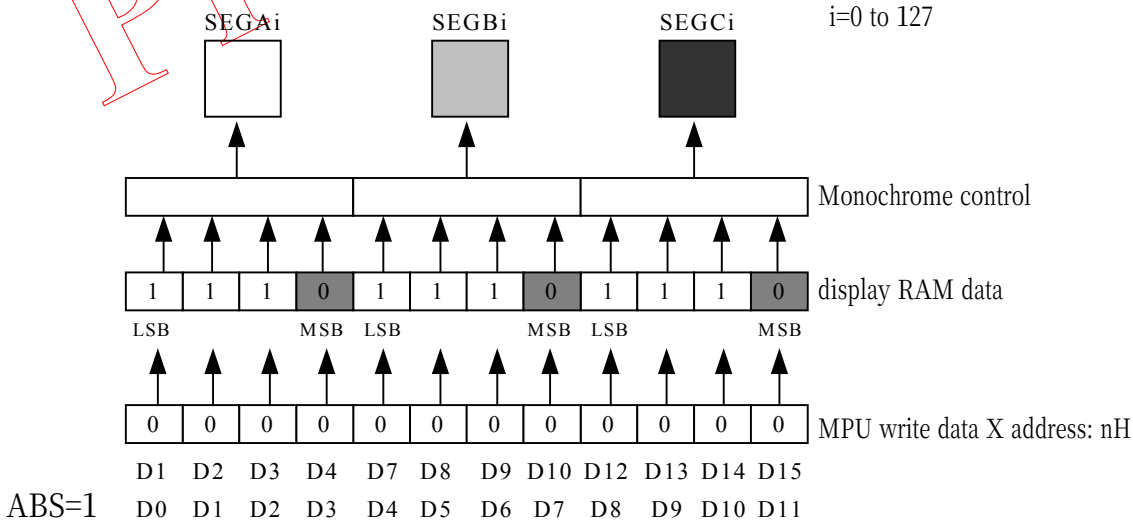
In the monochrome mode, only three MSB in each display data are valid, the RAM mapping is the same gradation display mode.

8-bit mode



Note : Internal X address : 2nH ,2n+1H (REF="0")
: (FE-2n)H , [FF-(2n+1)]H (REF="1")
In HSW=1, Address=00H~BFH

16-bit mode



Note : Internal X address : nH (REF="0")
: 7FH-nH (REF="1")

7.12 Gradation LSB Control

In 256 color mode(C256=1), the EM65566 provides segment driver output for 8-gradation display using 3-bits and that for 4-gradation display using 2-bits.
The segment driver output for the 4-gradation display uses 2-bits written to the corresponding RAM area and 1-bit supplemented by the gradation LSB circuit, and then selects 4-gradation form 8-gradation.

In 256 color mode(C256=1), the segment driver output for the 4-gradation display result in a gradation level of 0 regardless of the gradation LSB, when 2-bits of data on the display RAM are “00”. When 2-bits of data on the display RAM is “11”,a gradation level of 7/7 is selected regardless of the bit information of the gradation LSB.The other gradation levels are selected depending on 2-bits of data on the display RAM and the gradation LSB bits.
One bit of data is supplemented by setting the gradation LSB register (GLSB).
The Gradation LSB control bit applied to all 4-gradation segment drivers.
Gradation LSB = “0”: Selects 0 as the LSB information on the RAM for 4-gradation segment drivers.
Gradation LSB = “1”: Selects 1 as the LSB information on the RAM for 4-gradation segment drivers.

7.13 Gradation Palette

The EM65566 has two gradation display modes, the gradation fixed display mode and the gradation variable display mode. Select either of the two modes using the gradation display mode register.

PWM = “0”: Selects the variable display mode using 16 gradation selected from 32 gradation. (C256=0)
Selects the variable display mode using 8 gradation selected from 32 gradation. (C256=1)
PWM = “1”: Selects the fixed display mode using specific 16 gradation. (C256=0)
Selects the fixed display mode using specific 8 gradation. (C256=1)

To select the best gradation level suited to the LCD panel, use the gradation palette register among the 32-level gradation palettes in the gradation variable display mode. The segment driver output is set up by the selected 16-levels of gradation palettes.

The gradation palette register provides three registers for the SEGAi (0-127) group, SEGBi (0-127) group, and SEGCi (0-127) group of segment driver outputs [palettes Aj, Bj, and Cj (j = 0-15)]. Each register consists of a 5-bit register, selecting 16-gradations from the pattern for 32-gradations.

Caution: Different gradation levels can't be set in the same palette.

Initial values on gradation palette register

Gradation mode (C256=0)

[Three groups of palettes Aj, Bj, and Cj (j = 0-15) are available]

(MSB)RAM data(LSB)				Register Name	Initial value
0	0	0	0	Palette0	00000
0	0	0	1	Palette1	00011
0	0	1	0	Palette2	00101
0	0	1	1	Palette3	00111
0	1	0	0	Palette4	01001
0	1	0	1	Palette5	01011
0	1	1	0	Palette6	01101
0	1	1	1	Palette7	01111
1	0	0	0	Palette8	10001
1	0	0	1	Palette9	10011
1	0	1	0	Palette10	10101
1	0	1	1	Palette11	10111
1	1	0	0	Palette12	11001
1	1	0	1	Palette13	11011
1	1	1	0	Palette14	11101
1	1	1	1	Palette15	11111

256 color mode (C256=1)

[Three groups of palettes Aj, Bj, and Cj (j = 0-7) are available]

(MSB)RAM data(LSB)			Register Name	Initial value
0	0	0	Palette0	00000
0	0	1	Palette1	00101
0	1	0	Palette2	01010
0	1	1	Palette3	01110
1	0	0	Palette4	10001
1	0	1	Palette5	10001
1	1	0	Palette6	11010
1	1	1	Palette7	11111

Gradation level table (PWM = “0”, variable mode , MON= “0”)

[Three groups of palettes Aj, Bj, and Cj (j = 0-15) are available

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0	0	gradation palette0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	gradation palette8 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	gradation palette1 initial value	1 0 0 1 1	19/31	gradation palette9 initial value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	gradation palette2 initial value	1 0 1 0 1	21/31	gradation palette10 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7//31	gradation palette3 initial value	1 0 1 1 1	23/31	gradation palette11 initial value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	gradation palette4 initial value	1 1 0 0 1	25/31	gradation palette12 initial value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	gradation palette5 initial value	1 1 0 1 1	27/31	gradation palette13 initial value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	gradation palette6 initial value	1 1 1 0 1	29/31	gradation palette14 initial value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 0	15/31	gradation palette7 initial value	1 1 1 1 1	31/31	gradation palette15 initial value

256 color mode (C256=1)

[Three groups of palettes Aj, Bj, and Cj (j = 0-7) are available

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0	0	256 color palette0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	256 color palette4 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	256 color palette1 initial value	1 0 1 0 1	21/31	256 color palette5 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7//31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	256 color palette2 initial value	1 1 0 1 0	26/31	256 color palette6 initial value
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	256 color palette3 initial value	1 1 1 1 0	30/31	
0 1 1 1 0	15/31		1 1 1 1 1	31/31	256 color palette7 initial value

Gradation level table (PWM = "1", fixed mode , MON= "0", C256= "0")

(MSB)RAM data(LSB)				Gradation Level
0	0	0	0	0
0	0	0	1	1/15
0	0	1	0	2/15
0	0	1	1	3/15
0	1	0	0	4/15
0	1	0	1	5/15
0	1	1	0	6/15
0	1	1	1	7/15
1	0	0	0	8/15
1	0	0	1	9/15
1	0	1	0	10/15
1	0	1	1	11/15
1	1	0	0	12/15
1	1	0	1	13/15
1	1	1	0	14/15
1	1	1	1	15/15

Gradation level table (PWM = "1", fixed mode , MON= "0", C256= "1")

(MSB)RAM data(LSB)				Gradation Level
0	0	0	*	0
0	0	1	*	1/7
0	1	0	*	2/7
0	1	1	*	3/7
1	0	0	*	4/7
1	0	1	*	5/7
1	1	0	*	6/7
1	1	1	*	7/7

Monochrome mode , MON= "1"

(MSB)RAM data(LSB)				Gradation Level
0	*	*	*	0
1	*	*	*	1

*: don't care

7.14 Display Timing Circuit

The display timing circuit generates internal signals and timing pulses (LP, FLM, M and CLK) by clock. It can select external input (CK) or internal oscillation.

By setting up Master/Slave mode (M/S), the state of timing pulse pins and the timing generator changes.

M/S Pin	Mode	LP Pin	M Pin	FLM Pin	CLK Pin	State of timing generator
L	Slave	Input	Input	Input	Input	LP,FLM,M generation stop
H	Master	Output	Output	Output	Output	Operation state

Display timing pulse pins and Generator State

7.15 Signal Generation to Display Line Counter, and Display Data Latching Circuit

Both the clock to the line counter and clock to display data latching circuit from the display clock (LP) are generated. Synchronized with the display clock (LP), the line addresses of Display RAM are generated and 384-bits display data are latched to display data latching circuit to output to the LCD drive circuit (Segment outputs). Read-out of the display data to the LCD drive circuit is completely independent of MPU. Therefore, MPU that has no relationship the read-out operation of the display data can access.

7.16 Generation of the Alternated Signal (M) and the Synchronous Signal (FLM)

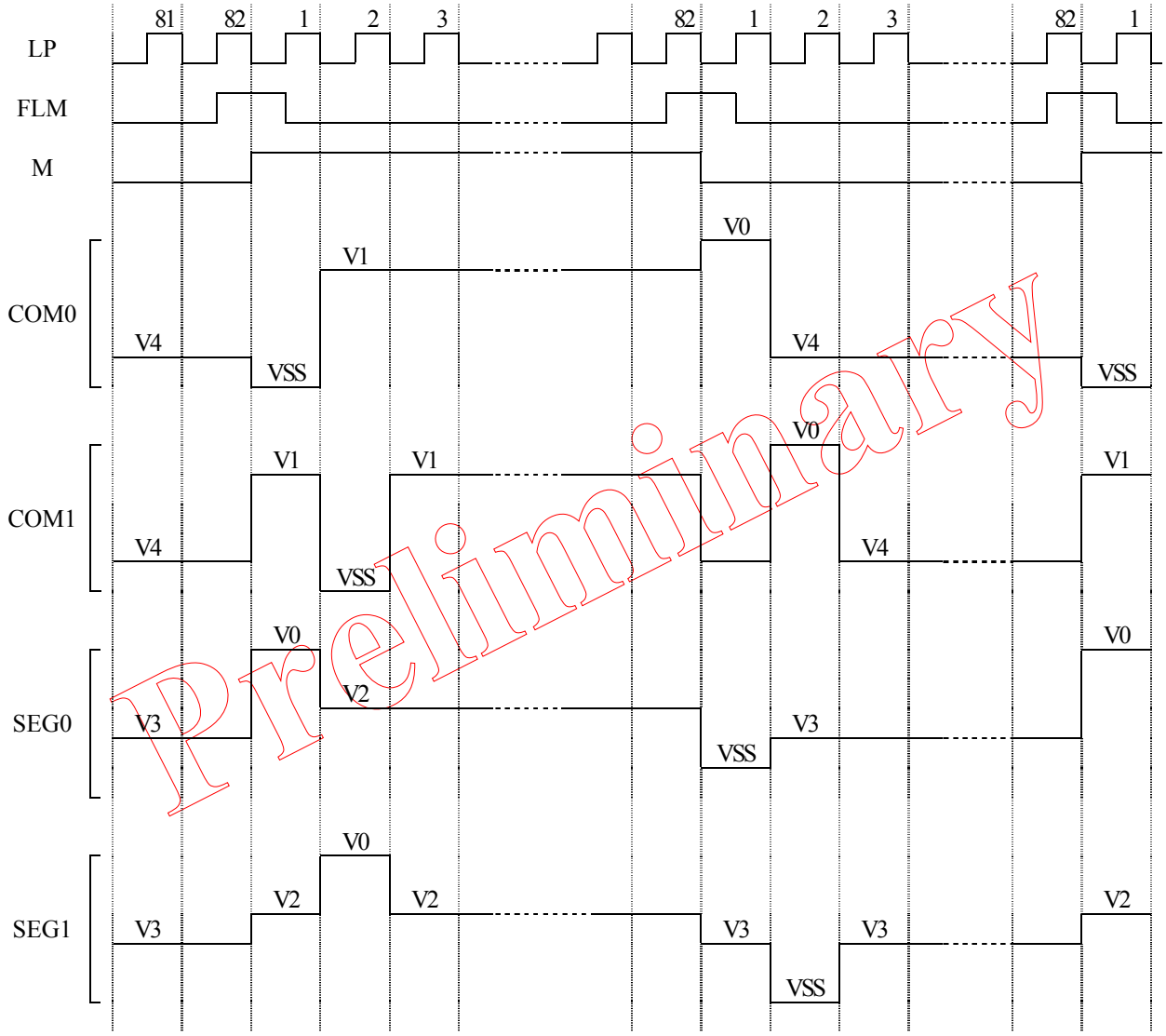
LCD alternated signal (M) and synchronous signal (FLM) are generated by the display clock (LP). The FLM generates alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame (M-signal level is reversed every one frame). However, by setting up data (n-1) in an n-line reverse register and n-line alternated control bit (NLIN) at “1”, n-line reverse waveform is generated. When the EM65566 is used in multi chip system, master chip must provide LP, FLM, and M signals for the slave chip.

7.17 Display Data Latching Circuit

Display data latching Circuit temporally latches display data that is output display data to LCD driver circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display all on functions are operated by controlling data in display data latch. Therefore, no data within display RAM changes.

7.18 Output Timing of LCD Driver

Display timing at Normal mode (not reverse mode), 1/82 DUTY, and on monochrome mode.



7.19 LCD Drive Circuit

This drive circuit generates four levels LCD drive voltage. The circuit has 384 segment outputs and 82 common outputs and outputs combined display data and M signal. Two of common outputs, COMA and COMB, are special outputs. The COMA and COMB outputs be not influenced by partial setting. Mainly use for display. The common drive circuit that has shift register sequentially outputs common scan signals.

7.20 Special Segment Driver Circuit

The EM65566 has each three special segment circuit (DSEGA0, DSEGB0, DSEGC0, DSEGA1, DSEGB1, and DSEGC1) at both side of Segment Driver Circuit. These special segment drivers are useful to display frame. The normal segment drivers correspond to the display RAM data, but special segment drivers correspond to the register data. The EM65566 have two registers for special segment circuit. These two registers are both 12 bits. One register corresponds to DSEGA0, DSEGB0, DSEGC0 output pins, another register corresponds to DSEGA1, DSEGB1, and DSEGC1 output pins. In all common timing special segment output makes same output. The gradation palette for DSEGA0, DSEGA1 corresponds to gradation palette for SEGA0-SEGA127. The gradation palette for DSEGB0, DSEGB1 corresponds to gradation palette for SEGB0-SEGB127.The gradation palette for DSEGC0, DSEGC1 corresponds to gradation palette for SEGC0-SEGC127. The special segment driver output depend on ALLON and REV register setting, not depend on LREV register setting. A DMY register set to “1” then can access register that corresponded to special segment driver.

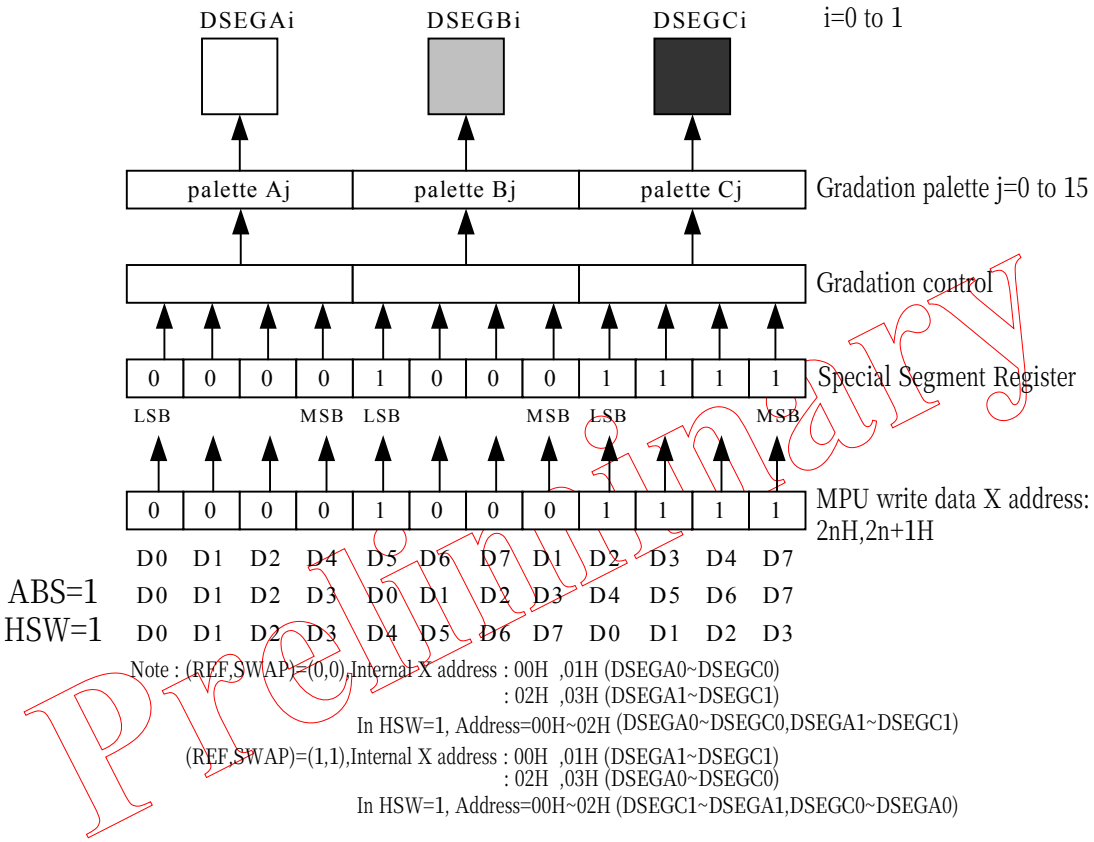
RS	DMY	68-family R/WB	80-family		Function
			RDB	WRB	
0	0	1	0	1	Display RAM read
0	0	0	1	0	Display RAM write
0	1	1	0	1	Special segment register read
0	1	0	1	0	Special segment register write

Accessing to special segment register use same method with display RAM access.
It is necessary to access that set X address, but Y address doesn’t need setup. Available X address for special segment register are 00H and 01H in 8 bits access mode, 00H in 16 bits access mode. In this case (DMY=”1”), address auto increment function doesn’t work. Each access needs each address.
Moreover, reading of special segment register has same limitation as display RAM reading. It need dummy reading. (See 6-2)

(1)Gradation mode (4096 color)

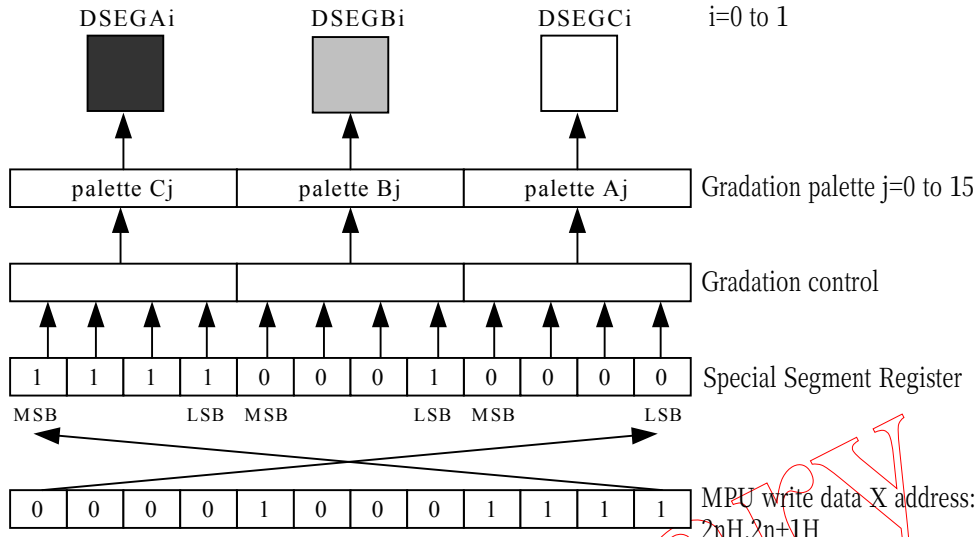
8 bits bus access

(REF, SWAP) = (0, 0) (1,1)



Note : (REF,SWAP)=(0,0),Internal X address : 00H ,01H (DSEGA0~DSEGC0)
: 02H ,03H (DSEGA1~DSEGC1)
In HSW=1, Address=00H~02H (DSEGA0~DSEGC0,DSEGA1~DSEGC1)
(REF,SWAP)=(1,1),Internal X address : 00H ,01H (DSEGA1~DSEGC1)
: 02H ,03H (DSEGA0~DSEGC0)
In HSW=1, Address=00H~02H (DSEGC1~DSEGA1,DSEGC0~DSEGA0)

(REF, SWAP) = (0, 1) (1,0)



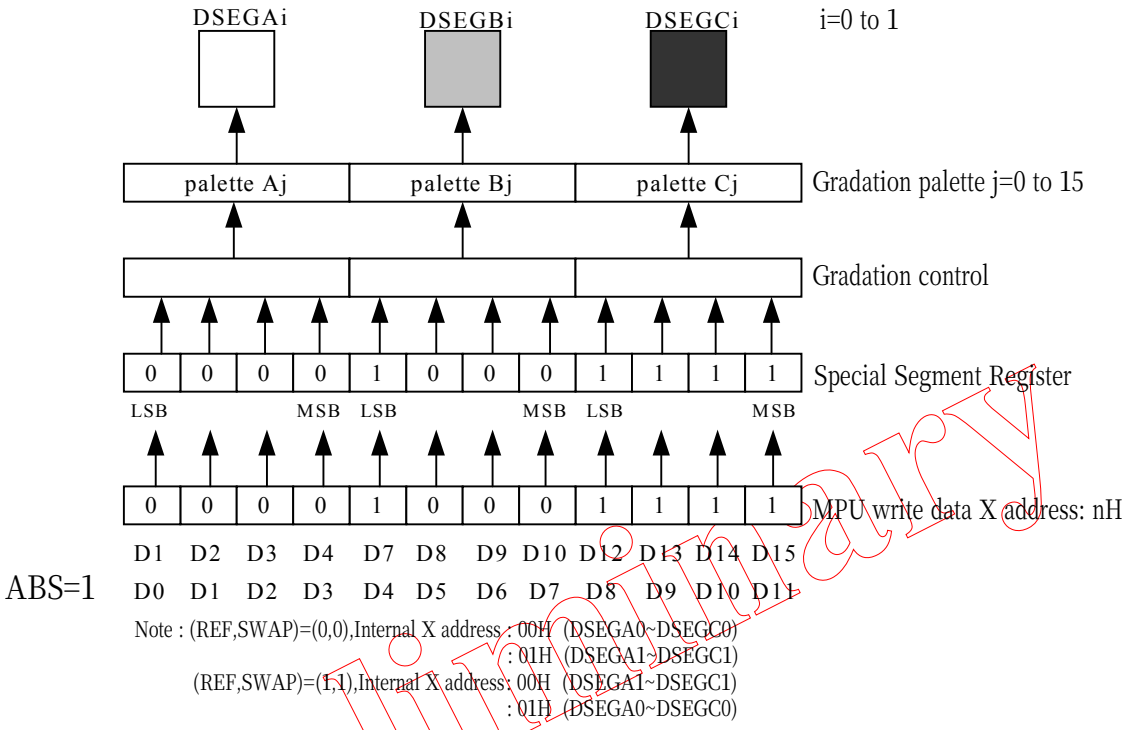
ABS=1
HSW=1

D0	D1	D2	D4	D5	D6	D7	D1	D2	D3	D4	D7
D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7
D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3

Note : (REF,SWAP)=(0,1),Internal X address : 00H ,01H (DSEGA0~DSEGC0)
: 02H ,03H (DSEGA1~DSEGC1)
In HSW=1, Address=00H~02H (DSEGA0~DSEGC0,DSEGA1~DSEGC1)
(REF,SWAP)=(1,0),Internal X address : 00H ,01H (DSEGA1~DSEGC1)
: 02H ,03H (DSEGA0~DSEGC0)
In HSW=1, Address=00H~02H (DSEGC1~DSEGA1,DSEGC0~DSEGA0)

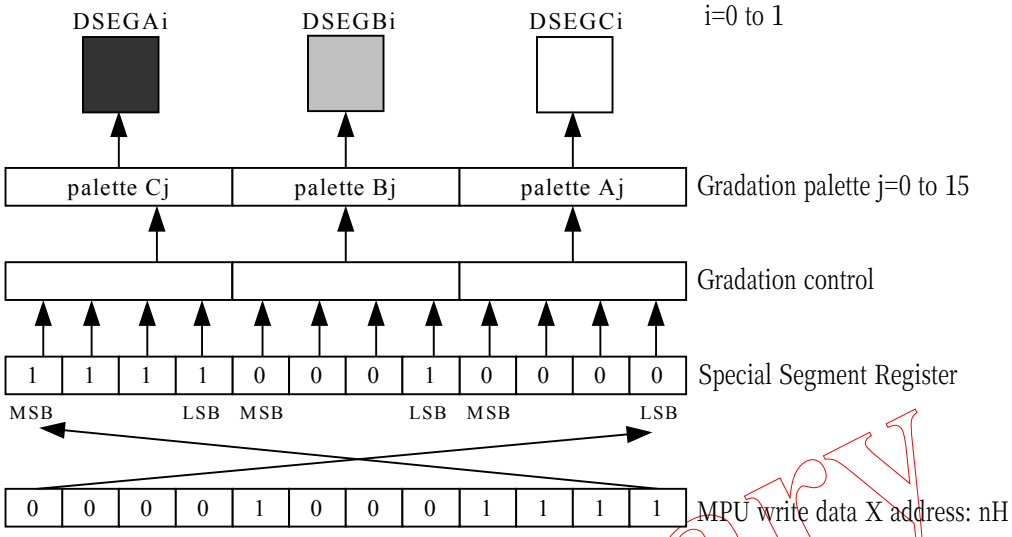
16 bits bus access

(REF, SWAP) = (0, 0) (1,1)



Note : (REF,SWAP)=(0,0),Internal X address : 00H (DSEGA0~DSEGC0)
: 01H (DSEGA1~DSEGC1)
(REF,SWAP)=(1,1),Internal X address: 00H (DSEGA1~DSEGC1)
: 01H (DSEGA0~DSEGC0)

(REF, SWAP) = (0, 1) (1,0)



ABS=1

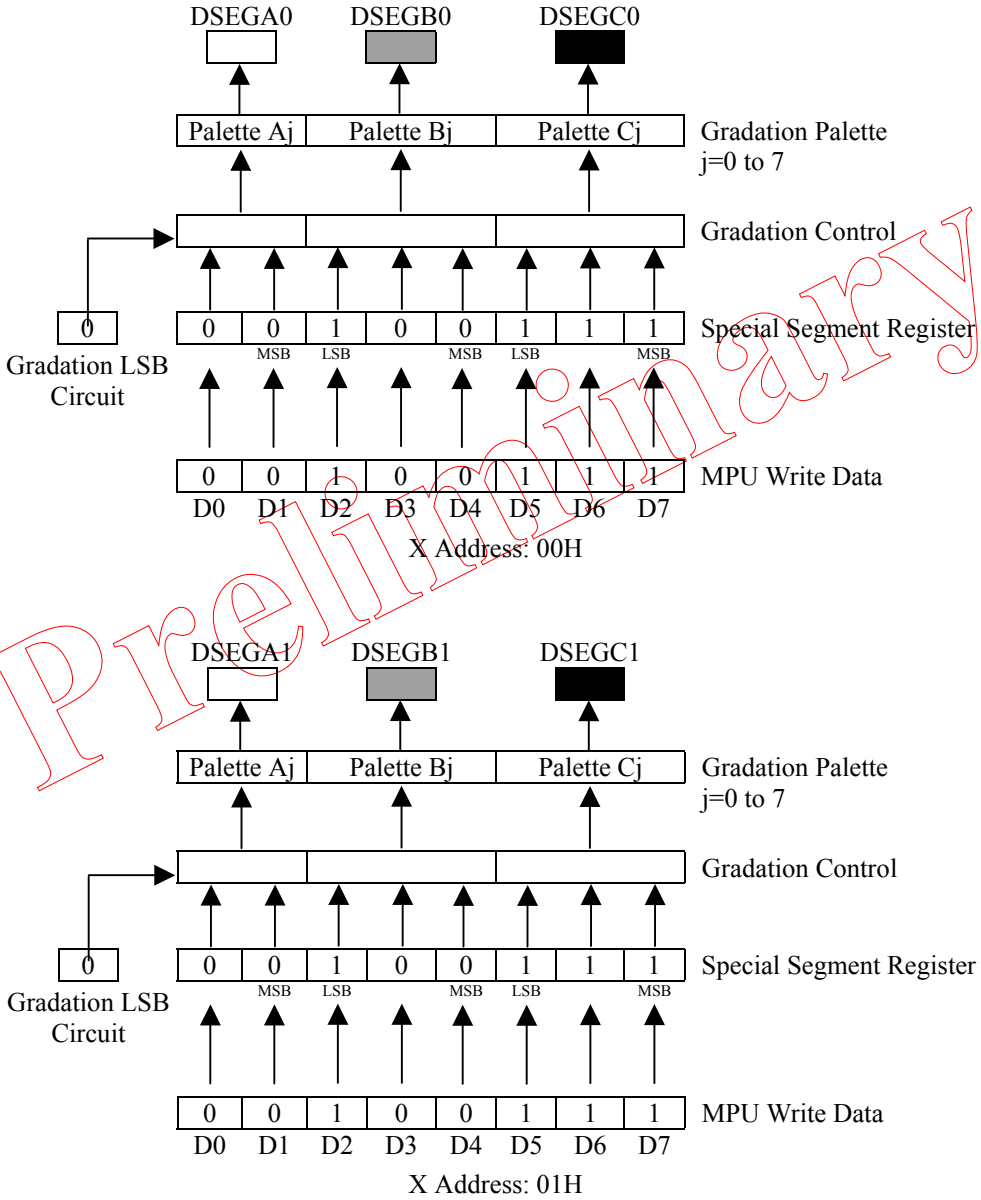
D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15
D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11

Note : (REF,SWAP)=(0,1),Internal X address : 00H (DSEGA0~DSEGC0)
: 01H (DSEGA1~DSEGC1)
(REF,SWAP)=(1,0),Internal X address: 00H (DSEGA1~DSEGC1)
: 01H (DSEGA0~DSEGC0)

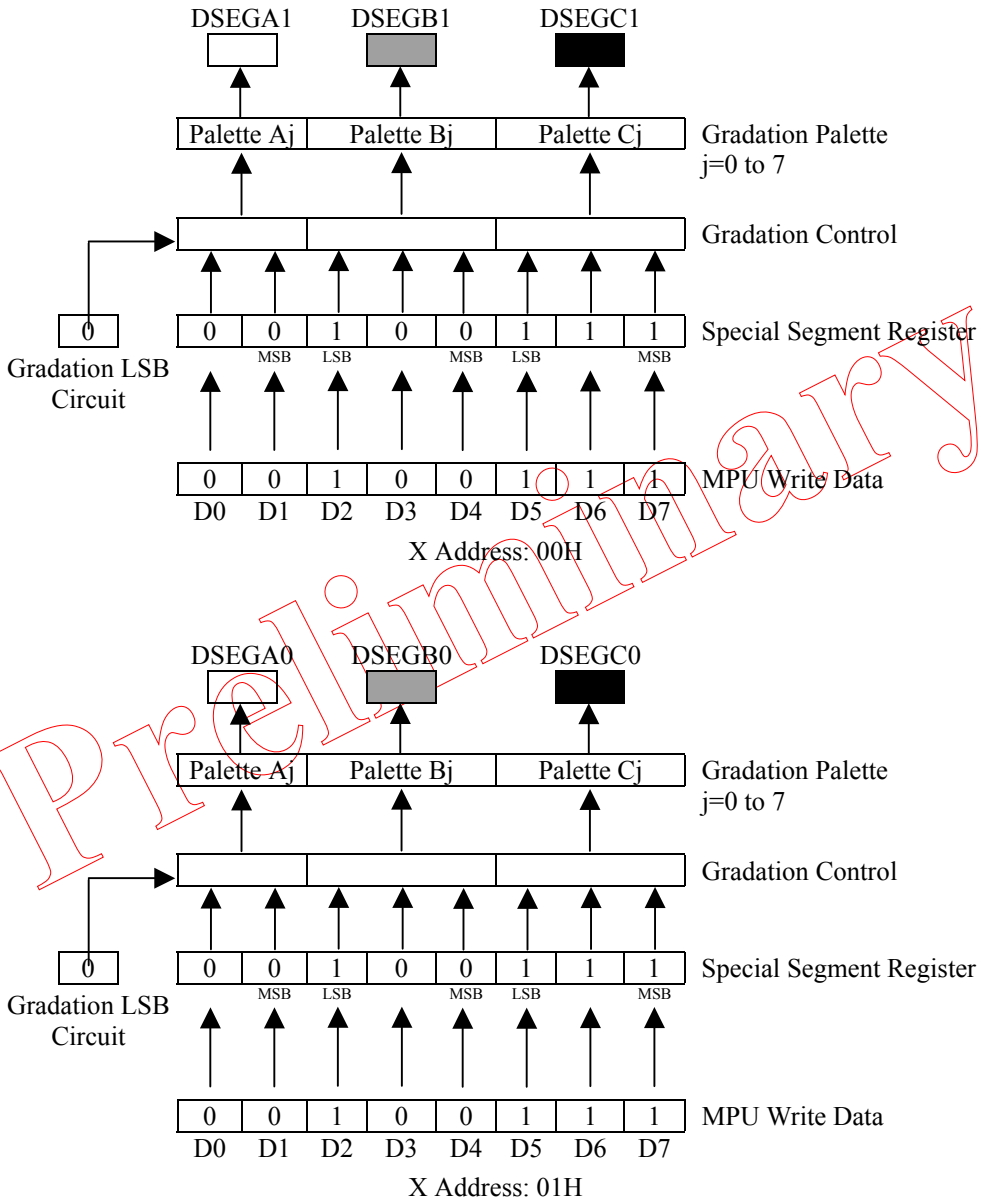
(2)Gradation mode (256 color)

8 bits bus access

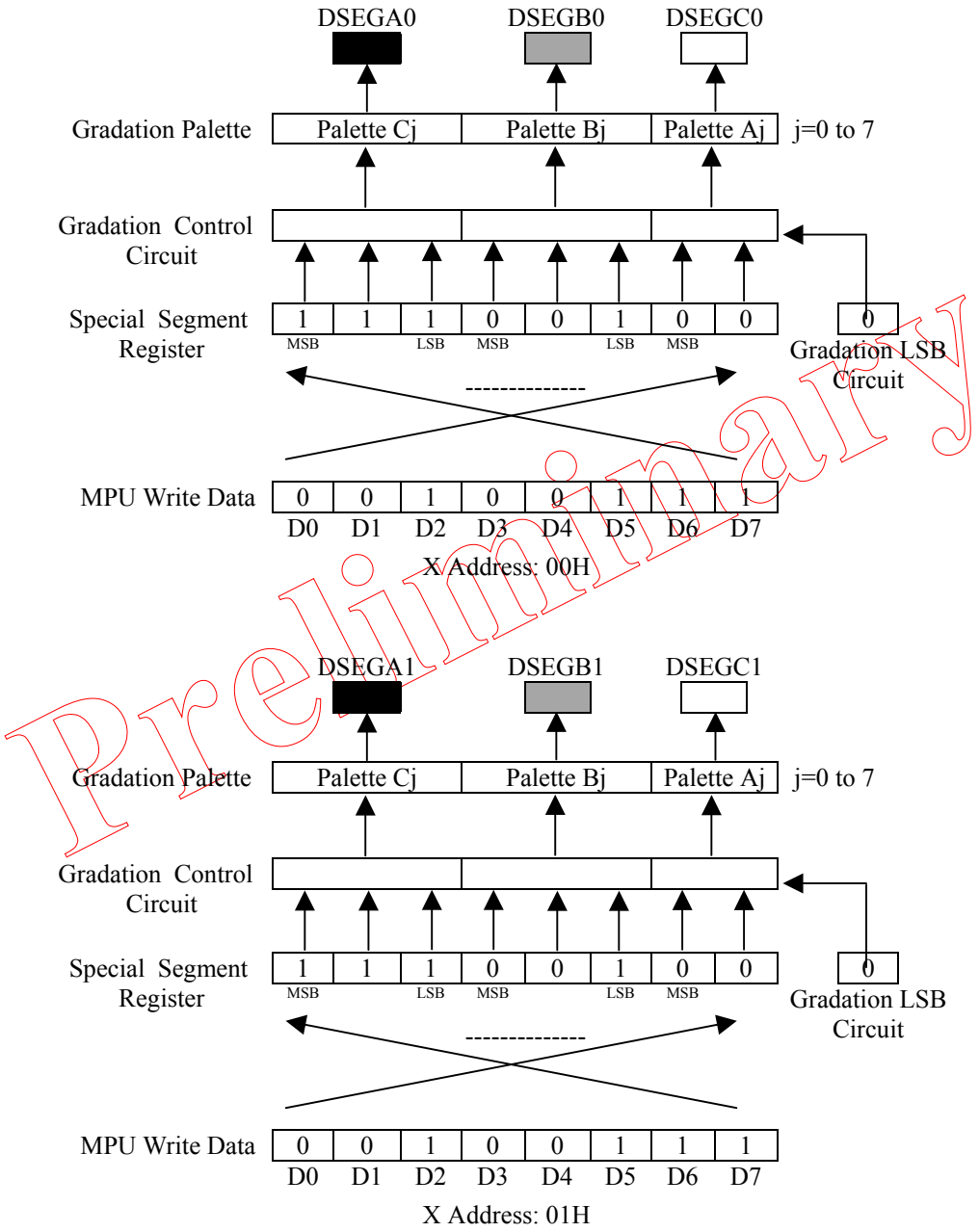
(REF, SWAP) = (0, 0)



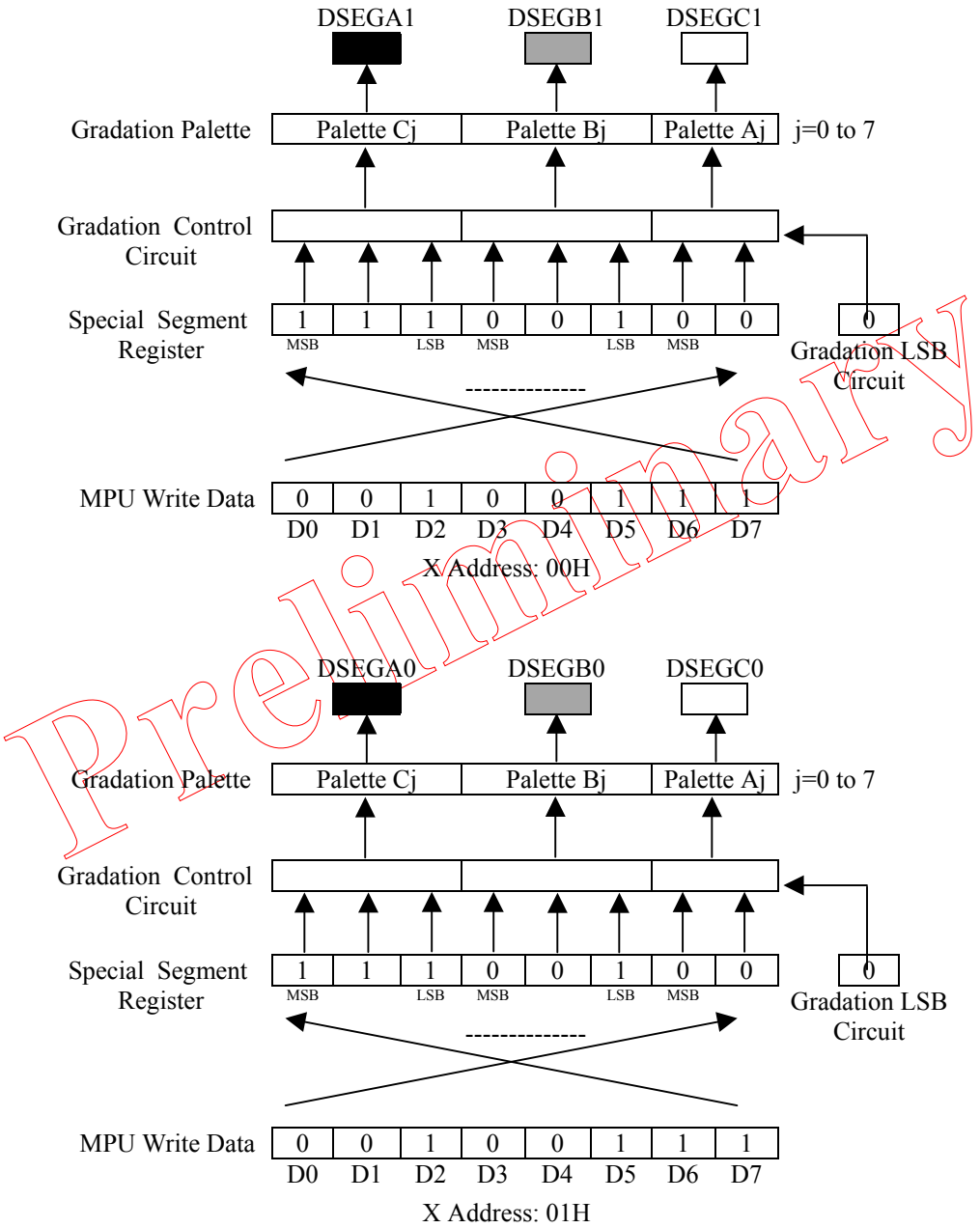
(REF, SWAP) = (1, 1)



(REF, SWAP) = (0, 1)

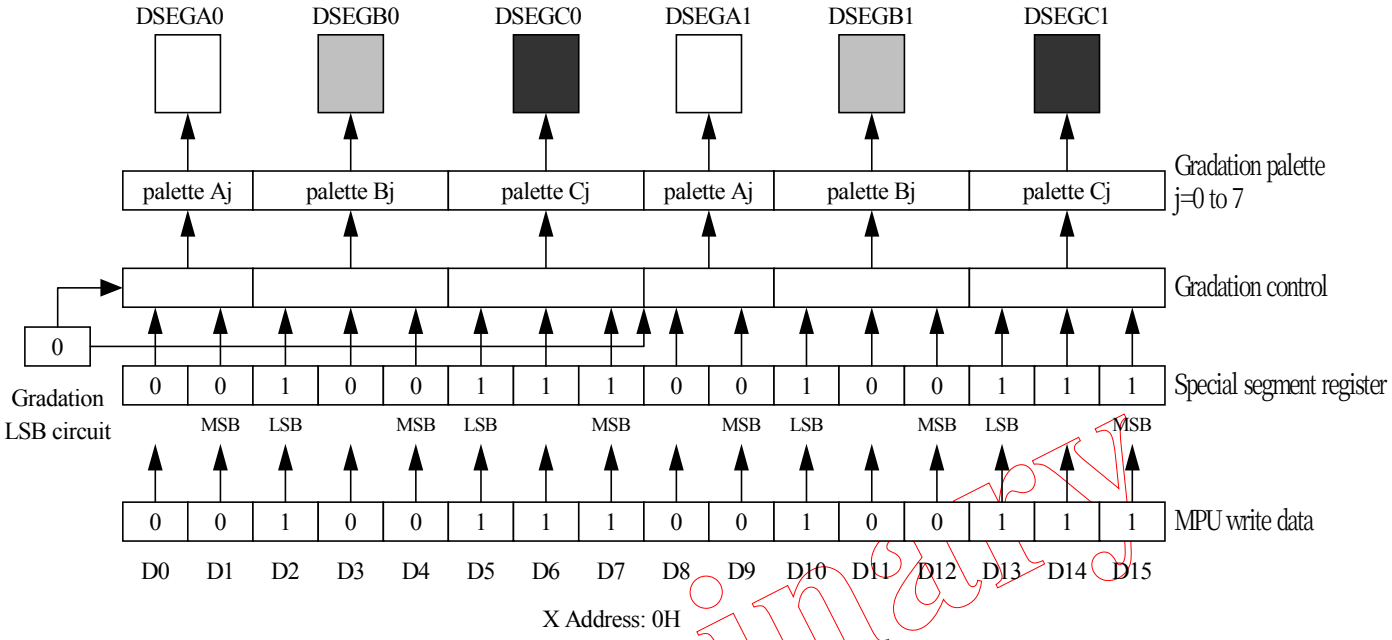


(REF, SWAP) = (1,0)

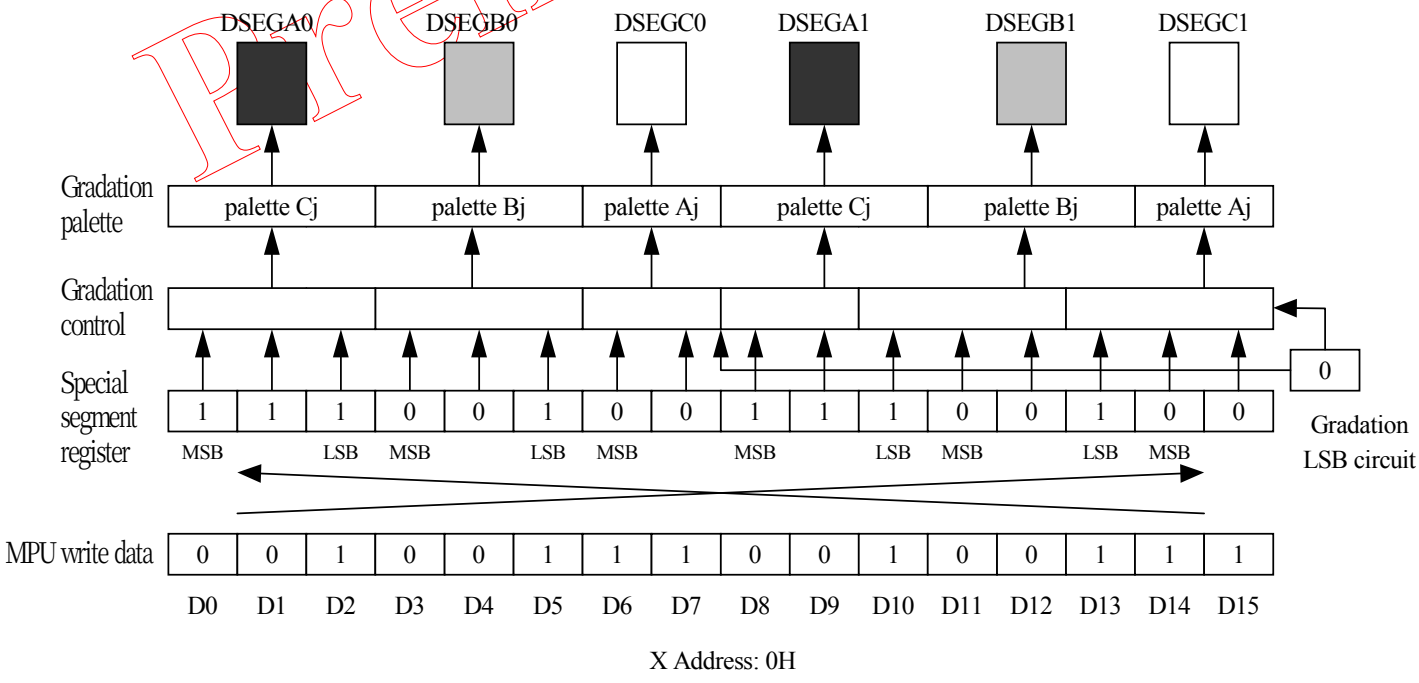


16 bits bus access

(REF, SWAP) = (0, 0) (1,1)



(REF, SWAP) = (1, 0) (0,1)

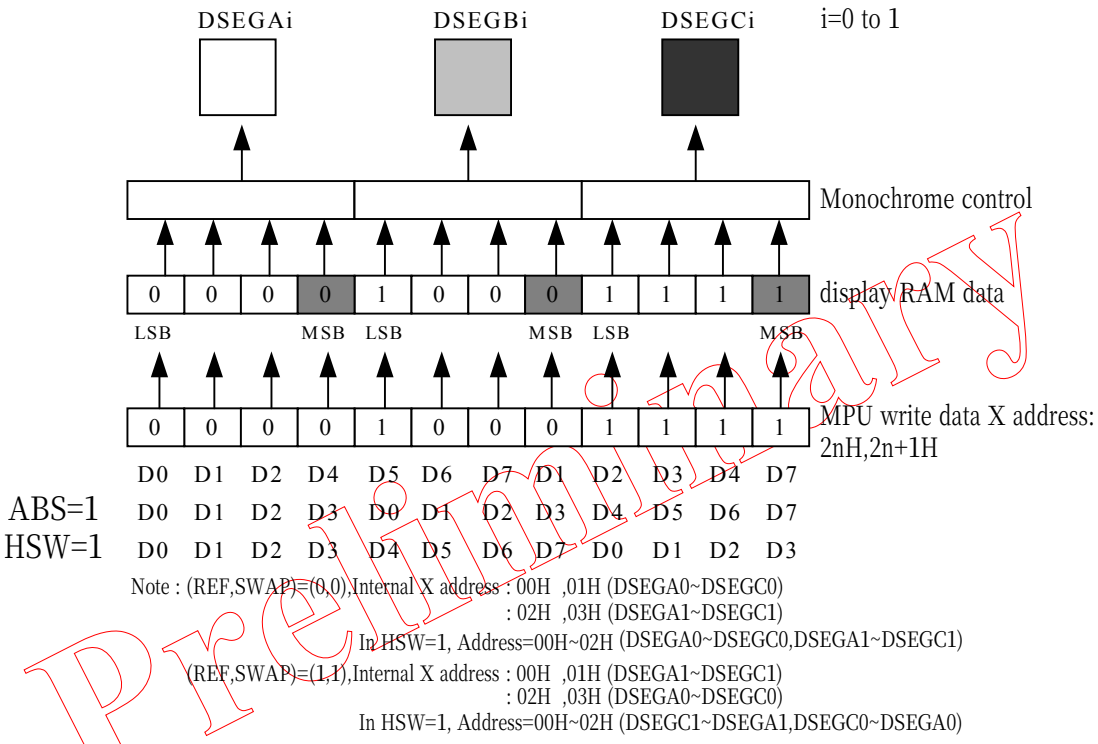


Monochrome mode

In case of monochrome mode, available X addresses for special segment register is same as gradation mode.

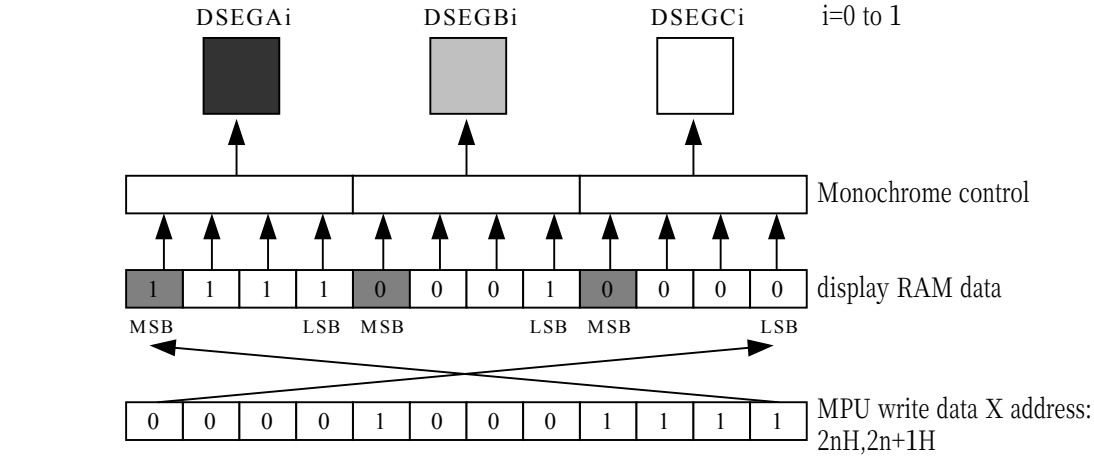
8 bits bus access

(REF, SWAP) = (0, 0) (1,1)



Note : (REF,SWAP)=(0,0),Internal X address : 00H ,01H (DSEGA0~DSEGC0)
: 02H ,03H (DSEGA1~DSEGC1)
In HSW=1, Address=00H~02H (DSEGA0~DSEGC0,DSEGA1~DSEGC1)
(REF,SWAP)=(1,1),Internal X address : 00H ,01H (DSEGA1~DSEGC1)
: 02H ,03H (DSEGA0~DSEGC0)
In HSW=1, Address=00H~02H (DSEGC1~DSEGA1,DSEGC0~DSEGA0)

(REF, SWAP) = (0, 1) (1,0)



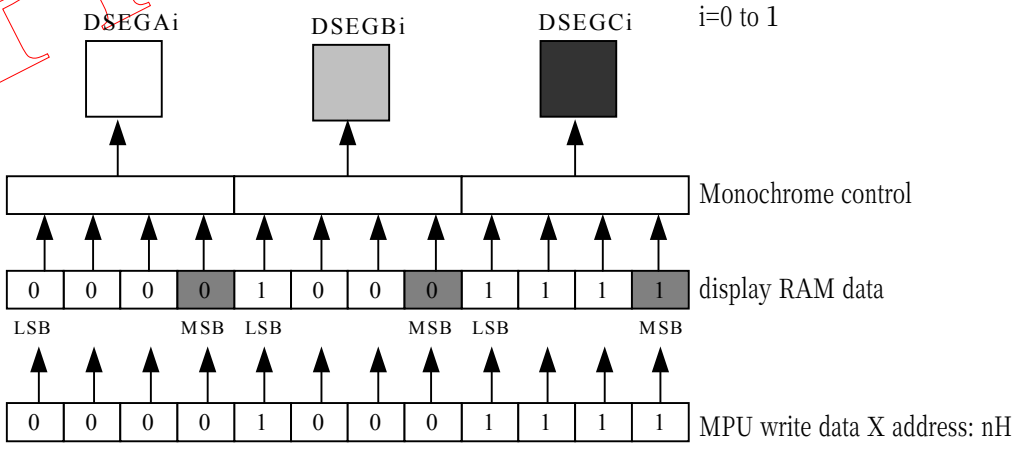
ABS=1
HSW=1

D0 D1 D2 D4 D5 D6 D7 D1 D2 D3 D4 D7
D0 D1 D2 D3 D0 D1 D2 D3 D4 D5 D6 D7
D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3

Note : (REF,SWAP)=(0,1),Internal X address : 00H ,01H (DSEGA0~DSEGC0)
: 02H ,03H (DSEGA1~DSEGC1)
In HSW=1, Address=00H~02H (DSEGA0~DSEGC0,DSEGA1~DSEGC1)
(REF,SWAP)=(1,0),Internal X address : 00H ,01H (DSEGA1~DSEGC1)
: 02H ,03H (DSEGA0~DSEGC0)
In HSW=1, Address=00H~02H (DSEGC1~DSEGA1,DSEGC0~DSEGA0)

16 bits bus access

(REF, SWAP) = (0, 0) (1,1)

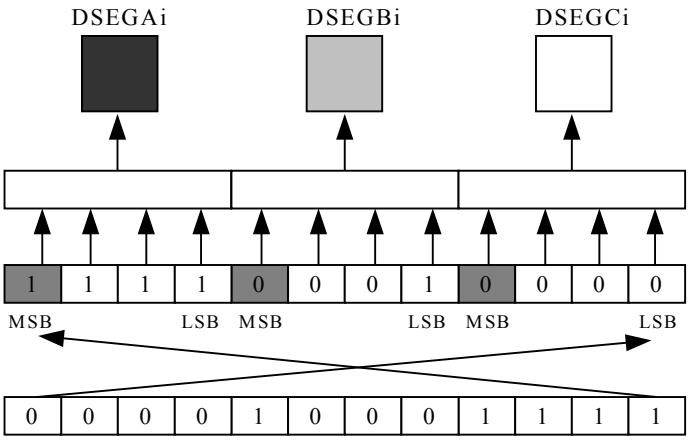


ABS=1

D1 D2 D3 D4 D7 D8 D9 D10 D12 D13 D14 D15
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11

Note : (REF,SWAP)=(0,0),Internal X address : 00H (DSEGA0~DSEGC0)
: 01H (DSEGA1~DSEGC1)
(REF,SWAP)=(1,1),Internal X address: 00H (DSEGA1~DSEGC1)
: 01H (DSEGA0~DSEGC0)

(REF, SWAP) = (0, 1) (1,0)



ABS=1

D1 D2 D3 D4 D7 D8 D9 D10 D12 D13 D14 D15
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11

Note : (REF,SWAP)=(0,1),Internal X address : 00H (DSEGA0~DSEGC0)
: 01H (DSEGA1~DSEGC1)
(REF,SWAP)=(1,0),Internal X address: 00H (DSEGA1~DSEGC1)
: 01H (DSEGA0~DSEGC0)

7.21 Oscillating Circuit

The EM65566 has the CR oscillator. The output from this oscillator is used as the timing signal source of the display and the boosting clock to the booster.

This can use only in the master operation mode.

When in the master operation mode and external clock is used, feed the clock to CK pin.

The duty cycle of the external clock must be 50%.

The resistance ratio of CR oscillator is programmable. If change this ratio, also change frame frequency for display.

7.22 Power Supply Circuit

This circuit supplies voltages necessary to drive a LCD. The circuit consists of booster and voltage converter. Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3 and V4 that are used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels. Otherwise, display quality will degrade considerably. Instead, use an external power supply. When using the external power supply, turn off the internal power supply (AMPON, DCON="00"), disconnect pins CAP1+, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP4-, VOUT, VEE, VREF and VREG. Then, feed external LCD drive voltages to pins V0, V1, V2, V3 and V4. The power circuit can be control by power circuit related register. So partial function of built-in power circuit can use with external power supply.

DCON	AMPON	Booster circuit	Voltage conversion circuit	Extemal voltage input	Note
0	0	DISABLE	DISABLE	V0,V1,V2,V3 and V4 are supplied	※1
0	1	DISABLE	ENABLE	VOUT is supplied	※2
1	1	ENABLE	ENABLE	-	-

※ 1 Because the booster and voltage converter not operating, disconnect pins
CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP4 - , VOUT, VREF, VREG and VEE.
Apply external LCD drive voltages to corresponding pin.

※ 2 Because the booster is not operating, disconnect pins
CAP1+, CAP1-, CAP2+, CPA2-, CAP3+, CAP3-, CAP4+, CAP4- and VEE.
Derive the voltage source to be supplied to the voltage converter from VOUT pin and then
Input the reference voltage at VREF pin.

7.23 Booster Circuit

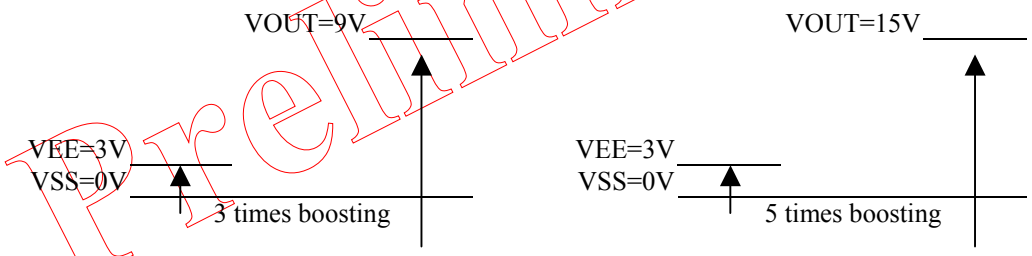
Placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3-, across CAP4+ and CAP4- and across VOUT and VSS boosts the voltage coming from VEE and VSS n-times and outputs the boosted voltage to VOUT pin. The twice, third, fourth or fifth boosted voltage output to the VOUT pin by the boost step register set. The boost step registers set by the command.

(1) In case of using only twice boosted voltage, placing C1 only across CAP1+ and CAP1- and opening CAP2+, CAP2-, CAP3+, CAP3-, CAP4+ and CAP4-.

(2) In case of using only third boosted voltage, placing C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2- and opening CAP3+, CAP3-, CAP4+ and CAP4-.

(3) In case of using only fourth boosted voltage, placing C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP3- and opening CAP4+ and CAP4-.

When use built-in booster circuit, output voltage (VOUT) must less than recommended operating voltage (15.0 Volt). If output voltage (VOUT) over recommended operating voltage, correct work of chip can not guarantee.



7.24 Electronic volume

The voltage conversion circuit has built-in an electronic volume, which allows the LCD drive voltage level V0 to be controlled with DV register setting and allows the tone of LCD to be controlled. The DV registers are 7-bits, so can select 128 voltage values for the LCD drive voltage V0.

7.25 Voltage Regulator

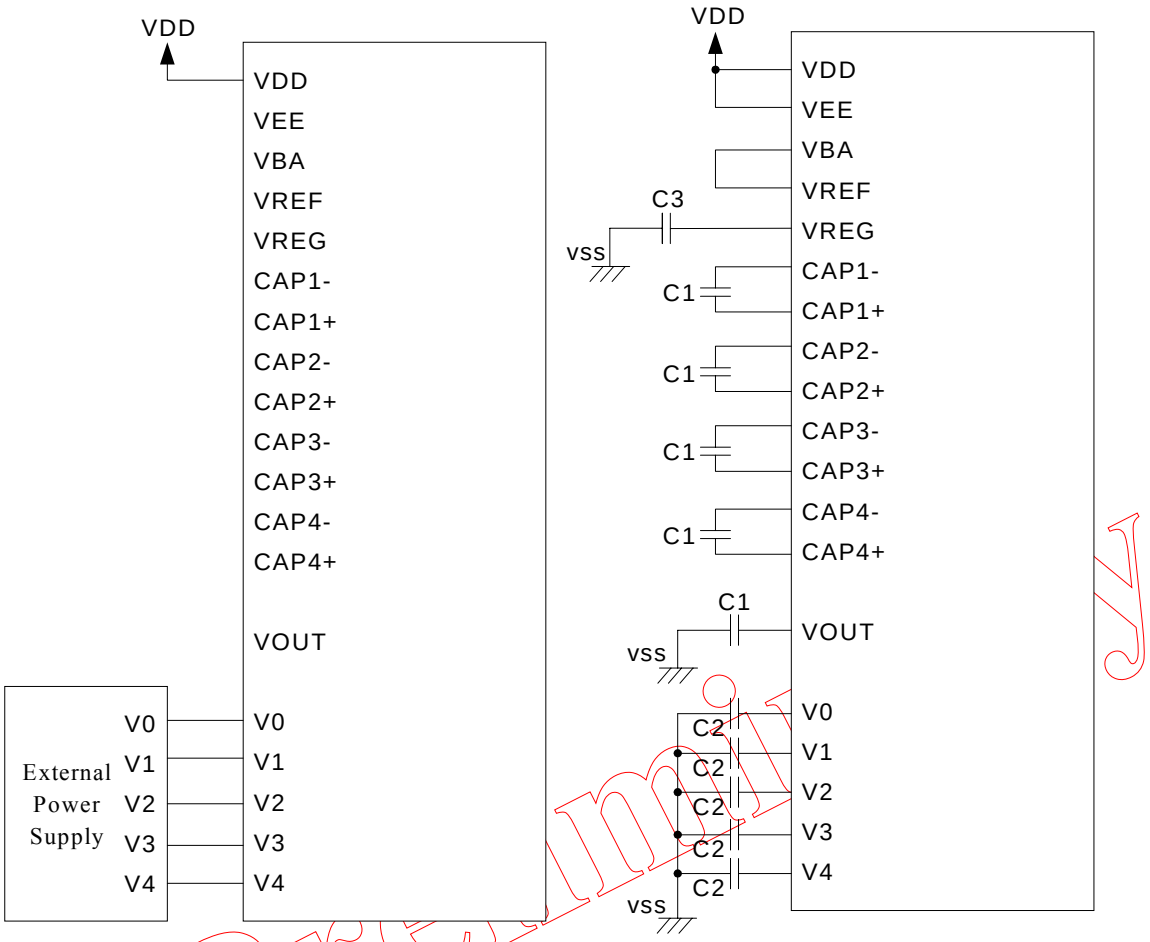
The EM65566 has built-in reference voltage regulator, which generate the voltage amplified by input voltage from VREF pin. The generated voltage is output at the VREG pin. Even if the boosted voltage level fluctuates, VREG remains stable so far as VOUT is higher than VREG Stable power supply can be obtained using this constant voltage, even if the load fluctuates. The EM65566 uses the generated VREG level for the reference level of the electronic volume to generate LCD drive voltage. In order to stabilize the output voltage at the VREG pin, connect the capacitor C3 as appropriate by choosing its value.

7.26 0.9 times VDD Voltage Generation Circuit

The EM65566 has 0.9 times VDD voltage generation circuit. This circuit output 0.9 times VDD voltage from VBA pin. When VBA output connect to VREF input, LCD drive voltage can generate without external reference voltage.

7.27 LCD Drive Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V0, that is, V1, V2, V3 and V4 are obtained by dividing V0 through a resistor network. The LCD drive voltage from EM65566 is biased at 1/5, 1/6, 1/7, 1/8 or 1/9. When using the internal power supply, connect a stabilizing capacitor C2 to each of pins V0 to V4. The capacitance of C2 should be determined while observing the LCD panel to be used. When using the external power supply, apply external LCD drive voltages to V0, V1, V2, V3, V4, disconnect pins CAP1+, CAP-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP4-, VOUT, VEE, VREF and VREG. When using only the voltage conversion circuit, turn off the internal booster circuit, disconnect pins CAP1+, CAP1-, CAP2+, CAP2-, CAP3+, CAP3-, CAP4+, CAP4- and VEE. Derive the voltage source to be supplied to the voltage converter from VOUT pin and then input the reference voltage to VREF pin.



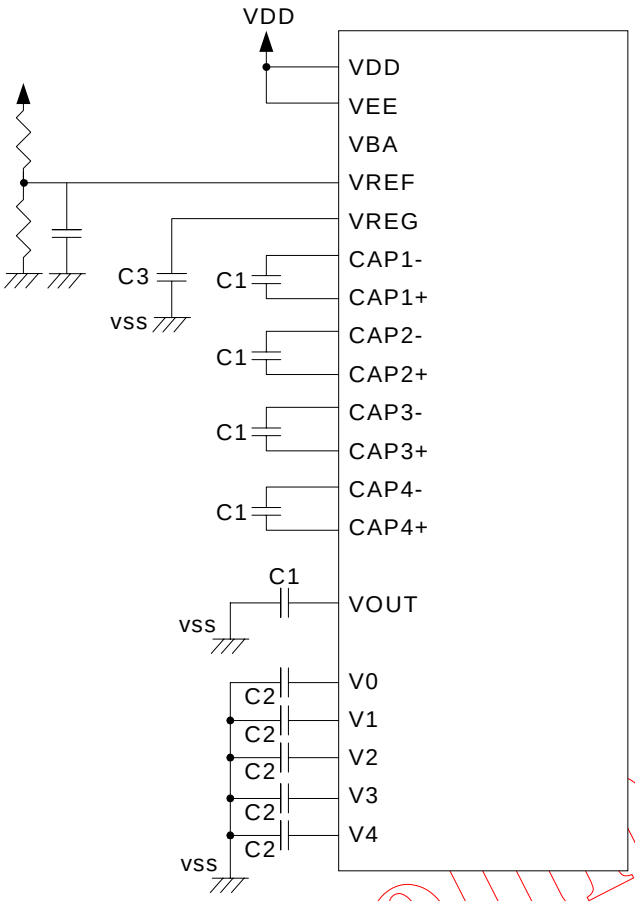
When using external power supply.

When using internal power circuit.
(5 times boosting)

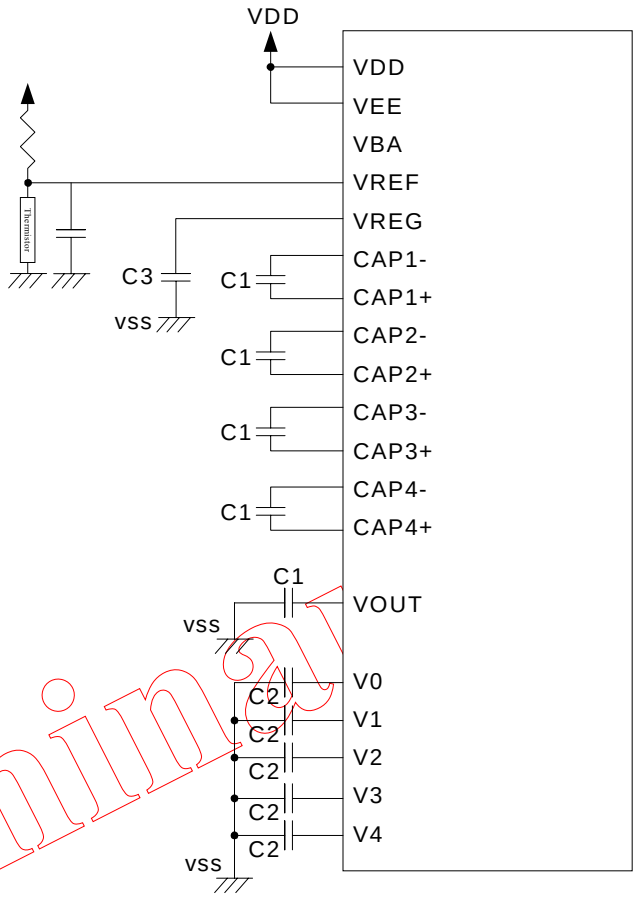
Recommended value:

C1	1.0 to 4.7 Uf
C2	1.0 to 2.2 Uf
C3	0.1 Uf

Note: External Capacitance must be use B characteristic.



When using internal power circuit with external reference voltage input.
(5 times boosting)

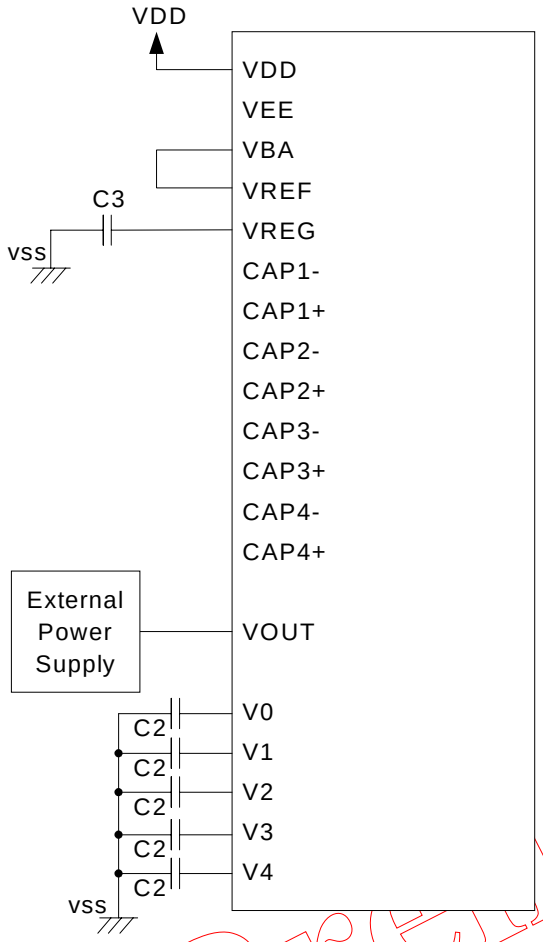


When using internal power circuit with thermistor for temperature independent.
(5 times boosting)

Recommended value.

C1	1.0 to 4.7 Uf
C2	1.0 to 2.2 Uf
C3	0.1 Uf

Note: External Capacitance must be use B characteristic.



When using internal power circuit.

(VOUT supplied from external, no use boosting circuit)

Recommended value.

C2	1.0 to 2.2 Uf
C3	0.1 Uf

Note: External Capacitance must be use B characteristic.

7.28 Partial Display Function

The EM65566 has the partial display function, which can display a part of graphic display area. This function is used be set lower bias ratio, lower boost step, and lower LCD drive voltage. Since setting partial display function, EM65566 provides low power consumption. Partial display function is the most suitable for clock indication or calendar indication when a portable equipment stand-by.

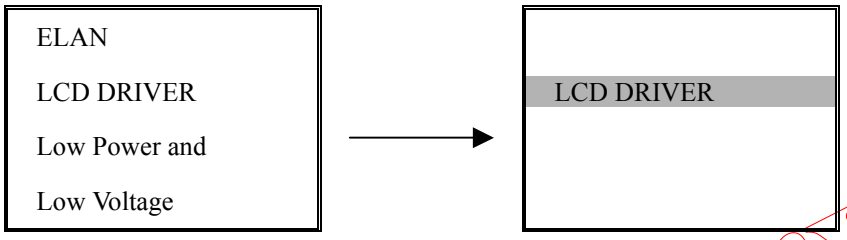
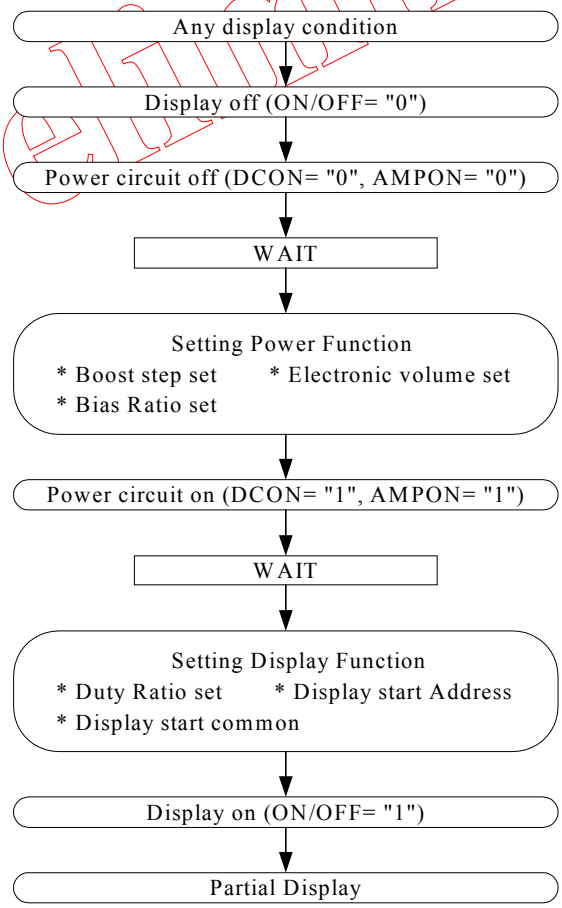


Image of partial Display

When using the partial display function, it is necessary to keep following sequence.



Select a display duty ratio for the partial display from 1/17, 1/32, 1/47, 1/62, and 1/77 using the DS(Lcd duty ratio) register. Set the most suitable values for LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and others according to the actually used LCD panel and the selected duty ratio.

7.29 Discharge circuit

The EM65566 has built-in the discharge circuit, which discharges electricity from capacitors for a stability of power sources(V0~V4).The discharge circuit is valid, while the DIS register is set to “1”. When the built-in power supply is used, should be set DIS=”1” after the power source is turned off (DCON, AMPON)=(0, 0). And don’t turn on both the built-in power source and the external power source (V0~V4, VOUT) while DIS=”1”.

7.30 Initialization

The EM65566 is initialized by setting RESB pin to “L”. Normally, RESB pin is initialized together with MPU by connecting to the reset pin of MPU. When power ON, be sure to make RESB=”L”.

4096 color mode

ITEM	Initial value
Display RAM	Not fixed
X Address	00H set
Y Address	00H set
Display starting line	Set at the first line(0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
Display duty	1/82
n-line alternated	every frame unit
(BF1,BF0)	(0,0)
Common shift direction	COM0 → COM79, COMA, COMB
Increment mode	Increment OFF
REF mode	Normal
Data SWAP Mode	OFF
Register in electronic volume	(0,0,0,0,0,0,0,0)
Power Supply	OFF
Display mode	Gradation display mode
Bias ratio	1/9 bias
Gradation palette 0	(0, 0, 0, 0, 0)
Gradation palette 1	(0, 0, 0, 1, 1)
Gradation palette 2	(0, 0, 1, 0, 1)
Gradation palette 3	(0, 0, 1, 1, 1)
Gradation palette 4	(0, 1, 0, 0, 1)
Gradation palette 5	(0, 1, 0, 1, 1)
Gradation palette 6	(0, 1, 1, 0, 1)
Gradation palette 7	(0, 1, 1, 1, 0)
Gradation palette 8	(1, 0, 0, 0, 1)
Gradation palette 9	(1, 0, 0, 1, 1)
Gradation palette 10	(1, 0, 1, 0, 1)
Gradation palette 11	(1, 0, 1, 1, 1)
Gradation palette 12	(1, 1, 0, 0, 1)
Gradation palette 13	(1, 1, 0, 1, 1)
Gradation palette 14	(1, 1, 1, 0, 1)
Gradation palette 15	(1, 1, 1, 1, 1)
Gradation display mode	Variable mode
Gradation LSB	0
RAM access data length	8-bits mode
Discharge Register	0

7.31 Precaution when Power ON and Power OFF

This LSI may be permanently damaged by high current that may flow if a voltage is supplied to the LCD driver power supply while the system power supply is floating. The detail is as follows.

(i)When using as external power supply

· Procedure for Power ON

(1) Logic system (VDD) power ON, make reset operation.

(2) Supply external LCD drive voltage to corresponding pins (V0, V1, V2, V3 and V4)

· Procedure for Power OFF

(1) Set HALT register to "1" or make reset operation.

(2) Cut off external LCD drive voltage.

(3) Logic system(VDD) power OFF.

Note: connect the serial resistor (50 to 100Ω) or fuse to the LCD drive power V0 or VOUT(when only use internal voltage conversion circuit) of the system as a current limiter. Moreover, set up the suitable value of the resistor in consideration of LCD display grade.

(ii)When using the built-in power supply

· Procedure for Power ON

(1) Logic system(VDD) power ON

(2) Booster circuit system(VEE) power ON

(3) Make reset operation, booster and voltage conversion circuit enable.

If VDD and VEE voltages aren't same potential, power on logic system (VDD) first.

· Procedure for Power OFF

(1) Set HALT register to "1" or make reset operation.

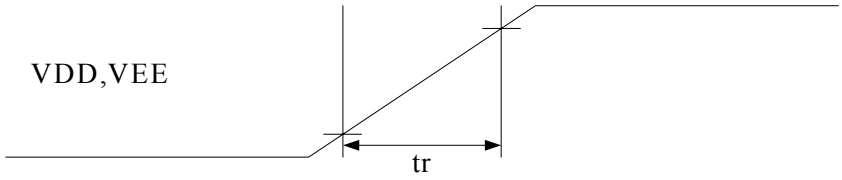
(2) Booster circuit system(VEE) power OFF.

(3) Logic system(VDD) power OFF.

If VDD and VEE are not same potential, cut off VEE first. After VEE, VOUT, V0, V1, V2, V3 and V4 voltages are below LCD ON voltage (threshold voltage for Liquid crystal turn on), power off logic system (VDD).

(iii)Power supply rising time

Though especially there is no constraint on the rising time of the power supply, the tr (rising time) of the following is recommended in the practical use.

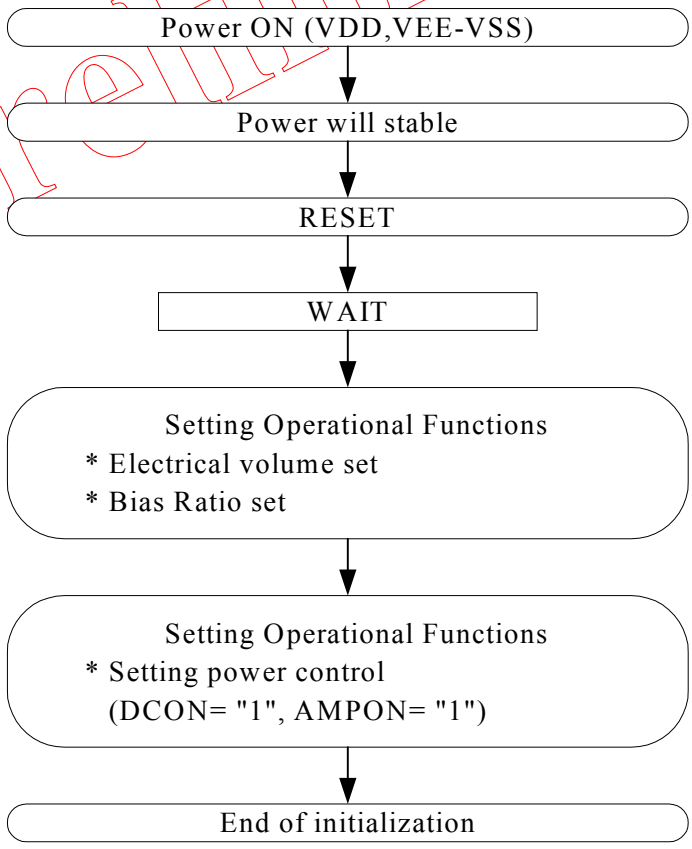


Item	Recommended rising time	Applicable Power
tr	30us ~ 10ms	VDD, VEE

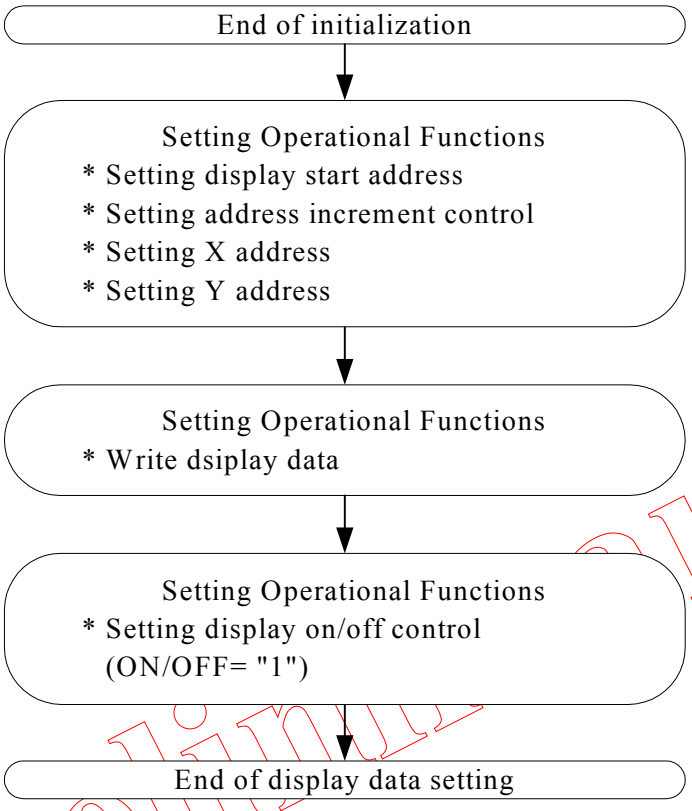
Note: The rising time is the time from 10% of VDD,VEE to 90%.

7.32 Example of Setting Registers

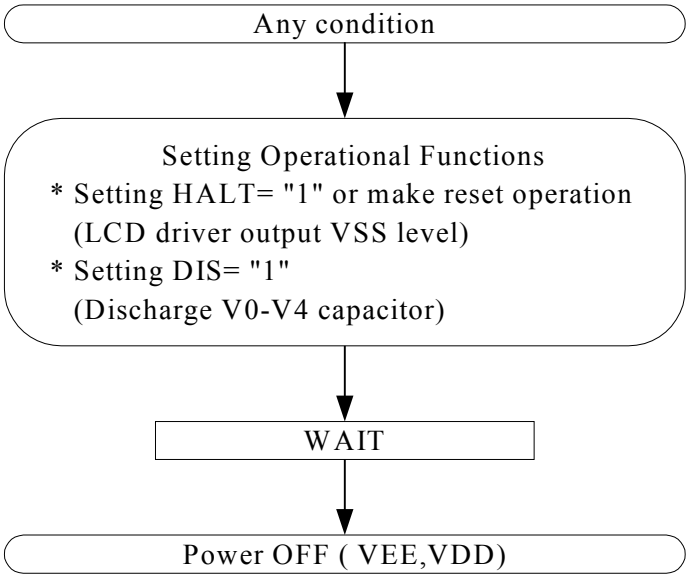
(1) Initialization



(2) Display data



(3) Power OFF



8. Control Register

8.1 control register

Control Register Table (Bank 0)

Control Register	Pins (for 80-family) & Bank							Address & Code								
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	Function
X Address (Lower nibble) [0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper nibble) [1H]	0	1	0	1	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Set of X direction Address in display RAM
Y Address (Lower nibble) [2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of Y direction Address in display RAM
Y Address (Upper nibble) [3H]	0	1	0	1	0	0	0	0	0	1	1	*	AY6	AY5	AY4	Set of Y direction Address in display RAM
Display start address (Lower nibble) [4H]	0	1	0	1	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Set address of display RAM making common starting line display
Display start address (Upper nibble) [5H]	0	1	0	1	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Set address of display RAM making common starting line display
n-line altemation (Lower nibble) [6H]	0	1	0	1	0	0	0	0	1	1	0	N3	N2	N1	N0	Set the number of altemated reverse line
n-line altemation (Upper nibble) [7H]	0	1	0	1	0	0	0	0	1	1	1	*	N6	N5	N4	Set the number of altemated reverse line
Display control (1) [8H]	0	1	0	1	0	0	0	1	0	0	0	SHIFT	MON	ALLON	ON/OFF	SHIFT: Select common shift direction MON: Select Monochrome/gradation ALLON: All display ON ON/OFF: Display ON/OFF control
Display control (2) [9H]	0	1	0	1	0	0	0	1	0	0	1	REV	NLIN	SWAP	REF	REV: Display normal/reverse NLIN: n line reverse control SWAP: Display data swapping REF: Seqment normal/reverse
Increment control [AH]	0	1	0	1	0	0	0	1	0	1	0	WIN	AIM	AYI	AXI	WIN: Select window. AIM: Select increment mode AYI: Y increment, AXI: X increment
Power control [BH]	0	1	0	1	0	0	0	1	0	1	1	AMPON	HALT	DCON	ACL	AMPON: Internal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio [CH]	0	1	0	1	0	0	0	1	1	0	0	*	DS2	DS1	DS0	Set LCD drive duty ratio
Booster [DH]	0	1	0	1	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Set number of boosting step for booster circuit
Bias ratio control [EH]	0	1	0	1	0	0	0	1	1	1	0	*	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 1)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette A0 (Lower nibble) [0H]	0	1	0	1	0	0	1	0	0	0	0	PA03 /PA83	PA02 /PA82	PA01 /PA81	PA00 /PA80	Set the umber of Gradation Palette A0
Gradation palette A0 (Upper nibble) [1H]	0	1	0	1	0	0	1	0	0	0	1	*	*	*	PA04 /PA84	Set the umber of Gradation Palette A0
Gradation palette A1 (Lower nibble) [2H]	0	1	0	1	0	0	1	0	0	1	0	PA13 /PA93	PA12 /PA92	PA11 /PA91	PA10 /PA90	Set the umber of Gradation Palette A1
Gradation palette A1 (Upper nibble) [3H]	0	1	0	1	0	0	1	0	0	1	1	*	*	*	PA14 /PA94	Set the umber of Gradation Palette A1
Gradation palette A2 (Lower nibble) [4H]	0	1	0	1	0	0	1	0	1	0	0	PA23 /PA103	PA22 /PA102	PA21 /PA101	PA20 /PA100	Set the umber of Gradation Palette A2
Gradation palette A2 (Upper nibble) [5H]	0	1	0	1	0	0	1	0	1	0	1	*	*	*	PA24 PA104	Set the umber of Gradation Palette A2
Gradation palette A3 (Lower nibble) [6H]	0	1	0	1	0	0	1	0	1	1	0	PA33 /PA113	PA32 /PA112	PA31 /PA111	PA30 /PA110	Set the umber of Gradation Palette A3
Gradation palette A3 (Upper nibble) [7H]	0	1	0	1	0	0	1	0	1	1	1	*	*	*	PA34 PA114	Set the umber of Gradation Palette A3
Gradation palette A4 (Lower nibble) [8H]	0	1	0	1	0	0	1	1	0	0	0	PA43 /PA123	PA42 /PA122	PA41 /PA121	PA40 /PA120	Set the umber of Gradation Palette A4
Gradation palette A4 (Upper nibble) [9H]	0	1	0	1	0	0	1	1	0	0	1	*	*	*	PA44 PA124	Set the umber of Gradation Palette A4
Gradation palette A5 (Lower nibble) [AH]	0	1	0	1	0	0	1	1	0	1	0	PA53 /PA133	PA52 /PA132	PA51 /PA131	PA50 /PA130	Set the umber of Gradation Palette A5
Gradation palette A5 (Upper nibble) [BH]	0	1	0	1	0	0	1	1	0	1	1	*	*	*	PA54 PA134	Set the umber of Gradation Palette A5
Gradation palette A6 (Lower nibble) [CH]	0	1	0	1	0	0	1	1	1	0	0	PA63 /PA143	PA62 /PA142	PA61 /PA141	PA60 /PA140	Set the umber of Gradation Palette A6
Gradation palette A6 (Upper nibble) [DH]	0	1	0	1	0	0	1	1	1	0	1	*	*	*	PA64 /PA144	Set the umber of Gradation Palette A6
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to " RE: set register bank number

Note: The "※" mark means "don't care".

Parentheses [ ] shows address for control register.

Caution: Different gradation levels can't be set in the same palette.

Control Register Table (Bank 2)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette A7 (Lower nibble) [0H]	0	1	0	1	0	1	0	0	0	0	0	PA73 /PA153	PA72 /PA152	PA71 /PA151	PA70 /PA150	Set the umber of Gradation Palette A7
Gradation palette A7 (Upper nibble) [1H]	0	1	0	1	0	1	0	0	0	0	1	*	*	*	PA74 /PA154	Set the umber of Gradation Palette A7
Gradation palette B0 (Lower nibble) [2H]	0	1	0	1	0	1	0	0	0	1	0	PB03 /PB83	PB02 /PB82	PB01 /PB81	PB00 /PB80	Set the umber of Gradation Palette B0
Gradation palette B0 (Upper nibble) [3H]	0	1	0	1	0	1	0	0	0	1	1	*	*	*	PB04 /PB84	Set the umber of Gradation Palette B0
Gradation palette B1 (Lower nibble) [4H]	0	1	0	1	0	1	0	0	1	0	0	PB13 PB93	PB12 PB92	PB11 PB91	PB10 PB90	Set the umber of Gradation Palette B1
Gradation palette B1 (Upper nibble) [5H]	0	1	0	1	0	1	0	0	1	0	1	*	*	*	PB14 PB94	Set the umber of Gradation Palette B1
Gradation palette B2 (Lower nibble) [6H]	0	1	0	1	0	1	0	0	1	1	0	PB23 PB103	PB22 PB102	PB21 PB101	PB20 PB100	Set the umber of Gradation Palette B2
Gradation palette B2 (Upper nibble) [7H]	0	1	0	1	0	1	0	0	1	1	1	*	*	*	PB24 PB104	Set the umber of Gradation Palette B2
Gradation palette B3 (Lower nibble) [8H]	0	1	0	1	0	1	0	1	0	0	0	PB33 PB113	PB32 PB112	PB31 PB111	PB30 PB110	Set the umber of Gradation Palette B3
Gradation palette B3 (Upper nibble) [9H]	0	1	0	1	0	1	0	1	0	0	1	*	*	*	PB34 PB114	Set the umber of Gradation Palette B3
Gradation palette B4 (Lower nibble) [AH]	0	1	0	1	0	1	0	1	0	1	0	PB43 PB123	PB42 PB122	PB41 PB121	PB40 PB120	Set the umber of Gradation Palette B4
Gradation palette B4 (Upper nibble) [BH]	0	1	0	1	0	1	0	1	0	1	1	*	*	*	PB44 PB124	Set the umber of Gradation Palette B4
Gradation palette B5 (Lower nibble) [CH]	0	1	0	1	0	1	0	1	1	0	0	PB53 PB133	PB52 PB132	PB51 PB131	PB50 PB130	Set the umber of Gradation Palette B5
Gradation palette B5 (Upper nibble) [DH]	0	1	0	1	0	1	0	1	1	0	1	*	*	*	PB54 PB134	Set the umber of Gradation Palette B5
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0 RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 3)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette B6 (Lower nibble) [0H]	0	1	0	1	0	1	1	0	0	0	0	PB63 /PB143	PB62 /PB142	PB61 /PB141	PB60 /PB140	Set the umber of Gradation Palette B6
Gradation palette B6 (Upper nibble) [1H]	0	1	0	1	0	1	1	0	0	0	1	*	*	*	PB64 /PB144	Set the umber of Gradation Palette B6
Gradation palette B7 (Lower nibble) [2H]	0	1	0	1	0	1	1	0	0	1	0	PB73 /PB153	PB72 /PB152	PB71 /PB151	PB70 /PB150	Set the umber of Gradation Palette B7
Gradation palette B7 (Upper nibble) [3H]	0	1	0	1	0	1	1	0	0	1	1	*	*	*	PB74 /PB154	Set the umber of Gradation Palette B7
Gradation palette C0 (Lower nibble) [4H]	0	1	0	1	0	1	1	0	1	0	0	PC03 /PC83	PC02 /PC82	PC01 /PC81	PC00 /PC80	Set the umber of Gradation Palette C0
Gradation palette C0 (Upper nibble) [5H]	0	1	0	1	0	1	1	0	1	0	1	*	*	*	PC04 /PC84	Set the umber of Gradation Palette C0
Gradation palette C1 (Lower nibble) [6H]	0	1	0	1	0	1	1	0	1	1	0	PC13 /PC93	PC12 /PC92	PC11 /PC91	PC10 /PC90	Set the umber of Gradation Palette C1
Gradation palette C1 (Upper nibble) [7H]	0	1	0	1	0	1	1	0	1	1	1	*	*	*	PB14 /PC94	Set the umber of Gradation Palette C1
Gradation palette C2 (Lower nibble) [8H]	0	1	0	1	0	1	1	1	0	0	0	PC23 /PC103	PC22 /PC102	PC21 /PC101	PC20 /PC100	Set the umber of Gradation Palette C2
Gradation palette C2 (Upper nibble) [9H]	0	1	0	1	0	1	1	1	0	0	1	*	*	*	PB24 /PC104	Set the umber of Gradation Palette C2
Gradation palette C3 (Lower nibble) [AH]	0	1	0	1	0	1	1	1	0	1	0	PC33 /PC113	PC32 /PC112	PC31 /PC111	PC30 /PC110	Set the umber of Gradation Palette C3
Gradation palette C3 (Upper nibble) [BH]	0	1	0	1	0	1	1	1	0	1	1	*	*	*	PB34 /PC114	Set the umber of Gradation Palette C3
Gradation palette C4 (Lower nibble) [CH]	0	1	0	1	0	1	1	1	1	0	0	PC43 /PC123	PC42 /PC122	PC41 /PC121	PC40 /PC120	Set the umber of Gradation Palette C4
Gradation palette C4 (Upper nibble) [DH]	0	1	0	1	0	1	1	1	1	0	1	*	*	*	PB44 /PC124	Set the umber of Gradation Palette C4
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0 RE: set register bank number

Note: The "※" mark means "don't care".

Parentheses [ ] shows address for control register.

Control Register Table (Bank 4)

Control Register	Pins (for 80-family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Gradation palette C5 (Lower nibble) [0H]	0	1	0	1	1	0	0	0	0	0	0	PC53 /PC133	PC52 /PC132	C51 /PC131	PC50 /PC130	Set the umber of Gradation Palette C5
Gradation palette C5 (Upper nibble) [1H]	0	1	0	1	1	0	0	0	0	0	1	*	*	*	PC54 /PC134	Set the umber of Gradation Palette C5
Gradation palette C6 (Lower nibble) [2H]	0	1	0	1	1	0	0	0	0	1	0	PC63 /PC143	PC62 /PC142	PC61 /PC141	PC60 /PC140	Set the umber of Gradation Palette C6
Gradation palette C6 (Upper nibble) [3H]	0	1	0	1	1	0	0	0	0	1	1	*	*	*	PC64 /PC144	Set the umber of Gradation Palette C6
Gradation palette C7 (Lower nibble) [4H]	0	1	0	1	1	0	0	0	1	0	0	PC73 /PC153	PC72 /PC152	PC71 /PC151	PC70 /PC150	Set the umber of Gradation Palette C7
Gradation palette C7 (Upper nibble) [5H]	0	1	0	1	1	0	0	0	1	0	1	*	*	*	PC74 /PC154	Set the umber of Gradation Palette C7
Display start common [6H]	0	1	0	1	1	0	0	0	1	1	0	*	SC2	SC1	SC0	Set Common Driver Start Line
EXCS control [7H]	0	1	0	1	1	0	0	0	1	1	1	*	*	*	EX CS	EXCS Pin control for Senal interface
Display Select Control [8H]	0	1	0	1	1	0	0	1	0	0	0	PWM	GL SB		PS	Select Plane(access/display) Set GLSB Bit. Select PWM Mod
RAM Data length Set [9H]	0	1	0	1	1	0	0	1	0	0	1	C256	HSW	ABS	WLS	Set Data length on RAM Access 8-bit access or 16-bit access
Electronic Volume (Lower nibble) [AH]	0	1	0	1	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Set Electronic Vollume Register (lower code)
Electronic Volume (Upper nibble) [BH]	0	1	0	1	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Set Electronic Vollume Register (upper code)
Register read Control [CH]	0	1	0	1	1	0	0	1	1	0	0	RA3	RA2	RA1	RA0	Set Register Address for read
Select Rf [DH]	0	1	0	1	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Select Rf ratio of OSC circuit
Extended Power Control [EH]	0	1	0	1	1	0	0	1	1	1	0	BF1	BF0	HPM	DIS	Discharge capacitance of V0,V1,V2,V3,V4 Pins
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TS T0	RE2	RE1	RE0	TST0: for LS1 test,must set to "(RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

Control Register Table (Bank 5)

Control Register		Pins (for 80-family) & Bank							Address & Code								Function
		CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Window X End Address (Lower nibble)	[0H]	0	1	0	1	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Set X end address for window function access
Window X End Address (Upper nibble)	[1H]	0	1	0	1	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Set X end address for window function access
Window Y End Address (Lower nibble)	[2H]	0	1	0	1	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Set Y end address for window function access
Window Y End Address (Upper nibble)	[3H]	0	1	0	1	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Set Y end address for window function access
Start Address for line reverse (Lower nibble)	[4H]	0	1	0	1	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Set start line for line reverse display
Start Address for line reverse (Upper nibble)	[5H]	0	1	0	1	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Set start line for line reverse display
End Address for line reverse (Lower nibble)	[6H]	0	1	0	1	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Set end line for line reverse display
End Address for line reverse (Upper nibble)	[7H]	0	1	0	1	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Set end line for line reverse display
Line reverse control	[8H]	0	1	0	1	1	0	1	1	0	0	0	*	*	BT	LREV	LREV: Line reverse control BT: Reverse type select
Select Address for special Segment	[9H]	0	1	0	1	1	0	1	1	0	0	1	*	*	*	DMY	Select address for special segment driver
Register Access Control	[FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test,must set to "0" RE: set register bank number

Note: The "※" mark means "don't care"

Parentheses [ ] shows address for control register.

8.2 Functions of Control Registers

The EM65566 has many control registers as shown in "7 Control Register". In case of control register access, upper nibble of data bus(D7~D4) represent register address, lower nibble of data bus(D3~D0) represent data. The access example is shown in the following. The Pins (CSB, RS, RDB, WRB) setting are for 80-family MPU interface. Only the setting of terminal (RDB,WRB) is different, when it is accessed by the 68-fanily MPU.

(Example) X Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

Register address | Data

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

Pins setting | Register Bank

In the writing to the control register, it is used directly as addressing D7~D4 of the data bus. In case of register read, first set RA register for specific register address, next can read specific register. Therefore, it is need 2-step for register read. Then, specific register output to D3~D0 of data bus. Except D3~D0 of data bus are all "H". Prohibit access to undefined register address area. When RS is "L", all read/write operations are accessed to display RAM. Then data bus doesn't include register address. In case of write, D3~D0 data is written to the register designated at D7~D4 in rising edge of the WRB signal. In case of read, register can output to data bus is RDB active period. Control register and display RAM are the equal access timing.

8.2.1 X Address Register (AX)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX3, AX2, AX1, AX0}= 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AX7	AX6	AX5	AX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX7, AX6, AX5, AX4}= 0H, read address: 1H)

The AX register set to X-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 4-bit respectively.

8.2.2 Y Address Register

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	1	0	AY3	AX2	AY1	AY0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {AY3, AY2, AY1, AY0}=0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	※	AY6	AY5	AY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AY6, AY5, AY4}=0H, read address: 3H)

※ **Mark shows "Don't care"**

The AY register set to Y-direction address of display RAM. In data setting, lower place and upper place are divided with 4-bit and 3-bit respectively. 00H to 51H are applicable to the values for AY6 to AY0, and 52H to FFH are not permitted. The address for (AY6 to AY0) = 50H, 51H are in the display RAM area for icon display.

8.2.3 Display Start Address Register (LA)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	LA3	LA2	LA1	LA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {LA3, LA2, LA1, LA0}=0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	LA6	LA5	LA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {LA6, LA5, LA4}=0H, read address: 5H)

※ **Mark shows "Don't care"**

The LA register indicated first output segment data in display RAM. This segment data output to common line indicated by SC register. After that output common line shift to the increment direction.

LA6	LA5	LA4	LA3	LA2	LA1	LA0	Line Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
1	0	0	1	1	1	1	79

8.2.4 n Line Alternated Register (N)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	N3	N2	N1	N0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {N3, N2, N1, N0}=0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	N6	N5	N4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {N6, N5, N4}=0H, read address: 7H)

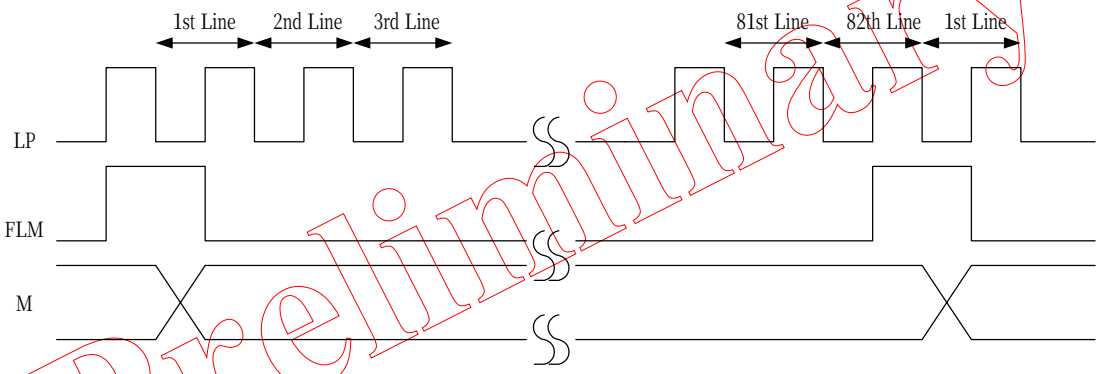
※ **Mark shows "Don't care"**

The reverse line number of LCD alternated drive is required to set in the register. The line number has a limit, must keeps between from 2 to 80 lines. The values set up by the alternated register become enable when NLIN control bit is "1". When NLIN control bit is "0", alternated drive waveform reverses by each frame is generated.

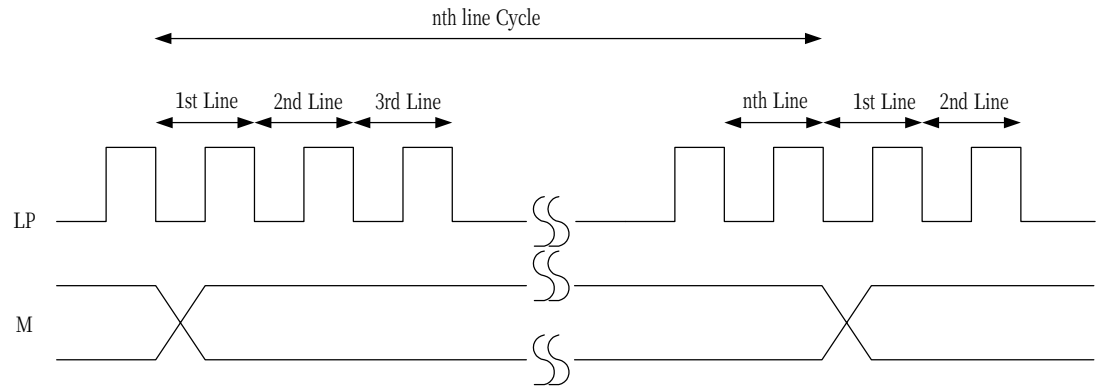
N6	*N5*	*N4*	*N3*	*N2*	*N1*	*N0*	*Line Address*
0	0	0	0	0	0	0	-
0	0	0	0	0	0	1	2
			⋮				
1	0	0	1	1	1	1	80

Alternated Timing

(i) NLIN="0" (in case of 1/82 DUTY Display)



(ii) NLIN="1"



8.2.5 Display Control (1) Register

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	0	SHIFT	MON	ALL ON	ON/ OFF

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {SHIFT, MON, ALLON, ON/OFF}=0H, read address: 8H)

Various control of display is set up.

ON/OFF

To control ON/OFF of display

ON/OFF = "0": Display OFF

ON/OFF = "1": Display ON

ALLON

Regardless of the data for display, all is on.

This control has priority over display normal/reverse commands.

ALLON = "0": Normal display

ALLON = "1": All display lighted

MON

Select Monochrome or Gradation display

MON = "0": Gradation display mode

MON = "1": Monochrome display mode

SHIFT

The shift direction of display scanning data in the common driver output is selected.

SHIFT = "0": COM0→COM79 shift-scan

SHIFT = "1": COM79→COM0 shift-scan

8.2.6 Display Control (2) Register

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	1	REV	NLIN	SWAP	REF

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {REV,NLIN,SWAP,REF}=0H, read address: 9H)

Various control of display is set up.

REF

When MPU accesses to display RAM, the X address and data can reverse. The REF function shows in the table below:

REF	*Access from MPU*		*Internal Access*		*Corresponding Segment Output*
	X Address	*D7-D0*	*X Address*	*D7-D0*	
0	NH	D0(LSB) : D7(MSB)	NH	(LSB) : (MSB)	SEG(8*NH)Output : SEG(8*NH+7)Output
1	NH	D0(LSB) : D7(MSB)	MaxH-NH	(MSB) : (LSB)	SEG(8*(maxH-NH)+7)Output : SEG(8*(maxH-NH))Output

Note: maxH: The maximum X-address in each access mode.

The order of segment driver output can be reversed by register by register setting, lessening the limitation in placing IC when assembling a LCD module.

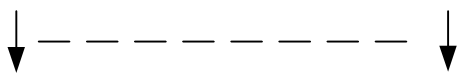
SWAP

When data to display RAM are written, the write data exchange bit order.

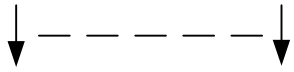
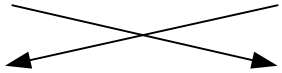
SWAP = "0": Normal mode.

SWAP = "1": in data writing, exchange bit order.

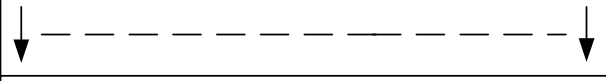
Example of exchange bit order

Write Data	SWAP=0	SWAP=1
	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
		
Internal Data	d0 d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11	d11 d10 d9 d8 d7 d6 d5 d4 d3 d2 d1 d0

8 bit access (HSW=1)

Write Data	SWAP=0	SWAP=1
	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7
		
Internal Data	d0 d1 d2 d3 d4 d5 d6 d7	d7 d6 d5 d4 d3 d2 d1 d0

16 bit access (HSW=1)

Write Data	SWAP=0	SWAP=1
	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
		
Internal Data	d0 d1 d2 d3 d4 d5 d6 d7 d8 d9 d10 d11 d12 d13 d14 d15	d15 d14 d13 d12 d11 d10 d9 d8 d7 d6 d5 d4 d3 d2 d1 d0

CAUTION: REF and SWAP both set to "1"

When data write to display RAM, the write data is normal bit order.

When data read from display RAM, the read data is exchanged bit order.

NLIN

The NLIN control n-line alternated drive.

NLIN = "0": n-line alternated drive OFF. In each frame, the alternated signals (M) are reversed.

NLIN ="1": n-line alternated drive ON. According to data set up in n-line alternated register, the alternation is made.

REV

Corresponding to the data of display RAM, the lighting or not-lighting of the display is set up.

REV ="0": When RAM data at "H", LCD at ON voltage (normal)

REV ="1": When RAM data at "L", LCD at ON voltage (reverse)

8.2.7 Increment Control Register Set

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	0	WIN	AIM	AYI	AXI

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the tine of reset: {WIN,AIM,AYI,AXI}=0H, read address: AH)

This register control the increment mode and window function when accessing to display RAM. The increment operation of AX and AY register can control by AIM,AYI and AXI registers setting and every write access or every read access to display RAM. The AY register directly connect to display RAM as Y address. The AX register connect to address converter, and that output to display RAM as X address in the auto increment mode, AX and AY register are increment, not directly increment X and Y address.

In setting to this control register, the increment operation of address can be made without setting successive addresses for writing data or for reading data to display RAM from MPU.

The WIN register use for window function control.

WIN="0": Normal RAM access

WIN="1": Window function access

In case of using window function access, should be set following register before access to RAM.

WIN="1", AXI="1", AYI="1"

X Address, Y Address, Window X End Address, Window Y End Address

Moreover, should be keep following address condition.

Window end X address ≧ Window start X address

Window end Y address ≧ Window start Y address

Detail of window function see "6-7 Display RAM access using Window Function".

The increment control of X and Y addresses by AIM, AYI and AXI registers are as follows.

AIM	*Address Increment Timing*
0	When writing to Display RAM or reading from Display RAM This is effective when access to successive address area
1	Only when writing to Display RAM This is effective the case of "Read Modify Write

AYI	*AXI*	*Select Address Increment Operation*	*Remark*
0	0	Address is not increment	(1)
0	1	X-Address is increment	(2)
1	0	Y-Address is increment	(3)
1	1	X and Y both are increment	(4)

(1) Regardless of AIM, no increment for AX and AY register.

(2) According to the setting-up of AIM, automatically change X address.

In accordance with the REF register, AX register and X address becomes as follows.

REF	Transition of AX Register	Transition of X Address
0		Same as AX register
1	00H→ 01H→.....→ max	max→maxH →.... →00H

Note: maxH: The internal maximum X-address in each access mode.

(3) According to the setting-up of AIM, automatically change Y address. Regardless of REF, increment by loop of

Transition of AY Register	Transition of Y Address
00H→01H →.....→ 51H	Same as AY register

(4) According to the setting-up of AIM, cooperative change X and Y address. When the X address exceed maxH, Y address increment occurs.

REF	Transition of AX and AY Register	Transition of X and Y Address
0	AX: 00H → 00H → – – → max AY: When each AX exceed maxH, increment AY 00H → 00H → – – → 51H	Same as AX and AY register
1		AX: max → maxH → – – → 00H AY: Same as AY register

Note: maxH: The internal maximum X-address in each access mode.

Following shows address increment in window function access.

REF	Transition of AX and AY Register	Transition of X and Y Address
0	AX:	Same as AX and AY register
1	AX: START Address → START Address+1 → – – → END Address AY: When each AX exceed AE, increment AY START Address → START Address+1 → – – → END Address	AX: maxH-(START Address) → maxH-(START Address+1) → – – → maxH-(END Address) AY: Same as AY register

Note: maxH: The internal maximum X-address in each access mode.

In each operation mode, the following increment operation is performed:

(i) When gradation display mode and 8-bit access are selected

Address are incremented as described above.

(ii) When gradation display mode and 16-bit access are selected:

Two bytes are accessed by accessing the RAM once.

The X-addresses increment in the order of 00H,01H,…3EH,and 3FH.

8.2.8 Power Control Register

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	1	AMPON	HALT	DCON	ACL

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the tine of reset: {AMPON, HALT,DCON,ACL}=0H, read address: BH)

ACL

The internal circuit can be initialized. This register is effective only at Master operation mode.

ACL = “0”: Normal operation

ACL = “1”: Initialization ON

When the reset operation begins internally after ACL register sets to “1”, the ACL register is automatically cleared to “0”. The internal reset signal has been generated with a clock (built-in oscillation circuit or CK input) for the display. Therefore, install the WAIT period for the display clock two cycles at least. After WAIT period, next operation can handle. Since built-in oscillation circuit and external CK input can not be used in the slave mode, the setting of the ACL register becomes the invalidity. Certainly use the RESB terminal, when the reset is applied on the slave chip.

DCON

The internal booster circuit is set ON/OFF

DCON = “0”: Booster circuit OFF

DCON=”1”: Booster circuit ON

HALT

The conditions of power saving are set ON/OFF by this command.

HALT = “0”: Normal operation

HALT=”1”: Power-saving operation

When setting in the power-saving state, the consumed current can be reduced to a value near to the standby current.

The internal condition at power saving are as follows.

(a) The oscillating circuit and power supply circuit are stopped.

(b) The LCD drive is stopped, and output of the segment driver and common driver are VSS level.

(c) The clock input from CK pin is inhibited.

(d) The contents of Display RAM data are maintained.

(e) The operational mode maintains the state of command execution before executing power saving command.

AMPON Command

The internal OP-AMP circuit block (voltage regulator, electronic volume, and voltage conversion circuit) is set ON/OFF by this command.

AMPON = "0": The internal OP-AMP circuit OFF

AMPON = "1": The internal OP-AMP circuit ON

8.2.9 LCD Duty (DS)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	0	※	DS2	DS1	DS0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {DS2, DS1, DS0}=0H, read address: CH)

※ **Mark shows "Don't care"**

The DS register set to LCD display duty.

DS2	*DS1*	*DS0*	*Display width and Duty*
0	0	0	80-dot width display in Y-direction, 1/82 duty
0	0	1	75-dot width display in Y-direction, 1/77 duty
0	1	0	60-dot width display in Y-direction, 1/62 duty
0	1	1	45-dot width display in Y-direction, 1/47 duty
1	0	0	30-dot width display in Y-direction, 1/32 duty
1	0	1	15-dot width display in Y-direction, 1/17 duty
1	1	0	Prohibit code
1	1	1	Prohibit code

Partial display can be made possible by setting an arbitrary duty ratio.

8.2.10 Booster Setup (VU)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	0	※	VU2	VU1	VU0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {VU2,VU1,VU0}=0H, read address: DH)

※ **Mark shows "Don't care"**

The booster steps set to VU register

.

VU2	*VU1*	*VU0*	*Booster Operation*
0	0	0	Booster disable (No operation)
0	0	1	2 times voltage output
0	1	0	3 times voltage output
0	1	1	4 times voltage output
1	0	0	5 times voltage output
1	0	1	Prohibit code
1	1	0	Prohibit code
1	1	1	Prohibit code

8.2.11 Bias Setting Register (B)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	1	0	※	B2	B1	B0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	0

(At the time of reset: {B2,B1,B0}=0H, read address: EH)

※ **Mark shows "Don't care"**

This register is used to set a bias ratio. A bias ratio can be selected from 1/9, 1/8, 1/7, 1/6, and 1/5 by setting B2, B1, and B0.

B2	*B1*	*B0*	*Bias*
0	0	0	1/9 Bias
0	0	1	1/8 Bias
0	1	0	1/7 Bias
0	1	1	1/6 Bias
1	0	0	1/5 Bias
1	0	1	Prohibit code
1	1	0	Prohibit code
1	1	1	Prohibit code

8.2.12 Register Access Control

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	1	0	TST0	RE2	RE1	RE0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0/1	0/1	0/1

(At the time of reset: {TST0,RE2,RE1,RE0}=0H, read address: FH)

※ **Mark shows "Don't care"**

The RE register set to number of register bank. Access to each control register, set RE register at first.

The TST0 register use for test of LSI, Therefore this register must be set to "0"

8-13 Gradation Palette Register (PA0~PA7, PB0~PB7, PC0~PC7)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	0	PA03 /PA83	PA02 /PA82	PA01 /PA81	PA00 /PA80

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: 0H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	※	※	※	PA04 /PA84

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: 1H)

(At the time of reset: PA04~PA00 = "00000")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PA13 /PA93	PA12 /PA92	PA11 /PA91	PA10 /PA90

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	※	※	※	PA14 /PA94

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 3H)

(At the time of reset: PA14~PA10 = "00101")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PA23 /PA103	PA22 /PA102	PA21 /PA101	PA20 /PA100

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PA24 /PA104

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 5H)

(At the time of reset: PA24~PA20 = "01010")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PA33 /PA113	PA32 /PA112	PA31 /PA111	PA30 /PA110

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	※	PA34 /PA114

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 7H)

(At the time of reset: PA34~PA30 = "01110")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PA43 /PA123	PA42 /PA122	PA41 /PA121	PA40 /PA120

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 8H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	1	※	※	※	PA44 /PA124

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: 9H)

(At the time of reset: PA44~PA40 = "10001")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	0	PA53 /PA133	PA52 /PA132	PA51 /PA131	PA50 /PA130

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: AH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	1	※	※	※	PA54 /PA134

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: BH)

(At the time of reset: PA54~PA50 = "10101")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	0	PA63 /PA143	PA62 /PA142	PA61 /PA141	PA60 /PA140

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: CH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	1	※	※	※	PA64 /PA144

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	0	1

(Read address: DH)

(At the time of reset: PA64~PA60 = "11010")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	0	PA73 /PA153	PA72 /PA152	PA71 /PA151	PA70 /PA150

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: 0H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	※	※	※	PA74 /PA154

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: 1H)

(At the time of reset: PA74~PA70 = "11111")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB03 /PB83	PB02 /PB82	PB01 /PB81	PB00 /PB80

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	※	※	※	PB04 /PB84

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 3H)

(At the time of reset: PB04~PB00 = "00000")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PB13 /PB93	PB12 /PB92	PB11 /PB91	PB10 /PB90

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PB14 /PB94

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 5H)

(At the time of reset: PB14~PB10 = "00101")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PB23 /PB103	PB22 /PB102	PB21 /PB101	PB20 /PB100

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	※	PB24 /PB104

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 7H)

(At the time of reset: PB24~PB20 = "01010")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PB33 /PB113	PB32 /PB112	PB31 /PB111	PB30 /PB110

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	0

(Read address: 8H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	1	※	※	※	PB34 /PB114

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: 9H)

(At the time of reset: PB34~PB30 = "01110")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	0	PB43 /PB123	PB42 /PB122	PB41 /PB121	PB40 /PB120

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: AH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	1	※	※	※	PB44 /PB124

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: BH)

(At the time of reset: PB44~PB40 = "10001")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	0	PB53 /PB133	PB52 /PB132	PB51 /PB131	PB50 /PB130

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: CH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	1	※	※	※	PB54 /PB134

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	0

(Read address: DH)

(At the time of reset: PB54~PB50 = "00101")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	0	PB63 /PB143	PB62 /PB142	PB61 /PB141	PB60 /PB140

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: 0H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	※	※	※	PB64 /PB144

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: 1H)

(At the time of reset: PB64~PB60 = "11010")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	PB73 /PB153	PB72 /PB152	PB71 /PB151	PB70 /PB150

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PB74 /PB154

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 3H)

(At the time of reset: PB74~PB70 = "11111")

※ Mark shows "Don't care"

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	PC03 /PC83	PC02 /PC82	PC01 /PC81	PC00 /PC80

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	※	※	※	PC04 /PC84

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 5H)

(At the time of reset: PC04~PC00 = "00000")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	PC13 /PC93	PC12 /PC92	PC11 /PC91	PC10 /PC90

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	※	※	※	PC14 /PC94

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 7H)

(At the time of reset: PC14~PC10 = "00101")

※ **Mark shows "Don't care"**

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	PC23 /PC103	PC22 /PC102	PC21 /PC101	PC20 /PC100

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	1	1

(Read address: 8H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	1	※	※	※	PC24 /PC104

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: 9H)

(At the time of reset: PC24~PC20 = "01010")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	0	PC33 /PC113	PC32 /PC112	PC31 /PC111	PC30 /PC110

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: AH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	1	※	※	※	PC34 /PC114

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: BH)

(At the time of reset: PC34~PC30 = "01110")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	0	PC43 /PC123	PC42 /PC122	PC41 /PC121	PC40 /PC120

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: CH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	1	※	※	※	PC44 /PC124

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	0	1	1

(Read address: DH)

(At the time of reset: PC44~PC40 = "10001")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	0	PC53 /PC133	PC52 /PC132	PC51 /PC131	PC50 /PC130

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: 0H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	※	※	※	PC54 /PC134

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: 1H)

(At the time of reset: PC54~PC50 = "10101")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	1	0	PC63 /PC143	PC62 /PC142	PC61 /PC141	PC60 /PC140

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: 2H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	1	1	※	※	※	PC64 /PC144

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: 3H)

(At the time of reset: PC64~PC60 = "11010")

※ **Mark shows "Don't care"**

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	1	0	0	PC73 /PC153	PC72 /PC152	PC71 /PC151	PC70 /PC150

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: 4H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	1	0	1	※	※	※	PC74 /PC154

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: 5H)

(At the time of reset: PC74~PC70 = "11111")

※ **Mark shows "Don't care"**

These gradation palette register set up gradation level. The EM65566 has 32 gradation levels. Gradation level table

4096 color mode

Caution: Different gradation levels can't be set in the same palette.

[Three groups of palettes Aj,Bj, and Cj (j=0-15) are available]

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0	0	gradation palette0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	gradation palette8 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	gradation palette1 initial value	1 0 0 1 1	19/31	gradation palette9 initial value
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	gradation palette2 initial value	1 0 1 0 1	21/31	gradation palette10 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7//31	gradation palette3 initial value	1 0 1 1 1	23/31	gradation palette11 initial value
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	gradation palette4 initial value	1 1 0 0 1	25/31	gradation palette12 initial value
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	gradation palette5 initial value	1 1 0 1 1	27/31	gradation palette13 initial value
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	gradation palette6 initial value	1 1 1 0 1	29/31	gradation palette14 initial value
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 0	15/31	gradation palette7 initial value	1 1 1 1 1	31/31	gradation palette15 initial value

256 color mode

[Three groups of palettes Aj,Bj, and Cj (j=0-7) are available]

Palette	Gradation level	Remarks	Palette	Gradation level	Remarks
0 0 0 0 0	0	256 color palette0 initial value	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	256 color palette4 initial value
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	256 color palette1 initial value	1 0 1 0 1	21/31	256 color palette5 initial value
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7//31		1 0 1 1 1	23/31	
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31	256 color palette2 initial value	1 1 0 1 0	26/31	256 color palette6 initial value
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31	256 color palette3 initial value	1 1 1 1 0	30/31	
0 1 1 1 0	15/31		1 1 1 1 1	31/31	256 color palette7 initial value

8.2.14 Display Start Common

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	1	1	0	※	SC2	SC1	SC0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset:{ SC2,SC1,SC0}=0H, read address: 6H)

※ **Mark shows "Don't care"**

The SC register set up the scanning start output of the common driver.

SC2	*SC1*	*SC0*	*Display starting common when SHIFT=0*	*Display starting common when SHIFT=1*
0	0	0	COM0~	COM79~
0	0	1	COM15~	COM64~
0	1	0	COM30~	COM49~
0	1	1	COM45~	COM34~
1	0	0	COM60~	COM19~
1	0	1	COM75~	COM4~
1	1	0	Prohibit code	
1	1	1	Prohibit code	

SHIFT="0": COM0 to COM79 shift-scan

SHIFT="1": COM79 down to COM0 shift-scan

8.2.15 EXCS Output Control

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	1	1	1	※	※	※	EXCS

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset: {EXCS} = 1H, read address: 6H)

※ **Mark shows "Don't care"**

The EXCS register control output value of EXCS pin.

The EXCS pin is output terminal. Therefore, the EXCS register can work in only master mode.

EXCS="0": EXCS pin output "L"

EXCS="1": EXCS pin output "H"

8.2.16 Display Select Control

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	0	PWM	GLSB		PS

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset: {PWM,GLSB,PS} = 0H, read address: 8H)

PS

In 4096 color mode, select 16 gradation level from 32 gradation palette. In 256 color mode, just setting lower 8 gradation.

PS= "0":Lower 8 gradation setting

PS= "1":Upper 8 gradation setting

GLSB

In 256 color mode, for the segment driver of 4-gradation display, select 4 gradations from 8 gradations using the 2 bits written to the corresponding RAM area and the 1 bit supplemented by the gradation LSB circuit. Supplement the 1 bit of data by setting the gradation LSB register (GLSB).

Gradation LSB = "0": Selects 0 as the LSB information on the RAM for 4-gradation segment driver.

Gradation LSB = "1": Selects 1 as the LSB information on the RAM for 4-gradation segment driver.

PWM

The PWM register select the gradation display mode.

PWM = "0": Variable display mode using 16 gradations selected from 32 gradations in 4096 color mode

Variable display mode using 8 gradations selected from 32 gradations in 256 color mode (C256=1)

PWM = "1": 16-gradation fixed display mode

8.2.17 Data Bus Size Select

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	1	C256	HSW	ABS	WLS

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset: {C256,HSW,ABS,WLS} = 0H, read address: 9H)

※ **Mark shows "Don't care"**

The WLS register select data bus size for access from MPU

WLS = "0": The data bus size is 8-bits width

WLS = "1": The data bus size is 16-bits width

When MPU access to control register using 16-bits bus size , high byte data is ignored.

ABS

ABS= "0": normal mode

ABS= "1": change corresponding bit from input data bus

HSW

HSW="0": High speed writing mode off

HSW="1": High speed writing mode on accessing the 8-bit data RAM

C256

C256= "0": 4096 color mode

C256= "1": 256 color mode

8.2.18 Electronic Volume Register

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	0	DV3	DV2	DV1	DV0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: AH)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	1	1	※	DV6	DV5	DV4

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(Read address: BH)

(At the time of reset: {DV6~DV0} = 00H)

※ **Mark shows "Don't care"**

The DV register can control V0 voltage.

The DV register has 7-bits, so can select 128 level voltage.

DV6	*DV5*	*DV4*	*DV3*	*DV2*	*DV1*	*DV0*	*Output voltage*
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	:
			:				:
1	1	1	1	1	1	0	:
1	1	1	1	1	1	1	Larger

The output voltage at VREG is specified by equation (1).

VREG = VREF * N ----------(1)

(N: Number of boosting steps)

The LCD drive voltage V0 is determined by VREG level and electronic volume code equation (2).

V0 = 0.5 * VREG + M * (VREG – 0.5VREG) / 127 ----------(2)

(M: DV6 to DV0 register values)

In order to prevent transient voltage from generating when an electronic volume code is set, the circuit design is such that the set value is not reflected as a level immediately after only the upper bits(DV6-DV4) of the electronic code have been set. The set value becomes valid when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

8.2.19 Resistance Ratio of CR Oscillator

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	1	※	RF2	RF1	RF0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset: {RF2, RF1, RF0} = 0H, read address: DH)

※ **Mark shows "Don't care"**

The RF registers can control resistance ratio of CR oscillator. Therefore frame frequency can change RF registers setting. When change RF registers value, should be need to check LCD display quality.

RF2	*RF1*	*RF0*	*Operation*
0	0	0	Initial Resistance Ratio
0	0	1	0.8 times of initial Resistance Ratio
0	1	0	0.9 times of initial Resistance Ratio
0	1	1	1.1 times of initial Resistance Ratio
1	0	0	1.2 times of initial Resistance Ratio
1	0	1	Prohibit Code
1	1	0	Prohibit Code
1	1	1	Prohibit Code

8.2.20 Extended power control

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	1	0	BF1	BF0	HPM	DIS

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset: {HPM, DIS} = 0H, {BF1,BF0}=0H;read address: EH)

The DIS register can control capacitors discharged that connected between the power supply V0-V4 for LCD drive voltage and VSS.

When using this register, refer to 6-30 (Discharge circuit).

DIS = “0”: Discharge OFF

DIS = “1”: Discharge start

The HPM register is the power control for the power supply circuit for liquid crystal drive.

HPM= “H”: High power mode

HPM= “L”: Normal mode

BF1~BF0: The operating frequency in the booster is selected. When the boosting frequency is high, the driving ability of booster become high, but the current consumption is increased. Adjust the boosting frequency considering the external capacitors and the current consumption.

BF1	*BF0*	*Operating clock frequency in the booster*
0	0	1.5K Hz * 8
0	1	1.5K Hz * 4
1	0	1.5K Hz * 2
1	1	1.5 K Hz

8.2.21 Internal Register Read Address

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	1	0	1	RA3	RA2	RA1	RA0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	0

(At the time of reset: {RA3,RA2,RA1,RA0} =0H;read address: CH)

The RA register set to specify the address for register read operation. The EM65566 has many registers and has register bank. Therefore, it is need 4-steps to read to read the specific register in maximum case.

(1) Write 04H to RE register for access to RA register.

(2) Writes specific register address to RA register.

(3) Write specific register bank to RE register.

(4) Read specific contents.

8.2.22 Internal Register Data Read

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
※	※	※	※	Internal Register read data			

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	0	1	0/1	0/1	0/1

※ **Mark shows "Don't care"**

This command is used to read data from an internal register. Before executing the command, you need to set the address and RE flag for reading data from the internal register.

8.2.23 Windows End X Address

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	0	EX3	EX2	EX1	EX0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {EX3,EX2,EX1,EX0} = 0H, read address: 0H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	EX7	EX6	EX5	EX4

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {EX7,EX6,EX5,EX4} = 0H, read address: 1H)

※ **Mark shows "Don't care"**

The EX registers set to X direction end address for window function.

8.2.24 Windows End Y Address

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	1	0	EY3	EY2	EY1	EY0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {EY3,EY2,EY1,EY0} = 0H, read address: 2H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	1	1	※	EY6	EY5	EY4

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {EY6,EY5,EY4} = 0H, read address: 3H)

※ **Mark shows "Don't care"**

The EY registers set to Y direction end address for window function.

8.2.25 Line Reverse Start Address

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	1	0	0	LS3	LS2	LS1	LS0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {LS3,LS2,LS1,LS0} = 0H, read address: 4H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	※	LS6	LS5	LS4

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {LS6,LS5,LS4} = 0H, read address: 5H)

※ **Mark shows "Don't care"**

The LS registers set to line reverse start address. Moreover, must keep following two conditions.

(1) 00H ≦ LS ≦ 4FH

(2) LS ≦ LE LE: Line reverse end address

8.2.26 Line Reverse End Address

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	1	1	0	LE3	LE2	LE1	LE0

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {LE3,LE2,LE1,LE0} = 0H, read address: 6H)

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
0	0	0	1	※	LE6	LE5	LE4

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {LE6,LE5,LE4} = 0H, read address: 7H)

※ **Mark shows "Don't care"**

The LE registers set to line reverse end address. Moreover, must keep following two conditions.

(3) 00H ≦ LS ≦ 4FH

(4) LS ≦ LE LS: Line reverse start address

8.2.27 Line Reverse Control

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	0	※	※	BT	LREV

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {BT,LREV} = 0H, read address: 8H)

※ **Mark shows "Don't care"**

The LREV registers control line reverse display function.

LREV = "0": Normal display (Not reverse).

LREV = "1": Line reverse display enable.

The area specified by Line Reverse Start/End Register reverse display.

The reverse type is selectable by BT register.

When use Line Reverse Display function, LS and LE registers must keep following relation.

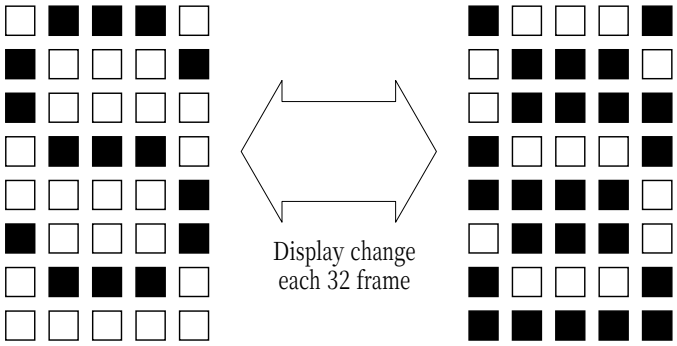
LS ≦ LE

The BT register control line reverse type. This is an option of line reverse display function.

This BTs setting is only available in case of LREV="1"

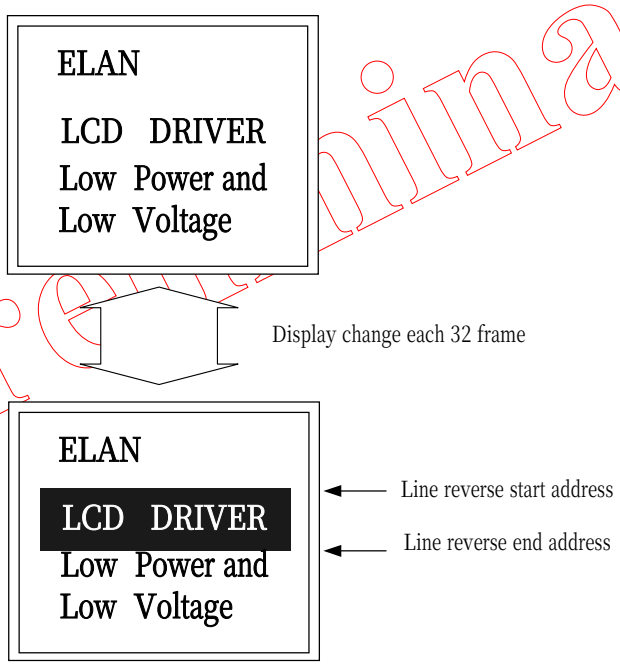
BT = "0": Reverse display

BT = "1": Reverse display at each 32 frame.



Blink example(LREV="1", BT="1")

The special segment outputs aren't influenced by LREV and BT setting. The display area by selected COMA and COMB common outputs aren't also influenced.



Blink example (LREV="1", BT="1")

8.2.28 Special Segment Driver Select:

D7	*D6*	*D5*	*D4*	*D3*	*D2*	*D1*	*D0*
1	0	0	1	※	※	※	DMY

CSB	*RS*	*RDB*	*WRB*	*RE2*	*RE1*	*RE0*
0	1	1	0	1	0	1

(At the time of reset: {DMY} = 0H, read address: 9H)

※ **Mark shows "Don't care"**

When access the special segment register, DMY register set up.

DMY = "0": Display RAM can access.

DMY = "1" Special Segment Register can access.

9. *Relationship between Setting and Common/Display RAM*

The relationship between the COM pin numbers and the addresses in the Y-direction on the display RAM changes according to the SHIFT command. LCD Duty Set command. Display Starting Common Position Set command, and Display Starting Line Set command.

When “0” is selected for the display starting line:
The relationship between the COM pin and the addresses in the vertical direction of the display RAM (hereafter called MY) changes on an 15 dots basis according to the LCD Duty Set command and the Display Starting Common Position Set command. When the SHIFT bit is “0”, the common position change in the forward direction. When “1” they change reverse direction. When “0” is selected as the values for LA6 to LA0 in the Display Starting Line Set command, the MY number corresponding to the display starting position is “0”. The MY numbers are sequentially shifted backward when display occurs. In any case, the relations of COMA = MY80 nad COMB = MY81 do not change.

When non-zero is selected for the display starting line:
The relationship between the COM pins and the addresses in the vertical direction on the display RAM, MY changes on an 15 dots basis according to the information in the LCD Duty Set command and Display Starting Common Position Set command. The common positions change in the forward when the SHIFT bit is “0”, and change in the reverse direction when the SHIFT bit is “1”. If non-zero is selected for the values for LA6 to LA0 by the Display Starting Line set command. the MY number corresponding to the display starting position shifts by the set value. The MY number shifts backward when display occurs. If it exceeds 79, it returns to 0, and the shifts sequentially. In any case, the relations of COMA = MY80 and COMB = MY81 do not change.

10. Absolute maximum ratings

10.1 Absolute maximum ratings

Item	*Symbol*	*Condition*	*Pin use*	*Rating*	*Unit*
Supply voltage (1)	VDD	Ta=25℃	VDD	-0.3 ~ + 4.0	V
Supply voltage (2)	VEE		VEE	-0.3 ~ + 4.0	V
Supply voltage (3)	VOUT		VOUT	--0.3 ~ + 16.0	V
Supply voltage (4)	VREG		VREG	-0.3 ~ + 16.0	V
Supply voltage (5)	V0		V0	-0.3 ~ + 16.0	V
Supply voltage (6)	V1,V2,V3,V4		V1,V2,V3,V4	-0.3 ~ V0+ 0.3	V
Input voltage	VI		*1	-0.3 ~ VDD+ 0.3	V
Storage temperature	Tstg			-45 ~ +125	℃

10.2 Recommended operating conditions

Item	*Symbol*	*Pin*	*Min.*	*Typ.*	*Max.*	*Unit*	*Note*
Supply voltage	VDD1	VDD	1.7		3.3	V	*1
	VDD2		2.4		3.3	V	*2
	VEE	VEE	2.4		3.3	V	*3
Operating voltage	V0	V0	5		15	V	*4
	VOUT	VOUT			15	V	
	VREG	VREG			VOUT*0.9	V	
	VREF	VREF	2.1		3.3	V	*5
Operating temperature	Topr		-30		85	℃	

*1 In case of VBA output doesn't use.

*2 In case of VBA output use.

*3 Power supply for internal boosting circuit. If applied voltage same as VDD, connect to VDD.

*4 Voltage V0>V1>V2>V3>V4>VSS must always satisfied.

*5 Voltage VEE > VREF must always satisfied.

11. DC characteristics

VSS=0V , VDD = 1.7 ~3.3V , Ta = -30 ~85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
High level input voltage	VIH		0.8VDD	0.9VDD	VDD	V	※ 1
Low level input voltage	VIL		0	0.1VDD	0.2VDD	V	※ 1
High level output current	IOH1	VOH = VDD-0.4V	-2.7	-3.2	-3.5	mA	※ 2
Low level output current	IOL1	VOL= 0.4V	2.7	3.2	3.5	mA	※ 2
High level output current	IOH2	VOH = VDD-0.4V	-0.8	-1.0	-1.2	mA	※ 3
Low level output current	IOL2	VOL= 0.4V	0.8	1.0	1.2	mA	※ 3
Input leakage current	ILI1	VI = VSS or VDD	-2	0	2	µA	※ 4
	ILI2	VI = VSS or VEE	-0.3	0	0.3	µA	※ 5
Output leakage current	ILO	VI = VSS or VDD	-2	0	2	µA	※ 6
LCD driver output resistance	RON	Δ |Von| = 0.5V, V0=10V	1.0	1.3	1.6	KΩ	※ 7
		Δ |Von| = 0.5V, V0=6V	1.2	1.7	2.2	KΩ	※ 7
Standby current through VDD pin	ISTB	CK=0, CSB=VDD, Ta=25°C, VDD=3V		5	15	µA	※ 8
Oscillator frequency (variable gradation mode, 4096 or 256 color mode)	$Fosc_1$	VDD=3V , Ta=25°C, Rf setting = (Rf2,Rf1,Rf0)=(000)	260	372	484	KHz	※ 9
Oscillator frequency (16 gradation mode)	$Fosc_2$	VDD=3V, Ta=25 °C, Rf setting = (Rf2,Rf1,Rf0)=(000)	122	180	240	KHz	※10
Oscillator frequency (8 gradation mode)	$Fosc_3$	VDD=3V, Ta=25 °C, Rf setting = (Rf2,Rf1,Rf0)=(000)	56	84	112	KHz	※11
Oscillator frequency (monochrome mode)	$Fosc_4$	VDD=3V , Ta=25°C, Rf setting = (Rf2,Rf1,Rf0)=(000)	8	12	16	KHz	※12
Booster output voltage on VOUT pin	VOUT1	Five times boosting RL = 500KΩ (VOUT-VSS)	5*VEE *0.95			V	※13
	VOUT2	Four times boosting RL = 500KΩ (VOUT-VSS)	4*VEE *0.95			V	※14
	VOUT3	Three times boosting RL = 500KΩ (VOUT-VSS)	3*VEE *0.95			V	※15
	VOUT4	Two times boosting RL = 500KΩ(VOUT-VSS)	2*VEE *0.95			V	※16
Current consumption	IDD1	VDD = 3V, 5 times booster All ON pattern		90	110	µA	※17
	IDD2	VDD = 3V, 5 times booster Checker pattern		155	180	µA	※18
VBA output voltage	VBA	VDD =2.4V~3.3V	0.9VDD*0.97	0.9VDD	0.9VDD*1.03	V	VBA
VREG output voltage	VREG	VEE =2.4V~3.3V, VREF=0.9VEE, N times boosting (N=2 to 5)	(VREF*N) *0.95	VREF*N *1	(VREF*N) *1.03	V	※19

Relationship of oscillating frequency (fosc) and external clock frequency (fCK) to LCD frame frequency (fFLM) is each display mode

Original oscillating clock	Display mode	Ratio of display duty cycle (1/D)			Pin used
		1/82, 1/77, 1/62	1/47, 1/32	1/17	
When use built-in oscillating circuit (fosc)	Variable gradation	fosc/(2*31*D)	fosc/(4*31*D)	fosc/(8*31*D)	FLM
	Simple gradation (4096 color)	fosc/(2*15*D)	fosc/(4*15*D)	fosc/(8*15*D)	
	Simple gradation (256 color)	fosc/(2*7*D)	fosc/(4*7*D)	fosc/(8*7*D)	
	Monochrome	fosc/(2*1*D)	fosc/(4*1*D)	fosc/(8*1*D)	
When use external clock from CK pin. (fCK)	Variable gradation	fCK/(2*31*D)	fCK /(4*31*D)	fCK /(8*31*D)	
	Simple gradation (4096 color)	fCK/(2*15*D)	fCK/(4*15*D)	fCK/(8*15*D)	
	Simple gradation (256 color)	fCK /(2*7*D)	fCK /(4*7*D)	fCK /(8*7*D)	
	Monochrome	fCK /(2*1*D)	fCK /(4*1*D)	fCK /(8*1*D)	

Pin used:

※ **1** D0-D15, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, CLK, LP, FLM, M, P/S, RESB, TEST pins.

※ **2** D0~D15 pins

※ **3** LP, FLM, M, CLK pins

※ **4** CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST pins

※ **5** VREF pin

※ **6** Applied when D0~D15, CLK, LP, FLM, and M are in the state of high impedance.

※ **7** SEGA0~SEGA127, SEGB0~SEGB127, SEGC0~SEGC127. DSEGA0~DSEGA1, DSEGB0~DSEGB0 , DSEGC0~DSEGC1 , COM0~COM79, COMA, COMB pins Resistance when being applied 0.5V between each output pin and each power supply (V0, V1, V2, V3, V4) and when being applied 1/9 bias.

※ **8** VDD pin, VDD pin current without load at the stoppage of original oscillating clock and at non-select (CSB=VDD)

※ **9** Oscillating frequency, when using the built-in oscillating circuit (variable gradation display mode,4096 or 256 color mode)

※ **10** Oscillating frequency, when using the built-in oscillating circuit (16 gradation fixed display mode)

※ **11** Oscillating frequency, when using the built-in oscillating circuit (8 gradation fixed display mode)

※ **12** Oscillating frequency, when using the built-in oscillating circuit (monochrome display mode)

※ **13** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 5 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/82 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1” ,(BF1,BF0)=(1,1)

※ **14** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 4 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/82 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1” ,(BF1,BF0)=(1,1)

※ **15** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 3 times

is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/82 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1” ,(BF1,BF0)=(1,1)

※ **16** VOUT pin. When using the built-in oscillating circuit, the built-in power supply is used, and boosting 2 times is used, this pin is applied. VEE=2.4~3.3 V, The electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Measuring conditions: bias=1/5~1/9, 1/82 duty, without load. RL=500 KΩ (between VOUT and VSS), C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1” ,(BF1,BF0)=(1,1)

※ **17** VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 5 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display ALL ON pattern {Rf2, Rf1, Rf0 = (“0 0 0 ”) }(on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE , VBA=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1” , NLIN=”0”, (BF1,BF0)=(1,1),1/82 duty , 1/9 bias,(BF1,BF0)=(1,1).

※ **18** VDD, VEE pin. When the built-in oscillating circuit and built-in power supply are used and there is no access from MPU. This pin is applied. Boosting 5 times is used the electronic control is preset (The code is (“1 1 1 1 1 1 1”)). Display a checkered pattern ,{Rf2, Rf1, Rf0 = (“0 0 0 ”) } (on monochrome display mode) and LCD driver pin with no load. Measuring conditions: VDD=VEE , VBA=VREF, C1=C2=1.0μF, C3=0.1μF, DCON=AMPON=”1” , NLIN=”0” ,(BF1,BF0)=(1,1) ,1/82 duty , 1/9 bias,(BF1,BF0)=(1,1)

※ **19** VREG pin. Measuring conditions: N times boosting(N=2~5), electronic control = “1 1 1 1 1 1 1” , Display a checkered pattern , DCON=AMPON=”1” , NLIN=”0” ,1/82 duty , VDD=VEE , VBA=VREF , C1=C2=1.0μF, C3=0.1μF , no load

Note: The capacitor C1 is use for booster related pin.

CAP1+ , CAP1- , CAP2+ , CAP2- , CAP3+ , CAP3- , CAP4+ , CAP4- , VOUT

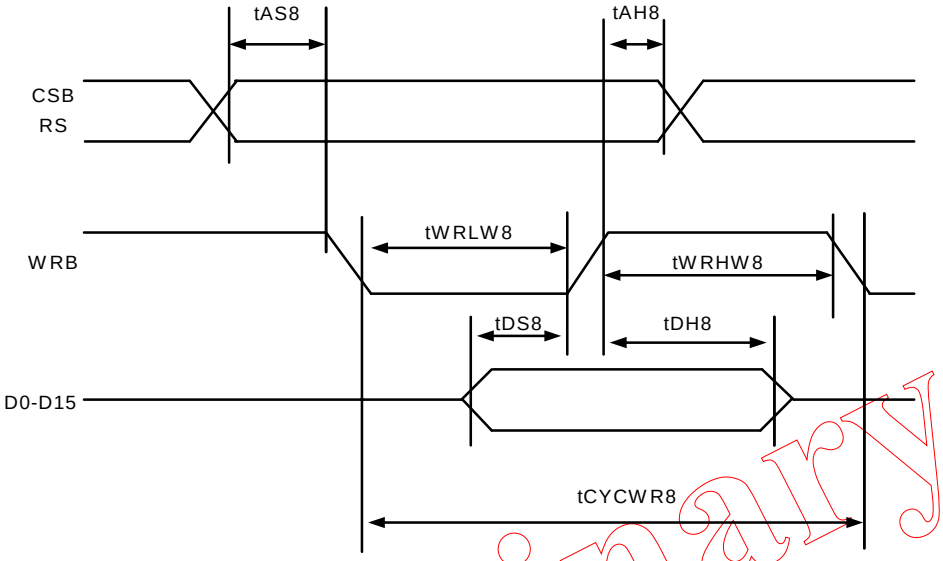
The capacitor C2 is use for bias related pin.

V0 , V1 , V2 , V3 , V4

The capacitor C3 is use for VREG pin.

12. AC characteristic

(1) 80-family MCU write timing



VSS=0V, VDD = 2.7~3.3V , Ta = -30~+85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in write	tCYCWR8		200			ns	WRB
Write pulse “L” width	tWRLW8		60			ns	(R/WB)
Write pulse “H” width	tWRHW8		135			ns	
Data setup time	tDS8		60			ns	D0~D15
Data hold time	tDH8		5			ns	

VSS=0V, VDD = 2.4~2.7V , Ta = -30~+85℃

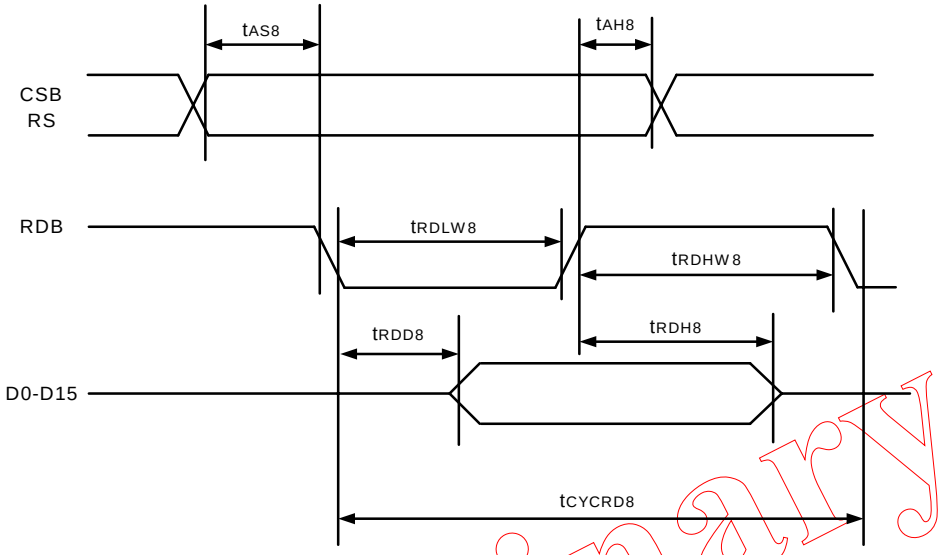
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in write	tCYCWR8		250			ns	WRB
Write pulse “L” width	tWRLW8		80			ns	(R/WB)
Write pulse “H” width	tWRHW8		160			ns	
Data setup time	tDS8		80			ns	D0~D15
Data hold time	tDH8		10			ns	

VSS=0V, VDD = 1.7~2.4V , Ta = -30~+85℃

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in write	tCYCWR8		500			ns	WRB
Write pulse “L” width	tWRLW8		140			ns	(R/WB)
Write pulse “H” width	tWRHW8		350			ns	
Data setup time	tDS8		100			ns	D0~D15
Data hold time	tDH8		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(2) 80-family MCU read timing



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85°C

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in read	tCYCRD8		380			ns	RDB(E)
Read pulse “L” width	tRDLW8		200			ns	
Read pulse “H” width	tRDHW8		170			ns	
Data setup time	tRDD8	CL = 80 pF			210	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85°C

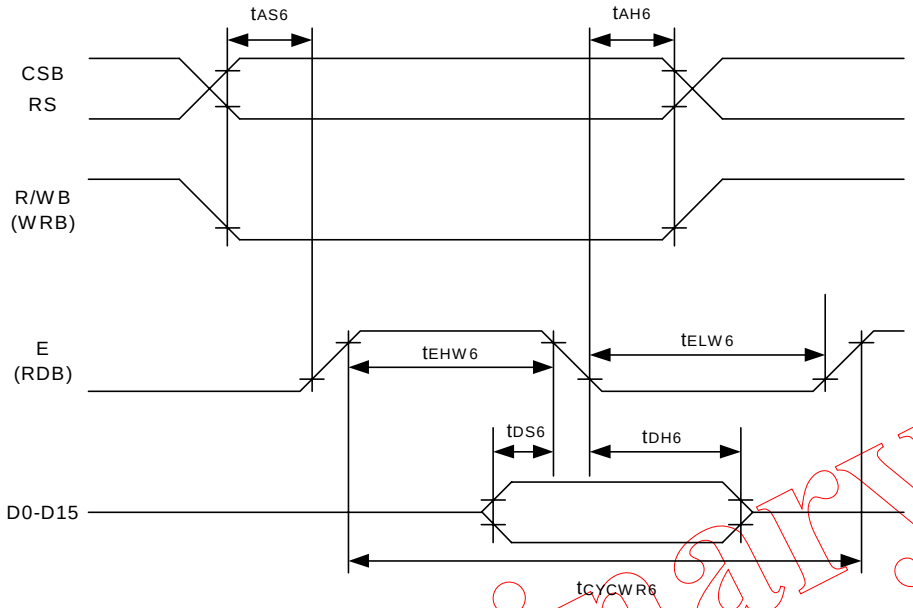
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in read	tCYCRD8		540			ns	RDB(E)
Read pulse “L” width	tRDLW8		290			ns	
Read pulse “H” width	tRDHW8		230			ns	
Data setup time	tRDD8	CL = 80 pF			300	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS=0V , VDD = 1.7~2.4V , Ta = -30~+85°C

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH8		0			ns	CSB
Address setup time	tAS8		0			ns	RS
System cycle time in read	tCYCRD8		840			ns	RDB(E)
Read pulse “L” width	tRDLW8		440			ns	
Read pulse “H” width	tRDHW8		380			ns	
Data setup time	tRDD8	CL = 80 pF			450	ns	D0~D15
Data hold time	tRDH8		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(3) 68-family MCU write timing



VSS=0V , VDD = 2.7 ~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCWR6		200			ns	
Write pulse “L” width	tELW6		60			ns	RDB(E)
Write pulse “H” width	tEHW6		135			ns	
Data setup time	tDS6		60			ns	D0~D15
Data hold time	tDH6		5			ns	

VSS=0V , VDD = 2.4 ~2.7V , Ta = -30~+85℃

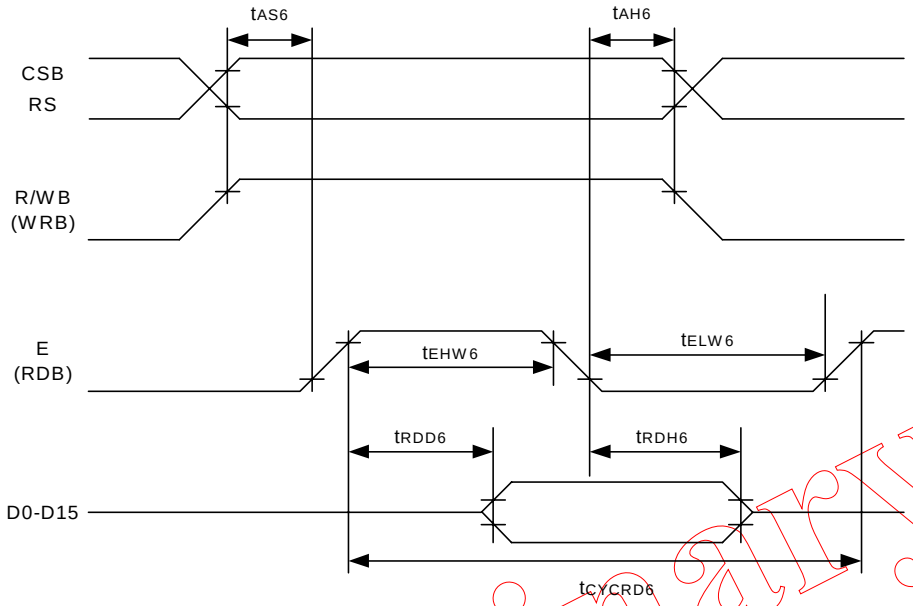
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCWR6		250			ns	
Write pulse “L” width	tELW6		80			ns	RDB(E)
Write pulse “H” width	tEHW6		160			ns	
Data setup time	tDS6		80			ns	D0~D15
Data hold time	tDH6		10			ns	

VSS=0V , VDD = 1.8 ~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in write	tCYCWR6		500			ns	
Write pulse “L” width	tELW6		140			ns	RDB(E)
Write pulse “H” width	tEHW6		350			ns	
Data setup time	tDS6		100			ns	D0~D15
Data hold time	tDH6		20			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(4) 68-family MCU read timing



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in read	tCYCRD6		380			ns	
Write pulse “L” width	tELW6		200			ns	RDB(E)
Write pulse “H” width	tEHW6		170			ns	
Data setup time	tRDD6	CL=50pF			210	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85℃

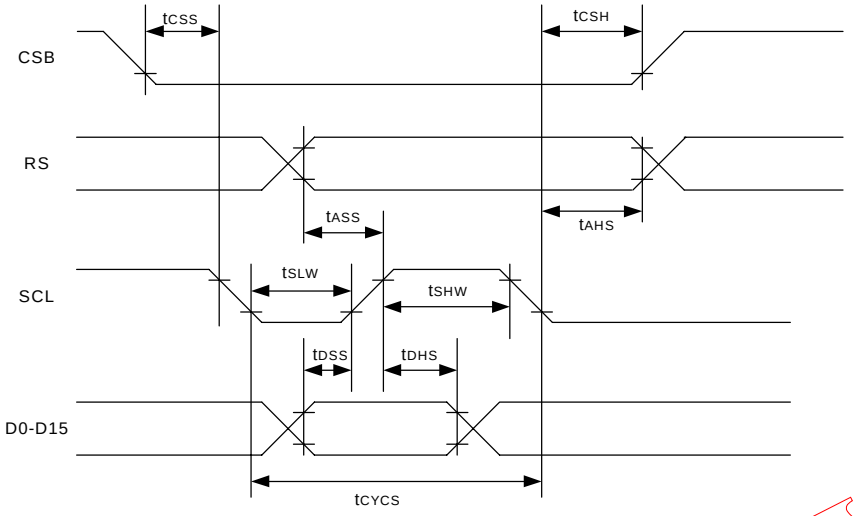
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in read	tCYCRD6		540			ns	
Write pulse “L” width	tELW6		290			ns	RDB(E)
Write pulse “H” width	tEHW6		230			ns	
Data setup time	tRDD6	CL=50pF			300	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 1.8~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Address hold time	tAH6		0			ns	CSB
Address setup time	tAS6		0			ns	RS
System cycle time in read	tCYCRD6		1000			ns	
Write pulse “L” width	tELW6		450			ns	RDB(E)
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tRDD6	CL=50pF			650	ns	D0~D15
Data hold time	tRDH6		10			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(5) Serial interface timing diagram



VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85°C

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

VSS=0V , VDD = 2.4~2.7V , Ta = -30~+85°C

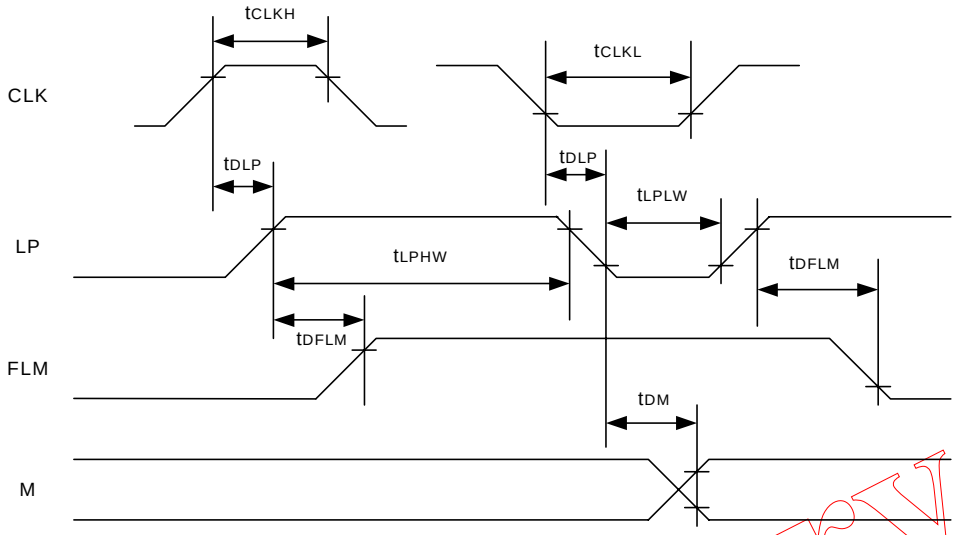
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		50			ns	RS
Address hold time	tAHS		50			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		50			ns	CSB
CSB hold time	tCSH		60			ns	

VSS=0V , VDD = 1.7~2.4V , Ta = -30~+85°C

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Serial clock period	tCYCS		230			ns	SCL
SCL pulse “H” width	tSHW		100			ns	
SCL pulse “L” width	tSLW		100			ns	
Address setup time	tASS		80			ns	RS
Address hold time	tAHS		80			ns	
Data setup time	tDSS		100			ns	SDA
Data hold time	tDHS		100			ns	
CSB-SCL time	tCSS		80			ns	CSB
CSB hold time	tCSH		100			ns	

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(6) Display control timing



Input timing (Slave mode) VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CLK pulse “H” width	tCLKH		1.6			µs	CLK
CLK pulse “L” width	tCLKL		1.6			µs	
LP pulse “H” width	tLPHW		50			µs	LP
LP pulse “L” width	tLPLW		50			µs	
LP delay time	tDLP		-1		1	µs	
FLM delay time	tDFLM		-1		1	µs	FLM
M delay time	tDM		-1		1	µs	M

Input timing (Slave mode) VSS=0V , VDD = 1.7~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CLK pulse “H” width	tCLKH		1.6			µs	CLK
CLK pulse “L” width	tCLKL		1.6			µs	
LP pulse “H” width	tLPHW		50			µs	LP
LP pulse “L” width	tLPLW		50			µs	
LP delay time	tDLP		-1		1	µs	
FLM delay time	tDFLM		-1		1	µs	FLM
M delay time	tDM		-1		1	µs	M

output timing (Master mode) VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

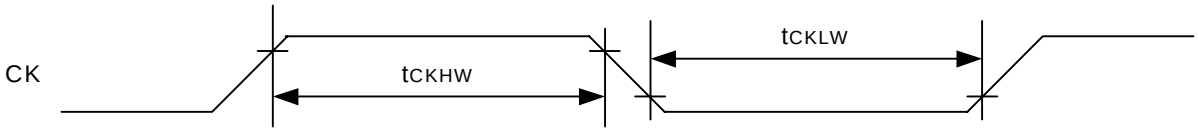
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
LP delay time	tDLP	CL =15 pF	-500		500	ns	LP
FLM delay time	tDFLM		-500		500	ns	FLM
M delay time	tDM		-500		500	ns	M

output timing (Master mode) VSS=0V , VDD = 1.7~2.4V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
LP delay time	tDLP	CL =15 pF	-1000		1000	µs	LP
FLM delay time	tDFLM		-1000		1000	µs	FLM
M delay time	tDM		-1000		1000	µs	M

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

(7) Master clock input timing



VSS=0V , VDD = 2.4~3.3V , Ta = -30~+85℃

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CK pulse “H” width (1)	tCKHW1		1.2		1.4	μs	CK
CK pulse “L” width (1)	tCKLW1		1.2		1.4	μs	※ 1
CK pulse “H” width (2)	tTCKHW2		5.4		6.5	μs	CK
CK pulse “L” width (2)	tCKLW2		5.4		6.5	μs	※ 2
CK pulse “H” width (3)	tCKHW3		3.8		4.5	μs	CK
CK pulse “L” width (3)	tCKLW3		3.8		4.5	μs	※ 3

VSS=0V , VDD = 1.7~2.4V , Ta = -30~+85℃

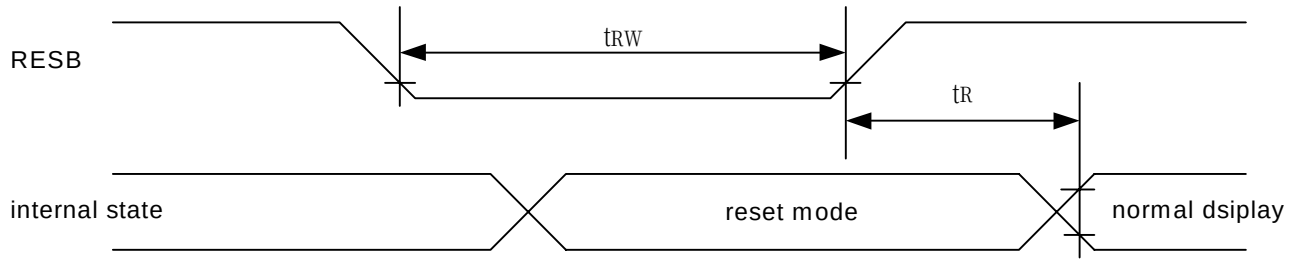
Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
CK pulse “H” width (1)	tCKHW1	Note1	1.2		1.4	μs	CK
CK pulse “L” width (1)	tCKLW1	Note1	1.2		1.4	μs	※ 1
CK pulse “H” width (2)	tCKHW2	Note2	5.4		6.5	μs	CK
CK pulse “L” width (2)	tCKLW2	Note2	5.4		6.5	μs	※ 2
CK pulse “H” width (3)	tCKHW3	Note3	3.8		4.5	μs	CK
CK pulse “L” width (3)	tCKLW3	Note3	3.8		4.5	μs	※ 3

※ 1 Applied when the gradation display mode. MON=”0” , PWM=”0”

※ 2 Applied when the simple gradation mode. MON=”0” , PWM=”1”

※ 3 Applied when the monochrome mode. MON=”1”

(8) Reset timing



VSS=0V, VDD = 2.4~3.3V, Ta = -30~+85°C

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Reset time	tR				1	µs	
Reset pulse "L" width	tRW		10			µs	RESB

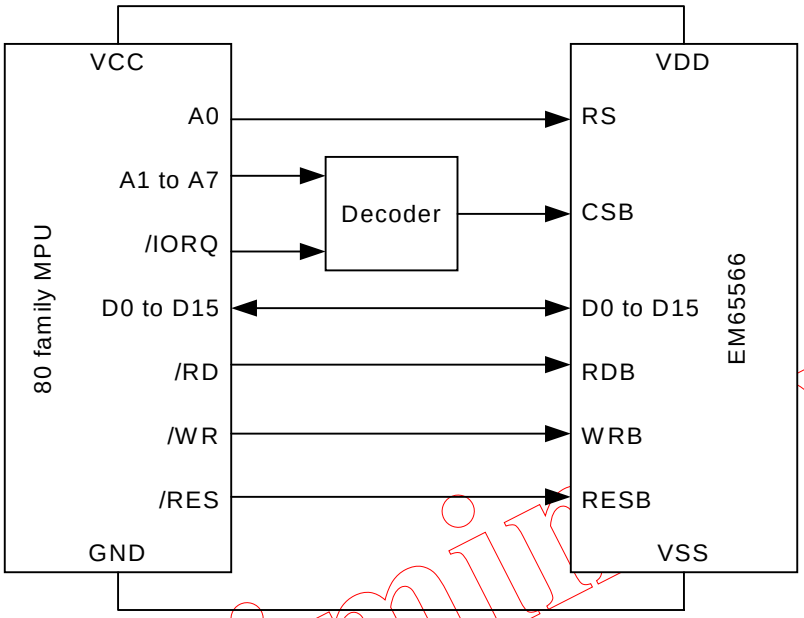
VSS=0V, VDD = 1.8~2.4V, Ta = -30~+85°C

Item	*Symbol*	*Condition*	*Min.*	*Typ.*	*Max.*	*Unit*	*Pin used*
Reset time	tR				1.5	µs	
Reset pulse "L" width	tRW		10			µs	RESB

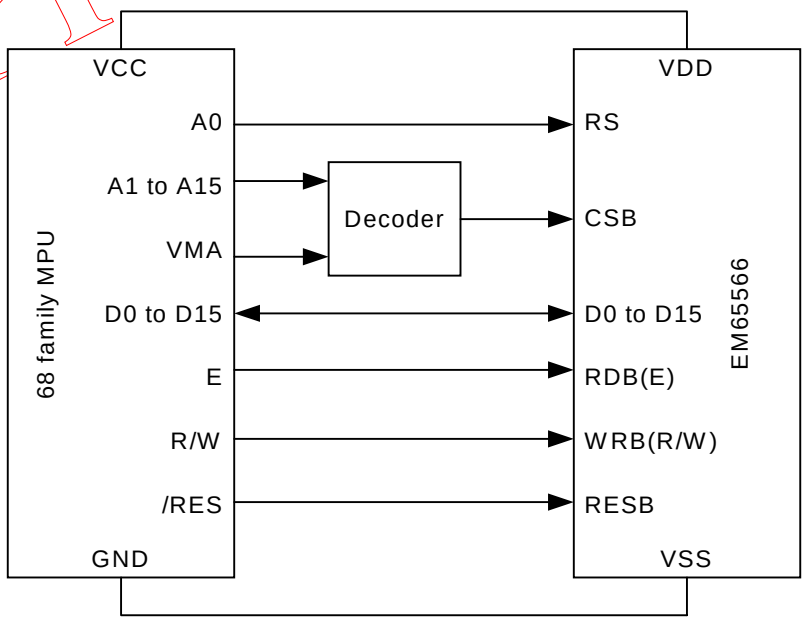
Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

13. Application circuit

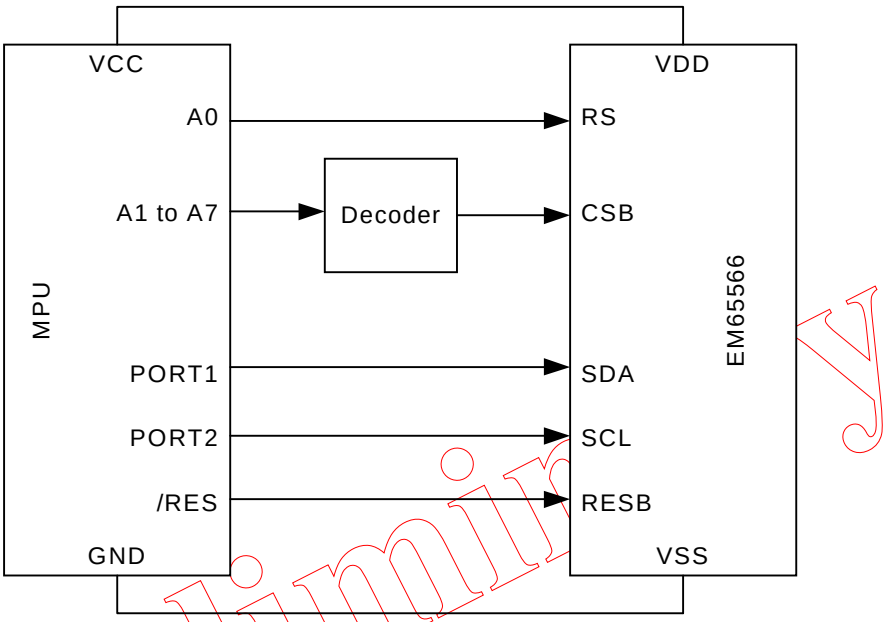
(1) Connection to 80-family MCU



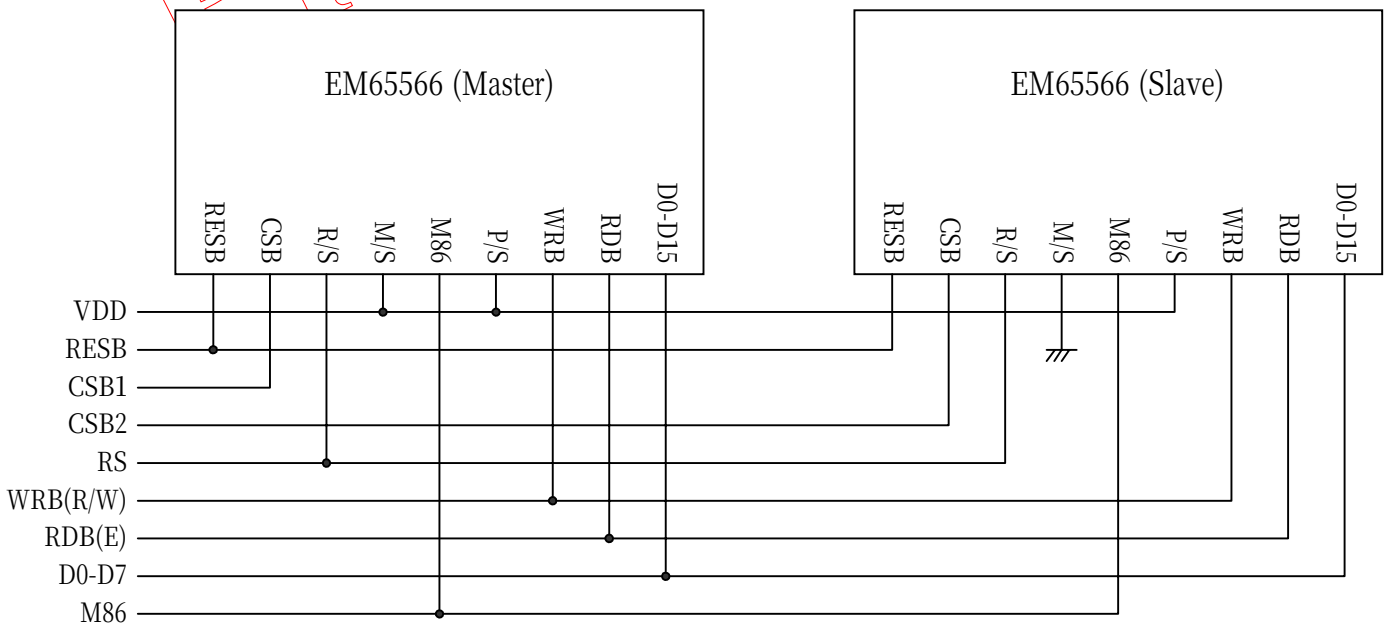
(2) Connection to 68-family MCU



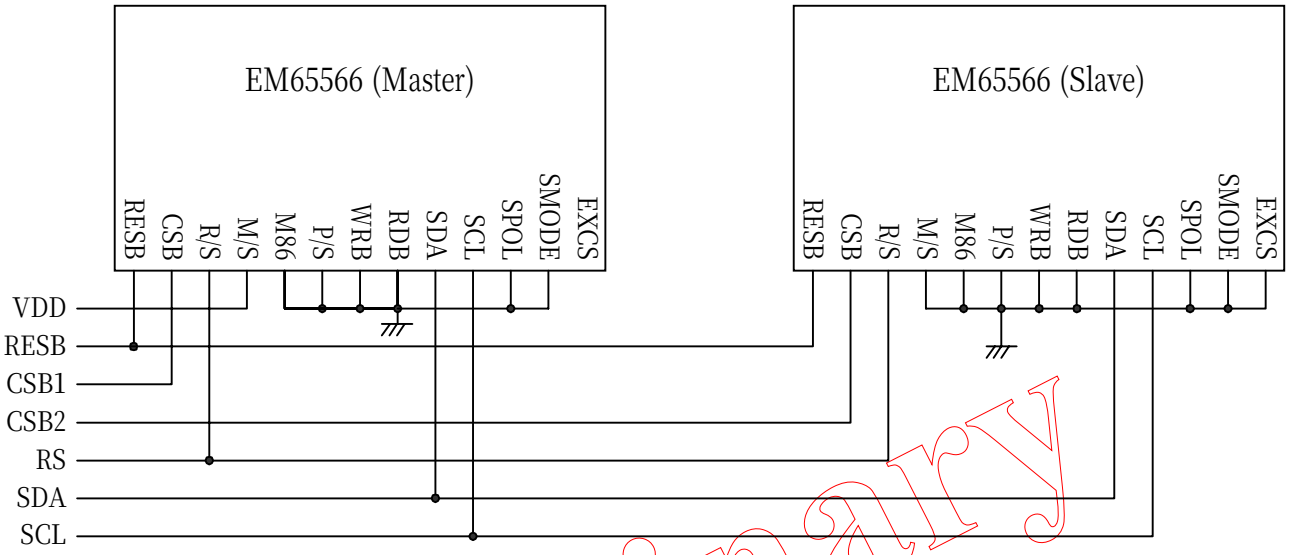
(3) Connection to the MCU with serial interface



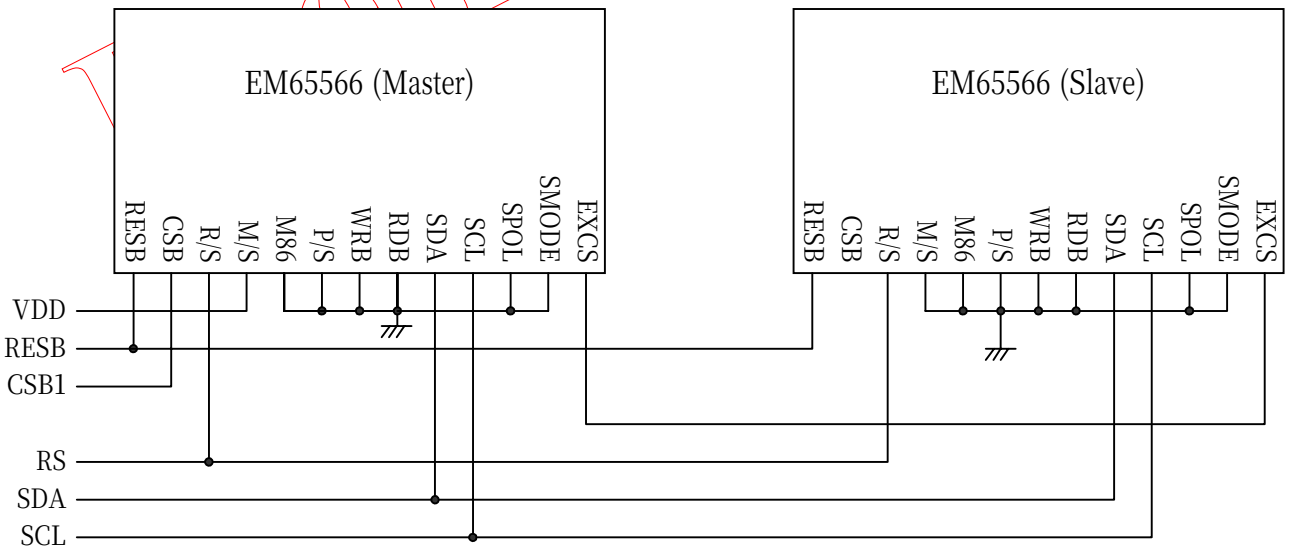
(4) Connection to Master / Slave about interface (parallel interface)



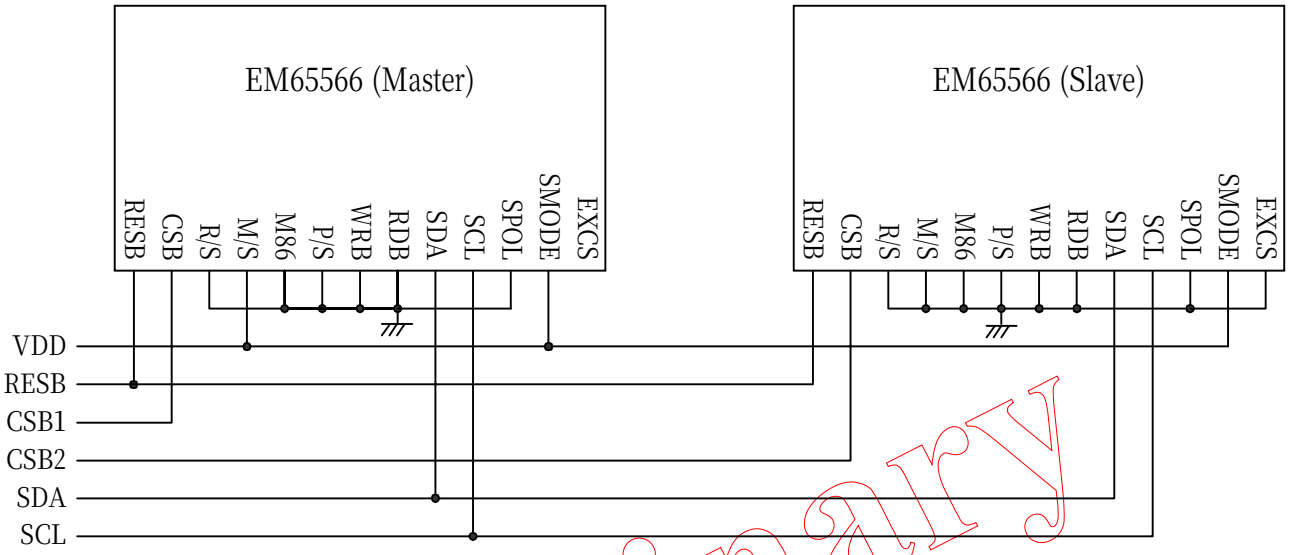
(5) 4 wires type serial interface with two chip enable signals



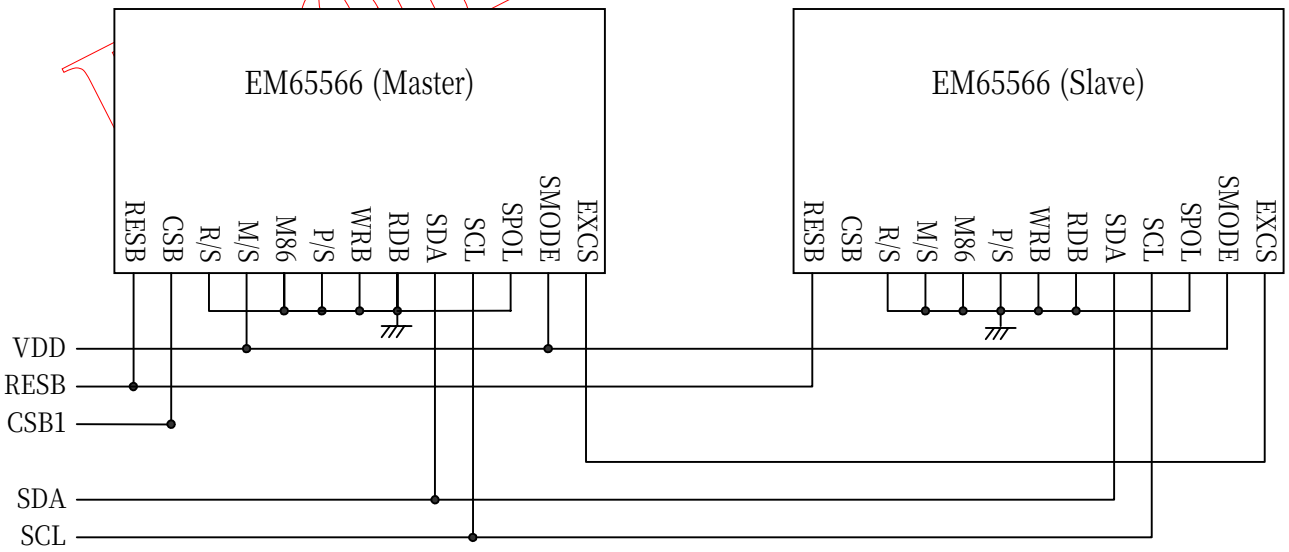
(6) 4 wires type serial interface with one chip enable signal



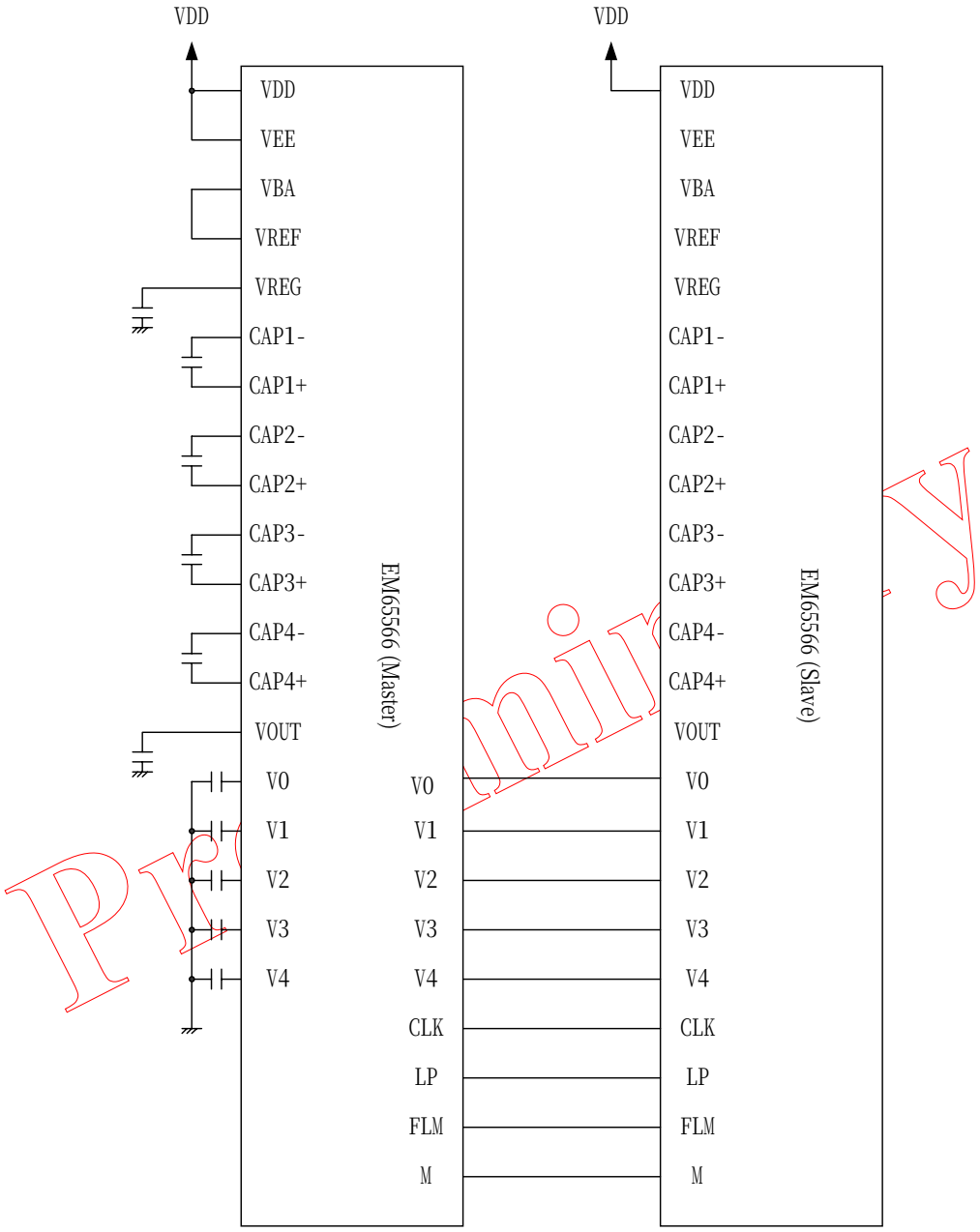
(7) 3 wires type serial interface with two chip enable signals



(8) 3 wires type serial interface with one chip enable signal



(9)Connection to master / slave about power block



Caution of application about master / slave

* The master chip control display timing (CLK,LP,FLM, and M). When making display OFF on the master chip, the master chip can not output the display timing. When making display OFF , beforehand set display OFF to the slave chip and set display OFF to the master chip.

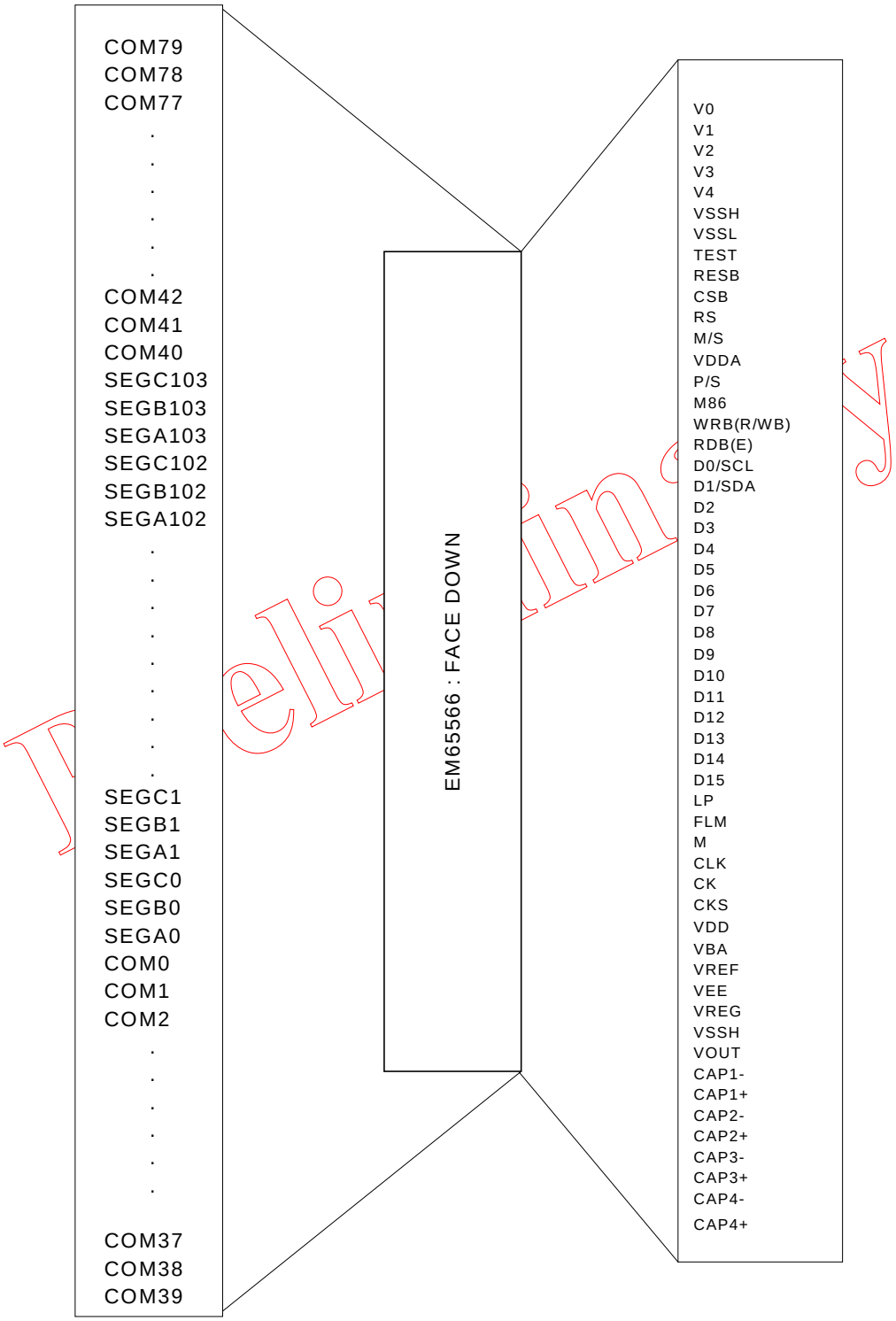
* When setting halt command, turn off the internal power supply, and output VSS level from LCD drive output pins , is set display OFF state. Because the master chip can not supply output voltage to the slave chip , beforehand set display OFF to the slave chip.

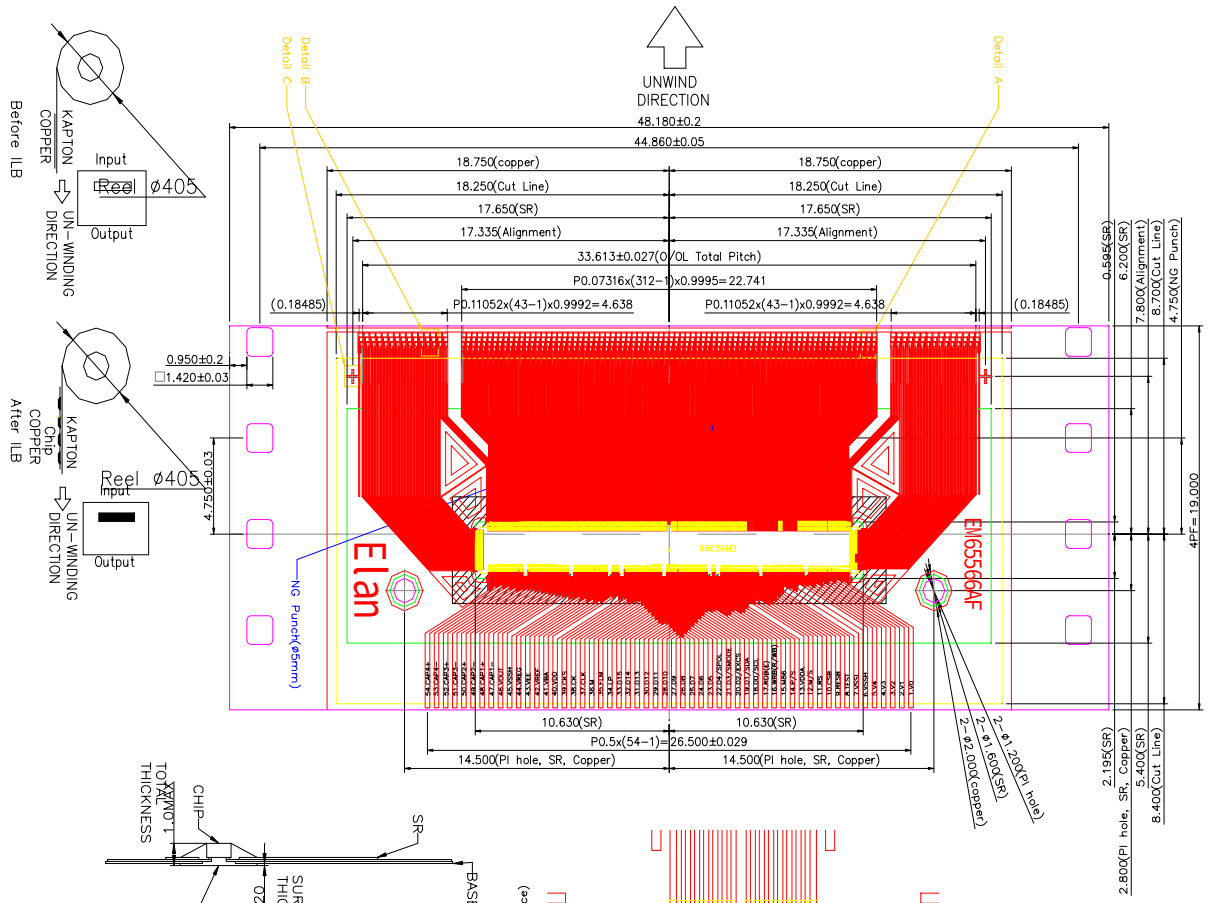
*In above connection example, the master chip is only available the electronic volume control.

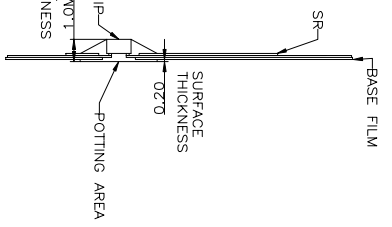
14. COF information

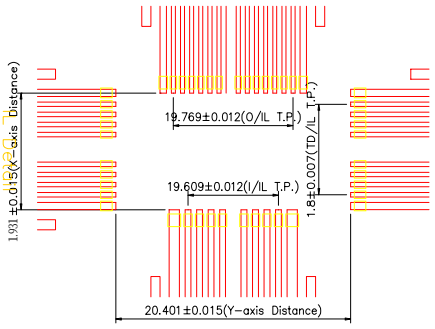
EM65566AF package

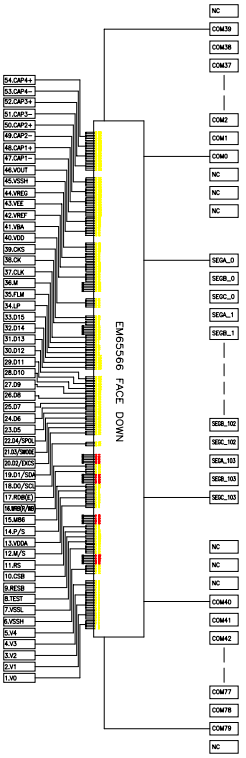
Pin connection diagram (80 x 104RGB outputs)





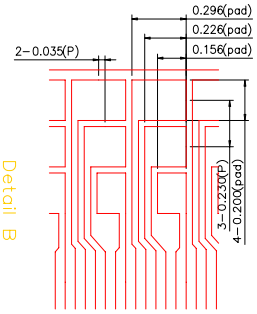






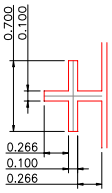
NOTES:

1. All Chamfer is R0.20mm if not specified
2. All SR Dimension Tolerance ±0.200mm if not specified
3. All SL Dimension Tolerance ±0.05mm if not specified
4. PKG Reel Size : ø405mm
5. Input IL total pitch from top 2nd to bottom 2nd
6. Output IL total pitch from top 2nd to bottom 2nd
7. IL total pitch in TD from right 2nd to left 2nd
8. MIN Pitch=50um(IL)

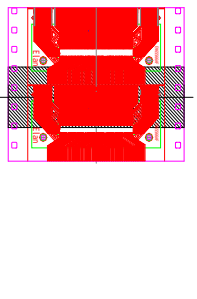


Detail B Scale 10:1

Detail A Scale 10:1

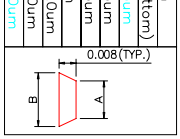


Detail C Scale 5:1



Detail for Splicing

Inner Lead Cross Section		
Item	A (Top)	B (Bottom)
Input IL	Min. 25um	32±5um
Output IL	Min. 15um	22±5um
TD IL	Min. 15um	22±5um
Outer Lead Cross Section		
Input OL	Min. 220um	250±20um
Output OL	Min. 35um	55±10um
Output OL	Min. 25um	37±10um



TAPE SPEC	48SW
PRODUCT PITCH	4 PERFORATIONS (19.00mm)
MATERIAL	
PLATING	Sn 0.25±0.05μm
SOLDER RESIST	SN-9000 20±15μm
Sumitomo CCL	Copper: 8±1.5μm
	PI: Kapton 38±3μm

UNIT: mm			
SCALE: 4:1			
DESIGNED BY	DRAWN BY	CHECK BY	APPROVED BY
Steven Yu	Steven Yu		
2003/01/27	2003/01/27		

GENERAL TOLERANCE .XX: ±0.05 .XXX: ±0.050

DRAWING NO.	S-30100-6612
PART NO.	30100-6612
REV	2
SHEET	1/1
TITLE	COF for EM65566
CAD FILE	S30100C2.dwg