Elan Microelectronics Crop.

ELAN RISC II™ series

EPD1600

June 20, 2001
Version 1.2

Specification Revision History		
Version	**Content**	**Date**
1.0	Initial version	Feb 7,2001
1.2	a. NEW CPU series rename to ***ELAN RISC II™ series*** a. Update TEST pin type b. Exchange the pin number of V4 & VCA pad c. Modify LVD spec to Vdet +/- 0.1V, and add the Vdet hysteresis voltage description d. Modify the DC Specification temperature range to Ta=0~+40 °C e. Add Pad Diagram f. Specify the V0 spec.: VDD=2.3V~3.3V, V0= Typ +/- 4% g. Specify the Vref temperature coefficient: 7mV/°C h. EPG-1600 rename to **EPG1600.**	June 20,2001

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I. General Description

ELAN RISC II™ series MCU is a 8 bit uC based data processor IC for use on palm top devices. Integrated on the chip are large ROM size and large RAM size, 8*8 hardware multiplier, key input circuit, SPI, melody timer, EL ,low voltage detection and embedded LCD driver(98*32).

II. Feature

(1) Kernel Feature:

- Operating voltage:2.2~3.6V.
- Maximum operation Speed: 10MHz clock.
- One Instruction cycle time = 2* System clock time
- 8 bit CPU with 80 instructions.
- 48 K words program ROM.
- 1M words data ROM.
- 128 bytes unbanked RAM, 8K bytes banked RAM .
- RAM stack can achieve maximum 128 levels.
- Enhanced TABLE LOOK UP function(1 or 2 cycles)
- High capacity memory access ability.
- Register to Register instruction.
- Compare and Branch in one instruction (2 cycles).
- Single Repeat function.
- 8*8 hardware multiplier.
- Decimal ADD and SUB instruction.
- Full range CALL and JUMP ability (2 cycles).

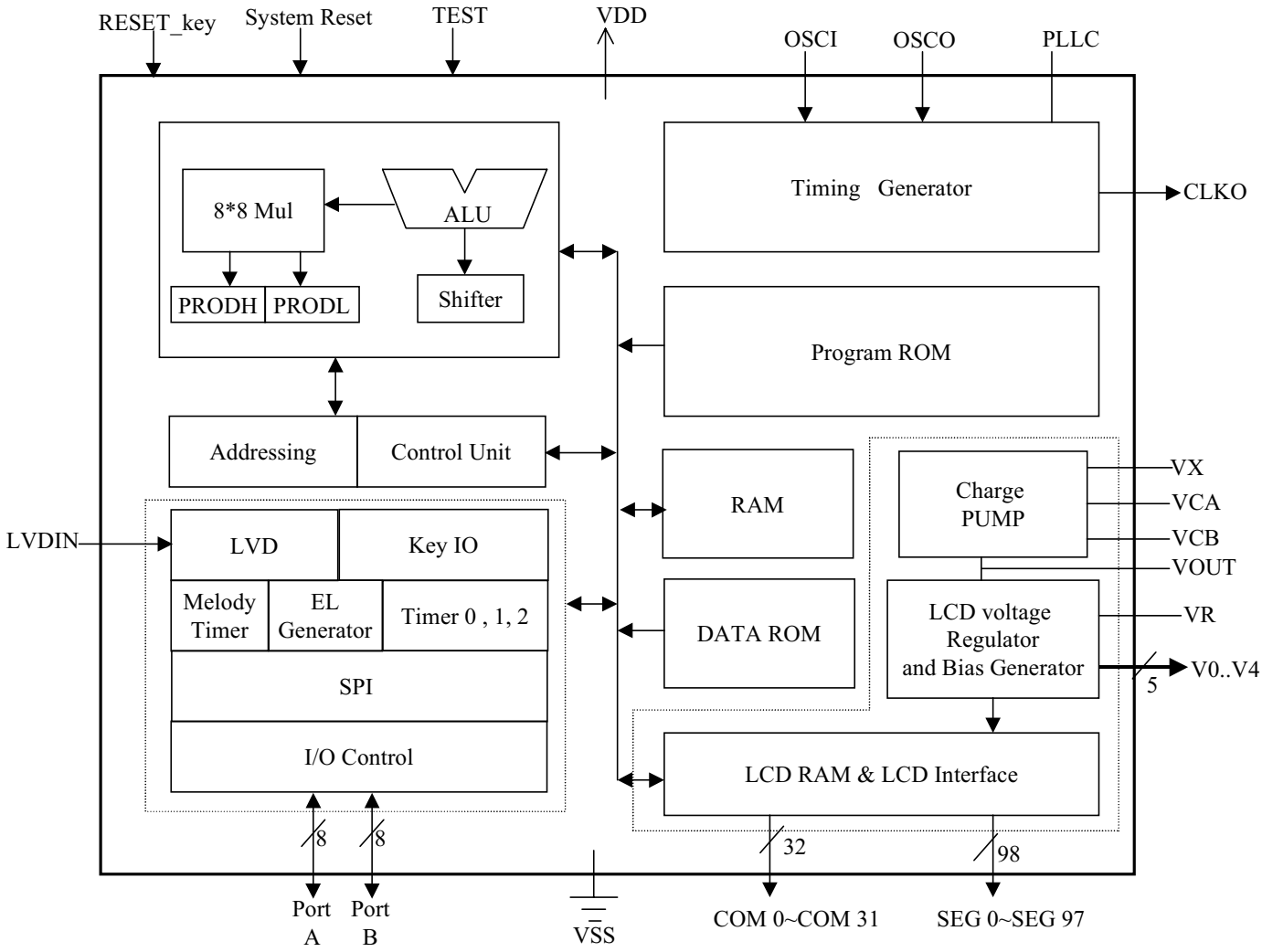
(2) Peripheral Feature:

- 16 I/O pins (Port A ~ Port B)
- One 16 bits general purpose timer, two 8 bits general purpose timer, one melody timer
- EL or IR generator.
- Low voltage detector.
- SPI (Serial Peripheral Interface)
- Clock output for external device.
- Key input and strobe function
- Embedded LCD Driver.(1/11,1/16,1/24 & 1/32 duty selectable)

(3) Special micro controller Feature:

- Watchdog Timer with its own on-chip RC oscillator
- CPU mode: SLEEP MODE, IDLE MODE, SLOW MODE, FAST MODE
- PLL frequency adjustable

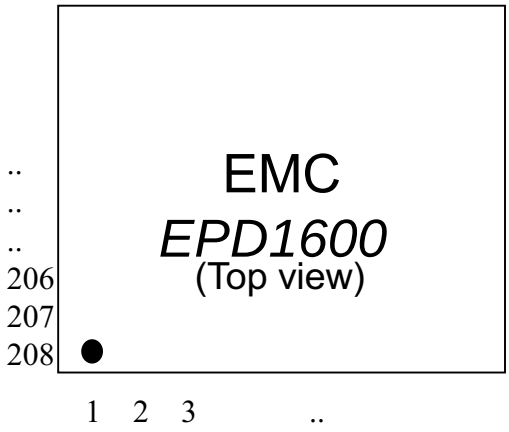
III. Block Diagram



IV. ELAN RISC II™ Series Part List

Part number	PROM	D-ROM	RAM	LCD	Peripheral	I/O pins
EPD8000	48k*16	512K*16	8k*8	Internal 98*32	SPI, Key, Melody, EL,LVD	16 (PortA~B)
EPD1600	**48k*16**	**1M*16**	**8k*8**	**Internal 98*32**	**SPI, Key, Melody, EL,LVD**	**16 (PortA~B)**

V. Pin Assignment



No.	Pin NAME	No.	Pin NAME	No.	Pin NAME	No.	Pin NAME
1	V4	53	SEG69	105	SEG29	157	PA.6
2	VR	54	N.C.	106	SEG28	158	N.C.
3	V0	55	N.C.	107	SEG27	159	N.C.
4	Vout	56	N.C.	108	SEG26	160	N.C.
5	V1	57	N.C.	109	SEG25	161	N.C.
6	V2	58	N.C.	110	SEG24	162	N.C.
7	V3	59	N.C.	111	SEG23	163	N.C.
8	VCB	60	SEG68	112	SEG22	164	N.C.
9	COM31	61	SEG67	113	SEG21	165	N.C.
10	COM30	62	SEG66	114	SEG20	166	N.C.
11	COM29	63	SEG65	115	SEG19	167	N.C.
12	COM28	64	SEG64	116	SEG18	168	N.C.
13	COM27	65	SEG63	117	SEG17	169	N.C.
14	COM26	66	SEG62	118	SEG16	170	PA.7 (ON_key)

15	COM25	67	SEG61	119	SEG15(strobe 15)	171	CLKO
16	COM24	68	SEG60	120	SEG14(strobe 14)	172	PB.0(/SPISS)
17	COM23	69	SEG59	121	SEG13(strobe 13)	173	PB.1(SPISCK)
18	COM22	70	SEG58	122	SEG12(strobe 12)	174	PB.2(SPISDO)
19	COM21	71	SEG57	123	SEG11(strobe 11)	175	PB.3(SPISDI)
20	COM20	72	SEG56	124	SEG10(strobe 10)	176	PB.4(CK)
21	COM19	73	SEG55	125	SEG9(strobe 9)	177	PB.5(CHOP)
22	COM18	74	SEG54	126	SEG8(strobe 8)	178	PB.6(MDO2)
23	COM17	75	SEG53	127	SEG7(strobe 7)	179	PB.7(MDO1)
24	COM16	76	SEG52	128	SEG6(strobe 6)	180	Reset_key
25	SEG97	77	SEG51	129	SEG5(strobe 5)	181	SYSTEM RESET
26	SEG96	78	SEG50	130	SEG4(strobe 4)	182	VDD
27	SEG95	79	SEG49	131	SEG3(strobe 3)	183	LVDIN
28	SEG94	80	SEG48	132	SEG2(strobe 2)	184	(Reserved)
29	SEG93	81	SEG47	133	SEG1(strobe 1)	185	(Reserved)
30	SEG92	82	SEG46	134	SEG0(strobe 0)	186	(Reserved)
31	SEG91	83	SEG45	135	COM0	187	(Reserved)
32	SEG90	84	SEG44	136	COM1	188	(Reserved)
33	SEG89	85	SEG43	137	COM2	189	PLLC
34	SEG88	86	SEG42	138	COM3	190	GND
35	SEG87	87	SEG41	139	COM4	191	OSCI
36	SEG86	88	SEG40	140	COM5	192	OSCO
37	SEG85	89	SEG39	141	COM6	193	TEST
38	SEG84	90	SEG38	142	COM7	194	N.C.
39	SEG83	91	SEG37	143	COM8	195	N.C.
40	SEG82	92	SEG36	144	COM9	196	N.C.
41	SEG81	93	SEG35	145	COM10	197	N.C.
42	SEG80	94	SEG34	146	COM11	198	N.C.
43	SEG79	95	SEG33	147	COM12	199	N.C.
44	SEG78	96	SEG32	148	COM13	200	N.C.
45	SEG77	97	N.C.	149	COM14	201	N.C.
46	SEG76	98	N.C.	150	COM15	202	N.C.
47	SEG75	99	N.C.	151	PA.0	203	N.C.
48	SEG74	100	N.C.	152	PA.1	204	N.C.
49	SEG73	101	N.C.	153	PA.2	205	N.C.
50	SEG72	102	N.C.	154	PA.3	206	N.C.
51	SEG71	103	SEG31	155	PA.4	207	VCA
52	SEG70	104	SEG30	156	PA.5	208	VX

Note: Pad 184 ~ Pad 188 is for factory test only. Please do NOT bonding these pads on application circuit.

VI. Pin Description

(1)System pin

Name	I/O type	Description	Note
VDD	-	Power supply	
VSS	-	Ground	
SYSTEM RESET	I	System reset pin	Int. pull-up
RESET_KEY	I	Low voltage related reset pin	Int. pull-up
TEST	I	Test mode select pin(High active)	Int. PULL Down
PLLC	I	PLL capacitor connecting pin	Ext. C to VSS
OSCI	I	X'tal or RC oscillator connecting pin	Ext. R to VDD
OSCO	O	X'tal oscillator connecting pin	
CLKO	O	Clock output pin	
LVDIN	I	Low Voltage detection input pin	

(2)Embedded LCD pin

Name	I/O type	Description	Note
VCA,VCB	-	Charge Pump capacitor. VCA connect 0.1uF Cap. To VCB	
Vout	-	Charge pump output voltage	
VX	-	Protection circuit output voltage	
VR	-	V0 voltage adjust pin.	
V4…V0	O	LCD bias pin	
COM0~ COM31	O	LCD common signal	
SEG0~ SEG97	O	LCD segment signal (SEG0~SEG15 is shared with Key strobe)	

(3)I/O Port

PORT	Bit	Function	I/O type	Description	Notes
Port A	**Bit7**	General Input	I	On key input	Int. Pull up controllable
		Interrupt and wake up	I	Input port interrupt and wake up pin	
	Bit6~0	General Input	I	Key input	2 Int. Pull up resistor controllable
		Interrupt and wake up	I	Input port interrupt and wake up pin	
Port B	**Bit 7**	MDO1	O	Melody positive output	-
		General I/O	I/O		Int. Pull up controllable
	Bit 6	MDO2	O	Melody negative output	-
		General I/O	I/O		Int. Pull up controllable
	Bit 5	CHOP	O	EL CHOP output pin	-
		General I/O	I/O		Int. Pull up controllable

	Bit 4	CK	O	EL CK output pin	-
		General I/O	I/O		Int. Pull up controllable
	Bit 3	SPISDI	I	SPI SDI pin	-
		General I/O	I/O		Int. Pull up controllable
	Bit 2	SPISDO	O	SPI SDO pin	-
		General I/O	I/O		Int. Pull up controllable
	Bit 1	SPISCK	I/O	SPI SCK pin	-
		General I/O	I/O		Int. Pull up controllable
	Bit 0	/SPISS	I	SPI /SS pin	-
		General I/O	I/O		Int. Pull up controllable

VII. Function Descriptions

(1) Kernel Part:

Feature:

1. Large ROM & RAM capacity, high expand ability.
2. Enhanced TABLE LOOK UP function. (1 or 2 cycles)
3. High capacity external memory access ability.
4. Register to Register instruction:
   (i) Register to Register within one cycle.
   (ii) Port to Register or Register to Port within one cycle.
5. Compare and Branch in one instruction(2cycles).
6. Single Repeat function.
7. Decimal ADD and SUB instruction.
8. 8*8 multiply instruction.
9. Full range CALL and JUMP ability(2 cycles).

File Register Map:

RAM size:128 bytes+ 64 bank *128 bytes=8320 bytes

	Addr.	Unbanked		Addr.	Unbanked
SPECIAL REGISTER	00h	**INDF0**		10h	**LCDDATA**
	01h	**FSR0**		11h	**TRL2**
	02h	**PCL**		12h	**PRODL**
	03h	**PCM**		13h	**PRODH**
	04h	**PCH**		14h	**SPRL**
	05h	**BSR**		15h	**SPRM**
	06h	**STKPTR**		16h	**SPRH**
	07h	**BSR1**		17h	(reserved)
	08h	**INDF1**		18h	(reserved)
	09h	**FSR1**		19h	**PORTA**
	0Ah	**ACC**		1Ah	**PORTB**
	0Bh	**TABPTRL**		1Bh	(reserved)
	0Ch	**TABPTRM**		1Ch	(reserved)
	0Dh	**TABPTRH**		1Dh	(reserved)
	0Eh	**CPUCON**		1Eh	(reserved)
	0Fh	**STATUS**		1Fh	(reserved)

CONTROL REGISTER	Addr.	Unbanked		Addr.	Unbanked
	20h	**PFS**		30h	**POST_ID**
	21h	**PACON**		31h	**TRL0L**
	22h	**STBCON**		32h	**TRL0H**
	23h	**DCRB**		33h	**TRL1**
	24h	(reserved)		34h	**TRCON**
	25h	(reserved)		35h	**MTRL**
	26h	(reserved)		36h	**MWTCON**
	27h	(reserved)		37h	**ELCON**
	28h	**LCDCON**		38h	**PAINTSTA**
	29h	(reserved)		39h	**PAINTEN**
	2Ah	(reserved)		3Ah	**INTSTA**
	2Bh	**SPICON**		3Bh	**INTCON**
	2Ch	**SPISTA**		3Ch	(reserved)
	2Dh	**PAWAKE**		3Dh	(reserved)
	2Eh	**LCDARL**		3Eh	(reserved)
	2Fh	**LCDARH**		3Fh	**PBCON**

Addr	Unbanked
40h | 7fh	General purpose RAM

Banked Register(select by BSR)

Addr.	Bank 0	Bank 1	Bank 2	Bank 3	……	Bank 63
80h | FFh	General Purpose RAM	General Purpose RAM	General Purpose RAM	General Purpose RAM	……	General Purpose RAM

#Initial Top of STACK position (STKPTR) locates at 00h.

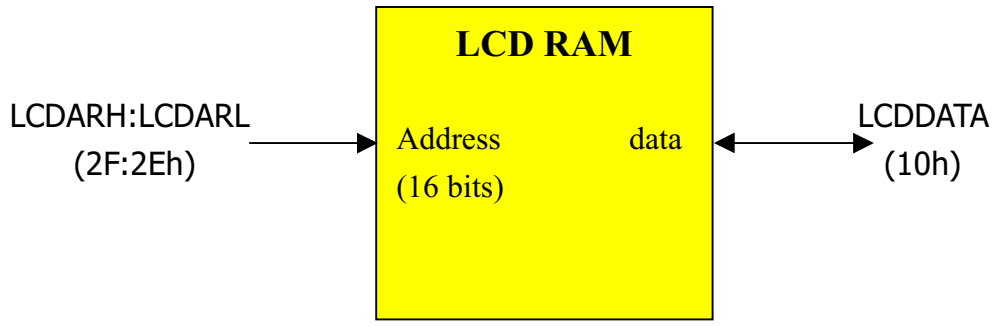
The stack level is bottom up(decrease) start from FFh of BANK 63.

Bit 0~6 of STKPTR use to pointer address from 80h~FFh

Bit 7=1 use to select BANK 63 ,Bit 7=0 use to select BANK 62.

#Each stack level will take 2 bytes, maximum 128 Stack levels.

LCD RAM MAP:



ROM Map:

ROM MAP:

Program ROM: 8 K words* 6 Segments=48k words

Data ROM: 1M words.

Addr.	Type	Segment
0000h | 1FFFh	Program ROM	Segment 0
2000h | 3FFFh		Segment 1
4000h | 5FFFh		Segment 2
6000h | 7FFFh		Segment 3
8000h | 9FFFh		Segment 4
A000h | BFDFh		Segment 5
BFE0h-BFFBh	TEST Program(28 Words)	
BFFCh-BFFFh	Code Option(4 words)	
C000h-FFFFFh	Reserved (Not Implemented)	
Addr.	**Type**	**Range**
100000h | 1FFFFFh	Data ROM	(0~1M words)

Register Description

Remark:

R = Readable bit **W** = Writable bit **-** = Not implement

Addr.	Register name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	Bit 0
0	**INDF0**	R/W							
		Indirect addressing pointer0.							
1	**FSR0**	R/W							
		File select register 0 for INDF0(R0)							
2	**PCL**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
3	**PCM**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8
4	**PCH**	-	-	-	-	-	-	-	-
		-	-	-	-	-	-	-	-
5	**BSR**	Bit 6,7: R (Fix at 0) , Bit6 ~ Bit 0: R/W							
		Bank select register(for INDF0 & general)							
6	**STKPTR**	R/W							
		Stack pointer							
7	**BSR1**	Bit 6,7: R (Fix at 0) , Bit6 ~ Bit 0: R/W							
		Bank select register(for INDF1)							
8	**INDF1**	R/W							
		Indirect addressing pointer1.							
9	**FSR1**	Bit 7: R (Fix at 1) , Bit6 ~ Bit 0: R/W							
		File select register 1 for INDF1(R8)							
A	**ACC**	R/W							
		Accumulator							
B	**TABPTRL**	R/W							
		Table pointer low							
C	**TABPTRM**	R/W							
		Table pointer middle							
D	**TABPTRH**	R/W							
		Table pointer high							
E	**CPUCON**	R/W	R/W	R/W	R	R/W	R	R/W	R/W
		CLKOEN	CKS	LVDEN	/LV	/GLINTD	PS	MS1	MS0
F	**STATUS**	R	R	R/W	R/W	R/W	R/W	R/W	R/W
		/TO	/PD	SGE	SLE	OV	Z	DC	C
10	**LCDDATA**	R/W							
		Indirect register to LCD RAM							
11	**TRL2**	R/W							
		Timer2 reload register							
12	**PRODL**	R/W							
		Multiplier product low							
13	**PRODH**	R/W							
		Multiplier product high							
14	**SPRL**	R/W							
		Shift register low byte of SPI							
15	**SPRM**	R/W							
		Shift register middle byte of SPI							
16	**SPRH**	R/W							
		Shift register high byte of SPI							
17	(Reserved)	-							
		-							
18	(Reserved)	-							

		-							
19	**PORTA**	R	R	R	R	R	R	R	R
		A.7	A.6	A.5	A.4	A.3	A.2	A.1	A.0
1A	**PORTB**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
1B	(Reserved)	-							
		-							
1C	(Reserved)	-							
		-							
1D	(Reserved)	-							
		-							
1E	(Reserved)	-							
		-							
1F	(Reserved)	-							
		-							
20	**PFS**	R/W							
		PLL frequency select							
21	**PACON**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		LVD2	LVD1	LVD0	LVDSEL	Bit7PU	/R2EN	/R1EN	KE
22	**STBCON**	-	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		-	SCAN	BitST	ALL	STB3	STB2	STB1	STB0
23	**DCRB**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		Bit7DC	Bit6DC	Bit5DC	Bit4DC	Bit3DC	Bit2DC	Bit1DC	Bit0DC
24	(Reserved)	-							
		-							
25	(Reserved)	-							
		-							
26	(Reserved)	-							
		-							
27	(Reserved)	-							
		-							
28	**LCDCON**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		BSEL2	BSEL1	BSEL0	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0
29	(Reserved)	-							
		-							
2A	(Reserved)	-							
		-							
2B	**SPICON**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
		TLS1	TLS0	BRS2	BRS1	BRS0	EDS	DORD	SE
2C	**SPISTA**	R/W	R/W	R/W	R/W	R/W	R/W	R	R
		LCDM1	LCDM0	SFR1	SFR0	SPWKEN	SMP	DCOL	RBF
2D	**PAWAKE**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		WKEN7	WKEN6	WKEN5	WKEN4	WKEN3	WKEN2	WKEN1	WKEN0
2E	**LCDARL**	R/W							
		Address low to LCD RAM							
2F	**LCDARH**	-	-	-	-	-	-	R/W	R/W
		-	-	-	-	-	-	LCDARH1	LCDARH0
30	**POST_ID**	-	R/W	R/W	R/W	-	R/W	R/W	R/W
		-	LCD_ID	FSR1_ID	FSR0_ID	-	LCDPE	FSR1PE	FSR0PE
31	**TRL0L**	R/W							
		Timer0 reload low byte							
32	**TRL0H**	R/W							
		Timer0 reload high byte							
33	**TRL1**	R/W							
		Timer1 reload register							
34	**TRCON**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

		T1WKEN	T1EN	T1PSR1	T1PSR0	T0EN	T0CS	T0PSR1	T0PSR0
35	**MTRL**	R/W Melody Timer reload register							
36	**MWTCON**	R/W T2EN	R/W T2PSR1	R/W T2PSR0	R/W WDTEN	R/W WDTPSR1	R/W WDTPSR0	R/W MTEN	R/W MDO2EN
37	**ELCON**	R/W ELTEN	R/W CKP	R/W ELTRL5 ~ ELTRL0					
38	**PAINTSTA**	R/W PA7I	R/W PA6I	R/W PA5I	R/W PA4I	R/W PA3I	R/W PA2I	R/W PA1I	R/W PA0I
39	**PAINTEN**	R/W PA7IE	R/W PA6IE	R/W PA5IE	R/W PA4IE	R/W PA3IE	R/W PA2IE	R/W PA1IE	R/W PA0IE
3A	**INTSTA**	- -	- -	- -	R/W SRBFI	R/W LVDI	R/W TMR2I	R/W TMR1I	R/W TMR0I
3B	**INTCON**	- -	- -	- -	R/W SRBFIE	R/W LVDIE	R/W TMR2IE	R/W TMR1IE	R/W TMR0IE
3C	(Reserved)	- -							
3D	(Reserved)	- -							
3E	(Reserved)	- -							
3F	**PBCON**	R/W Bit7PU	R/W Bit6PU	R/W Bit5PU	R/W Bit4PU	R/W Bit3PU	R/W Bit2PU	R/W Bit1PU	R/W Bit0PU

R0(INDF0)

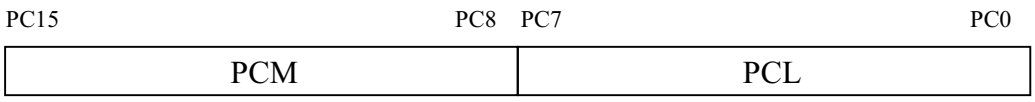
*R0 is not a physically implemented register. It is useful as indirect addressing pointer0. Any instruction using R0 as register actually accesses data pointed by the File select register0(R1) and bank select register(R5).

R1(FSR0)

*R1 is an address register for indirect addressing pointer0. User can select up to 256 bytes register on working bank(selected by BSR).

*When enable FSR0 auto increase/decrease function by R30(Post_ID), FSR0 will ***NOT*** carry into or borrow from BSR register. On the contrary, FSR1 will carry into or borrow from BSR1.

R2~R4(PCL,PCM,PCH)



*Generates up to 48K*16 on chip ROM addresses to the relative programming instruction codes.

*"S0CALL" loads the low 12 bits of the PC(4K*16 ROM).

*"SCALL","SJUMP" loads the low 13 bits of the PC(8K*16 ROM).

*"LCALL","LJUMP" loads the full 16 bits of the PC(48K*16 ROM).

*"ADD R2,A" or "ADC R2,A" allows a relative address be added to the current PC. The carry bit of R2 will automatically carry into PCM .

R5(BSR)

*Determine which bank is active(working bank) among the 64 banks.

*INDF0 is pointed on the working bank determined by R5.

R6(STKPTR)

*The stack level is bottom up(decrease) start from FFh of BANK 63.

*Stack locates on BANK 62 and 63 from address FFh~80h. And initial stack pointer is 00h.

*Bit 0~6 of STKPTR use to pointer address from 80h~FFh

*Bit 7=1 used to select BANK 63 ,Bit 7=0 used to select BANK 62.

R7(BSR1)

*R7 is a bank register for indirect addressing pointer 1(R8,R9) only. Can't determine the working bank for general register.

R8(INDF1)

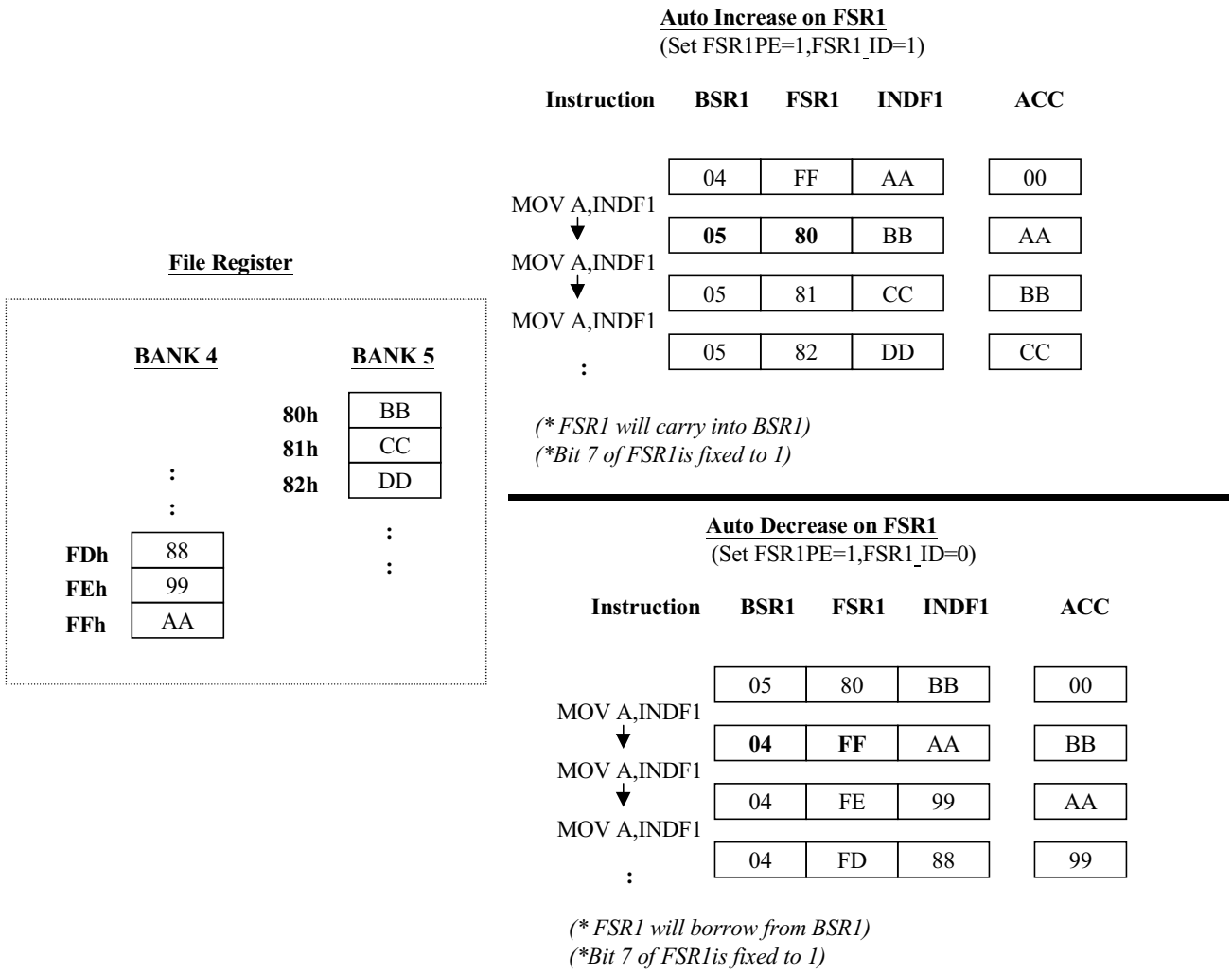
*R8 is not a physically implemented register. It is useful as indirect addressing pointer 1. Any instruction using R8 as register actually accesses data pointed by the File select Register1(R9) and bank select register1(R7).

R9(FSR1)

*R9 is an address register for INDF1 only. User can select address 0x80 to 0xFF register on the bank pointed by R7.

*Bit 7 of FSR1 is fixed to 1.

*Linear addressing ability of INDF1 shown below.



RA(ACC)

*Accumulator. Internal data transfer , or instruction operand holding.

RB~RD(TABPTRL,TABPTRM,TABPTRH)

*Internal program ROM or external memory address register.

*Bit 23 used to select internal/external memory, **Bit 22~Bit 1** used to point the address of memory, **Bit 0** used to select the low or high byte of pointed word. (See TBRD instruction).

*External memory table look up function is reserved for the future model.

RE(CPUCON)

bit 7 bit0

CLKOEN	CKS	LVDEN	/LV	/GLINTD	PS	MS1	MS0

*bit7(CLKOEN): clock output enable control bit.

CLKO pin is tri-state when clock output disable.(**CLKOEN=0)**

*bit6(CKS): clock select bit of clock output pin (CLKO).

0: CLKO pin output frequency at 32.768KHz(Fosc)

1: CLKO pin output frequency at 21.845KHz(Fosc/1.5).

*bit5(LVDEN): Enable Low Voltage Detector control bit.

*bit4(/LV): Low voltage detected. This is a read only bits. When the voltage of **LVDIN** pin is lower than Vdet(Vth-)(selected by **LVD0~LVD2** bit of R21), this bit will be clear.

0: Low voltage is detected.

1: Low voltage is not detected or LVD is disable.

*bit3(/GLINTD): Global interrupt disable bit.

0:Disable all interrupt.

1:Enable all un-mask interrupt.

*bit2(PS): PLL stable flag. This bit will be cleared when PLL not turned on or PLL is turned on but not stable. And be set after PLL turned on and frequency stable.

0: PLL is not turned on or PLL frequency not yet stable .

1: PLL is turned on and frequency stable.

*bit1(MS1): Mode select bit 1. Used to enter SLEEP MODE or IDLE MODE after executing "**SLEP**" instruction.

0: SLEEP MODE

1: IDLE MODE

*bit0(MS0): Mode select bit 0. Used to enter SLOW MODE or FAST MODE.

0: SLOW MODE.

1: FAST MODE.

RF(STATUS)

bit 7 bit0

/TO	/PD	SGE	SLE	OV	Z	DC	C

*bit7(/TO): Reset to 0 when WDT time out reset. Set to 1 by "WDTC" instruction , enter SLEEP MODE , power on reset or Reset pin low condition.

*bit6(/PD) : Reset to 0 when enter sleep mode. Set to 1 by "WDTC" instruction , power on reset or Reset pin low condition.

*bit5(SGE): Computation result great than or equal to zero(Positive value) after signed arithmetic. Only affected by HEX arithmetic instruction.

*bit4(SLE): Computation result less than or equal to zero(Negative value) after signed arithmetic. Only affected by HEX arithmetic instruction.

*bit3(OV): Overflow flag. Use in signed operation when bit6 carry into or borrow from signed bit(bit7).

*Note: 1.When OV=1 after signed arithmetic , user can check **SGE** bit and **SLE** bit to know either overflow(carry into sign bit) or underflow (borrow from sign bit) happened.*

OV=1 and SGE=1 ➔ overflow happened

OV=1 and SLE=1 ➔ underflow happened

*2. When overflow happened, user should **clear** the MSB of Accumulator to get the correct value.*

*When underflow happened, user should **set** the MSB of accumulator to get the correct value.*

Ex1. ADD positive value with positive value, and ACC signed bit was affected

```
MOV     ACC,#60h    ;signed number +60h
ADD     ACC,#70h    ;+60h ADD with +70h
```

==========

after instruction:

ACC=d0h

SGE=1, means the result is great than or equal to 0(positive value)

OV=1, means result carry into signed bit(bit 7), overflow happened.

correct the signed bit:

ACC=50h (Clear the signed bit)

The actual result= +80h* 1(OV=1) + 50h = +d0h

Ex2. SUB positive value from negative value, and ACC signed bit was affected

```
MOV     ACC,#50h    ;signed number +50h
SUB     ACC,#90h    ;+50h SUB from -70h (signed number of 90h)
```

==========

after instruction:

ACC=40h

SLE=1, means the result is less than or equal to 0(negative value)

OV=1, means result borrow from signed bit(bit 7), underflow happened.

correct the signed bit:

ACC=c0h (set the signed bit)

The actual result= -80h* 1(OV=1) - 40h(signed number of c0h) = -c0h

*bit2(Z) : Zero flag.

*bit1(DC) : Auxiliary carry flag.

*bit0(C) : Carry flag.

R10(LCDDATA)

*R10 is an indirect addressing pointer of LCD RAM.

Any instruction using R10 as register actually accesses LCD RAM pointed by

LCDARH:LCDARL(R2F:R2E).

R11(TRL2)

*Timer2 reload register.

R12,R13(PRODL,PRODH)

*An unsigned 8*8 hardware multiplier is included in the micro controller. The result is stored into the 16 bits product register (PRODH:PRODL).

R14~R16(SPRL:SPRM:SPRH)

*SPI shift buffer for 24/16/8 bits length.

R17~R18

*Reserved.

R19~R1A(PORTA~PORTB)

*Port A ~ Port B are general I/O register.

R1B~R1F

*Reserved.

R20(PFS)

*PLL frequency select.

R21(PACON)

bit 7							bit0
LVD2	LVD1	LVD0	LVDSEL	Bit7PU	/R2EN	/R1EN	KE

*bit7~5(LVD2~0): LVD detection voltage select bits.

LVD2~0	Vdet(Vth-)	Vdet(Vth+)	Deviation	LVD2~0	Vdet(Vth-)	Vdet(Vth+)	Deviation
000	2.2V	2.3V	±0.1V	100	2.6V	2.7V	±0.1V
001	2.3V	2.4V		101	2.7V	2.8V	
010	2.4V	2.5V		110	2.8V	2.9V	
011	2.5V	2.6V		111	2.9V	3.0V	

The initial value of LVD2~0 after CPU reset is "000".

*bit4(LVDSEL): Built in LVD/External LVD select

0: External LVD selected.

1: Built-in LVD selected.

*bit3(Bit7PU): Enable PortA.7 pull up resistor.

*bit2(/R2EN): Enable R2(large resistor) pull up resistor.

0: Enable R2 pull up resistor.

1: Disable R2 pull up resistor.

*bit1(/R1EN): Enable R1(small resistor) pull up resistor.

0: Enable R1 pull up resistor.

1: Disable R1 pull up resistor.

*bit0(KE): Key input enable/disable control bit.

0: Disable Key input function (PORTA register is ***NOT*** correspondence with Key input in software scan mode).

1: Enable Key input function (PORTA register is correspondence with Key input in software scan mode).

R22(STBCON)

bit 7							bit0
-	SCAN	BitST	ALL	STB3	STB2	STB1	STB0

*bit7: Reserved.

*bit6(SCAN) : Automatic key scan or specify the scan signal bit by bit(software scan).

0 : Key scan was specified as the bit **STB3~0** defined.

1 : Auto strobe scanning.

*bit5(BitST) : Enable Bit strobe

0 : Display waveform.

1 : Strobe signal as STB3~0 defined.

*bit4(ALL): Set All strobe.

0 : Bit strobe.

1 : All strobe.

*bit3~0(STB3~0): Strobe output selector bit.

R23(DCRB)

*bit7~0(Bit7DC~Bit0DC):Direction control of Port B .

0:output pin

1:input pin

R24~R27

*Reserved.

R28(LCDCON)

bit 7							bit0
BSEL2	BSEL1	BSEL0	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0

*bit7~5(BSEL2~0) : LCD Bias select

BSEL2	BSEL1	BSEL0	LCD Bias
0	0	0	1/3
0	0	1	1/3.5

0	1	0	1/4
0	1	1	1/4.5
1	0	0	1/5
1	0	1	1/5.5
1	1	0	1/6
1	1	1	1/6.5

*bit4~0(ADJ4~0): LCD contrast adjustment .

ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	α	**Contrast**
0	0	0	0	0	0	Weakest
0	0	0	0	1	1	
.	.	.	.	.	.	
.	.	.	.	.	.	
1	1	1	1	0	30	
1	1	1	1	1	31	Strongest

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV$$

$$VEV = (1 - \frac{(31 - \alpha)}{124}) \times VREF$$

(Vref=2.12V at 20°C)

R29~R2A

*Reserved.

R2B(SPICON)

bit 7 bit0

TLS1	TLS0	BRS2	BRS1	BRS0	EDS	DORD	SE

*Bit7~6(TLS1~TLS0):Shift buffer length select. Shift buffer length is programmable.

00: SPI disable

01: SPI shift buffer length = 24 bits

10: SPI shift buffer length = 16 bits

11: SPI shift buffer length = 8 bits

*bit5~3(BRS2~BRS0):Bit rate select. Programming the clock frequency/rates and sources.

000:Master,TMR0/2

001:Master,Fsystem/4.

010:Master,Fsystem/16.

011:Master,Fsystem/64.

100:Master,Fsystem/256.

101:Master,Fsystem/1024.

110:Slave,/SS enable

111:Slave,/SS disable

*bit2(EDS): Select the raising / falling edges latch by programming the EDS bit

0: Falling edge

1: Raising edge

*bit1(DORD):Data transmission order.

0:Shift left (MSB first)

1:Shift right (LSB first)

*bit0(SE): Shift Enable.

Set to 1 automatically when write data into SPRL register and begin to shift.

Reset to 0 when transfer buffer empty detected.

R2C(SPISTA)

bit 7 bit0

LCDM1	LCDM0	SFR1	SFR0	SPWKEN	SMP	DCOL	RBF

*bit7~6(LCDM1~0): LCD operation mode control register.

LCDM1:LCDM0	Operation mode
00	Disable(LCD off)
01	Blanking
10	LCD enable
11	LCD enable

Note: Blanking means All COM & SEG pin are tied to ground.

*bit5~4(SFR1~0) : Frame frequency adjustment.

SFR1	SFR0	CL frequency	Frame frequency (Hz)		
			Min	Typ	Max
0	0	Fosc /13	59.1	78.8	98.6
0	1	Fosc / 14	54.9	73.2	91.5
1	0	Fosc / 15	51.3	68.3	85.4
1	1	Fosc / 16	48.0	64.1	80.1

Note: 1.Fosc = 32.8kHz +/- 25% (all conditions)

2.This table is based on 1/32 duty.

*bit3(SPWKEN):SPI wake up enable control bit.

0:Disable SPI (slave mode) read buffer full wakeup.

1: Enable SPI (slave mode) read buffer full wakeup.

*bit2(SMP):SPI data input sample phase.

0:Input data sampled at middle of data output time

1:Input data sampled at the end of data output time

In slave mode, data input sample is fixed at middle of data output time.

*bit1(DCOL):SPI data collision.

0:Data collision didn't occurs

1:Data collision occurs. Should be cleared by software.

*bit0(RBF):Set to 1 by Buffer Full Detector, and clear to 0 automatically when read data from SPRL register.

R2D(PAWAKE)

bit 7 bit0

WKEN7	WKEN6	WKEN5	WKEN4	WKEN3	WKEN2	WKEN1	WKEN0

*bit7~0(WKEN7~WKEN0): Wake up enable control bit of Port A.

0: Disable Port A wake up function.

1: Enable Port A wake up function.

R2E~R2F(LCDARL,LCDARH)

* LCDARH:LCDARL is the address for LCD RAM.

*LCDARH: Page address for LCD RAM.

*LCDARL: Column address for LCD RAM.

R30(POST_ID)

bit 7							bit0
-	LCD_ID	FSR1_ID	FSR0_ID	-	LCDPE	FSR1PE	FSR0PE

*Post increase / decrease control register.

*For example , enable LCD post decrease function(bit2=1[enable],bit6=0[decrease]), then LCDARL will automatic decrease after access(read or write) LCDDATA(R10). (Note: LCDARL will NOT carry into /borrow from LCDARH.)

*bit 0(FSR0PE): Enable FSR0 post increase/decrease function.

*bit 1(FSR1PE): Enable FSR1 post increase/decrease function.

*bit 2(LCDPE): Enable LCDARL post increase/decrease function.

*bit 3: Reserved.

*bit 4(FSR0_ID): Set to 1 means auto_increase, reset to 0 means auto_decrease of FSR0.

*bit 5(FSR1_ID): Set to 1 means auto_increase, reset to 0 means auto_decrease of FSR1.

*bit 6(LCD_ID): Set to 1 means auto_increase, reset to 0 means auto_decrease of LCDARL.

*bit7: Reserved.

*The initial value of bit0~bit3 is 0, and bit 4~bit 7 is 1.

R31~R32(TRL0L~TRL0H)

*Timer0 reload low byte and high byte.

R33(TRL1)

*Timer1 reload register.

R34(TRCON)

bit 7							bit0
T1WKEN	T1EN	T1PSR1	T1PSR0	T0EN	T0CS	T0PSR1	T0PSR0

*Timer0 and timer1 control register.

*bit7(T1WKEN): Enable bit of Timer1 underflow wake up function in IDLE MODE.

0: Disable Timer1 wake up function .

1: Enable Timer1 wake up function.

*bit6(T1EN): Timer1 enable control bit

0: Disable Timer1(stop counting) .

1: Enable Timer1 .

*bit5~4(T1PSR1~T1PSR0): Timer1 Prescaler select bits.

T1PSR1:T1PSR0	Prescale value
00	1:4
01	1:16
10	1:64
11	1:256

*bit3(T0EN): Timer0 enable control bit

0: Disable Timer0(stop counting) .

1: Enable Timer0 .

*bit2(T0CS): Timer 0 clock source select bit.

0: Clock source is from Fosc.

1: Clock source is from half of the system clock.

*bit1~0(T0PSR1:T0PSR0): Timer0 Prescaler select bits.

T0PSR1:T0PSR0	Prescale value
00	1:1
01	1:4
10	1:16
11	1:64

R35(MTRL)

*Melody Timer reload register.

R36(MWTCON)

bit 7							bit0
T2EN	T2PSR1	T2PSR0	WDTEN	WDTPSR1	WDTPSR0	MTEN	MDO2EN

*Timer2 ,Melody timer and WDT control register.

*bit7(T2EN): Timer2 enable control bit

0: Disable Timer2(stop counting) .

1: Enable Timer2 .

*bit6~5(T2PSR1~T2PSR0): Timer2 Prescaler select bits.

T2PSR1:T2PSR0	Prescale value
00	1:1
01	1:2
10	1:4
11	1:8

*bit4(WDTEN): Watch Dog Timer enable bit

*bit3~2(WDTPSR1~WDTPSR0): Watch Dog timer Prescaler select bits.

WDTPSR1:WDTPSR0	Prescale value
00	1:4
01	1:16
10	1:64
11	1:128

*bit1(MTEN): Melody Timer enable control bit.

*bit0(MDO2EN): Melody negative output port enable control bit.

R37(ELCON)

bit 7							bit0
ELTEN	CKP	ELTRL5 ~ ELTRL0					

*bit7(ELTEN): EL Timer enable control bit.

0: Disable EL Timer(stop counting) and recover CK and CHOP pin to general I/O pin.

1: Enable EL Timer and change Port B.4 and Port B.5 to CK and CHOP output pin.

*bit6(CKP): EL clock polarity select bit.

0: Idle state for CHOP pin is low level.

1: Idle state for CHOP pin is high level.

*bit5~0(ELTRL5~0): Used to store the auto reload value of EL timer. When underflow happens, ELTRL will automatic reload into 6 bits counter .

R38(PAINTSTA)

bit 7							bit0
PA7I	PA6I	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I

*bit7~0(PA7I~PA0I): INT status of Port A interrupt. Set when pin **falling edge** detected. Clear by software.

R39(PAINTEN)

bit 7							bit0
PA7IE	PA6IE	PA5IE	PA4IE	PA3IE	PA2IE	PA1IE	PA0IE

*Port A interrupt enable control register

*bit7~0(PA7IE~PA0IE): Control bit of interrupt.

0: Disable Port A interrupt function.

1: Enable Port A interrupt function.

R3A(INTSTA)

bit 7							bit0
-	-	-	SRBFI	LVDI	TMR2I	TMR1I	TMR0I

*bit0(TMR0I): Set to 1 when TMR0 underflow happened. Clear to 0 by software or Timer0 disable.

*bit1(TMR1I): Set to 1 when TMR1 underflow happened. Clear to 0 by software or Timer1 disable.

*bit2(TMR2I): Set to 1 when TMR2 underflow happened. Clear to 0 by software or Timer2 disable.

*bit3(LVDI): Set to 1 when LVD low level detected(**Falling edge**). Clear to 0 by software or LVD disable.

*bit4(SRBFI): Set to 1 when SPI read buffer full happened. Clear to 0 by software or SPI disable.

*bit5~7: Reserved.

R3B(INTCON)

bit 7							bit0
-	-	-	SRBFIE	LVDIE	TMR2IE	TMR1IE	TMR0IE

* 0: Disable Port A interrupt function.
1: Enable Port A interrupt function.

*bit0(TMR0IE): Control bit of TIMER0 interrupt.

*bit1(TMR1IE): Control bit of TIMER1 interrupt.

*bit2(TMR2IE): Control bit of TIMER2 interrupt.

*bit3(LVDIE): Control bit of LVD interrupt.

*bit4(SRBFIE): Control bit of SPI read buffer full interrupt.

*bit5~7: Reserved.

R3C~R3E

*Reserved.

R3F(PBCON)

*bit7~0(Bit7PU~Bit0PU):Pull up resistor control of Port B.

0:Disable pull up resistor

1:Enable pull up resistor

Code Option

(Locate on the final 4 words of Program ROM)

WORD0 (0xBFFC):

bit 7							bit0
EXTVH	TBRD_3T	DRSEL1	DRSEL0	-	ELSEL	IM	OSCSEL

*bit0 (OSCSEL): RC oscillator or Crystal select bit

0:RC oscillator

1:Crystal oscillator

*bit1 (IM): Initial mode after Reset.

0: SLOW Mode

1: FAST Mode

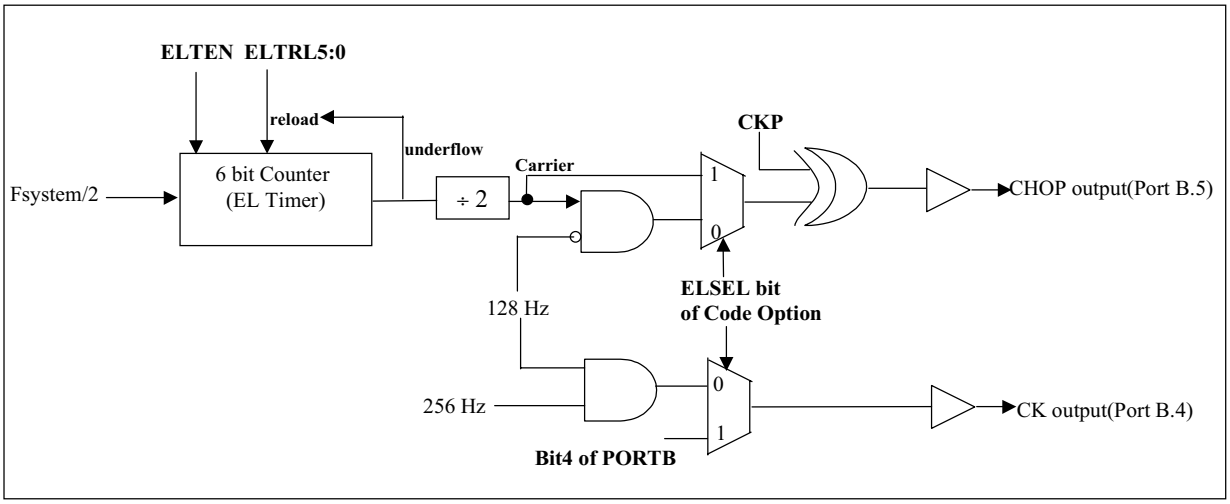
*bit2(ELSEL): EL output timing select bit

0: CHOP output is from carrier gating with 128Hz and CKP .

CK output is from 128Hz gating with 256Hz.

1: CHOP output is directly from carrier .

CK output is directly from Bit4 of PORTB register.



*bit3: No use.

*bit4~bit5(DRSEL1:0): LCD duty ratio select bit.

00: 1/ 11 duty

01: 1/ 16 duty

10: 1/ 24 duty

11: 1/ 32 duty

CL Frequency V.S. Duty ratio table:

		CL frequency			
SFR1	SFR0	1/11 duty	1/16 duty	1/24 duty	1/32 duty
0	0	Fosc /38	Fosc /26	Fosc /17	Fosc /13
0	1	Fosc / 40	Fosc / 28	Fosc / 18	Fosc / 14
1	0	Fosc / 44	Fosc / 30	Fosc / 20	Fosc / 15
1	1	Fosc / 46	Fosc / 32	Fosc / 22	Fosc / 16

*bit6(TBRD_3T): TBRD instruction three cycle enable bit.

0: ”TBRD” is 2 cycles instruction.

1: ”TBRD” is 3 cycles instruction. (for use at large DATA ROM version)

*bit7(EXTVH): Vout is from external power source or internal charge pump selection.

0: Internal.

1: External

bit 15 bit8

OPV4_1	OPV4_0	OPV3_1	OPV3_0	OPV2_1	OPV2_0	OPV1_1	OPV1_0

*bit8~bit9(OPV1_0:1):V1 OP buffer type selection

*bit10~bit11(OPV2_0:1):V2 OP buffer type selection

*bit12~bit13(OPV3_0:1):V3 OP buffer type selection

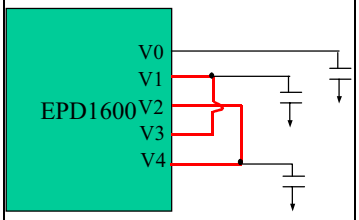
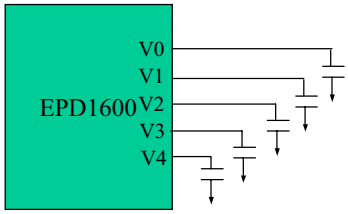
*bit14~bit15(OPV4_0:1):V4 OP buffer type selection

(OPVx_1,OPVx_0) OP Buffer	00	01	10	11
V1	Source	*1	Class A/B	OFF
V2	Sink	*1	Class A/B	OFF
V3	Source	*1	Class A/B	OFF
V4	Sink	*1	Class A/B	OFF

*1: When Normal display: V1=source, V2=sink, V3=source, V4=sink

When Auto key scan: Every time when 30us strobe start, OP Amp. will change to class A/B for 60us, then return to Normal Display.

Note: OP buffer type configuration for different application

Application OP Buffer	1/3 Bias & Small panel	Other Bias & Small panel	Other Bias & Large panel
V1	*1	*1	Class A/B
V2	Off	*1	Class A/B
V3	Off	*1	Class A/B
V4	*1	*1	Class A/B
Circuit			
Current Consumption	Very low	Low	High, but high driving ability

WORD1 (0xBFFD):

bit 7							bit0
-	-	CSOP	PLLST_OPT	HFSEL	OPT1	OPT0	-

*bit0:Reserved.

*bit1(OPT0):Reserved.

*bit2(OPT1):Reserved.

*bit3(HFSEL): High frequency select bit. ***This function is only available in ROMless CPU.***

0: High frequency system clock is from PLL clock.

1: High frequency system clock is from HOSCO pin.

*bit4(PLLST_OPT):PLL stable accuracy select bit.

0: PS bit will be set when PLL frequency is within target +/- 10%.

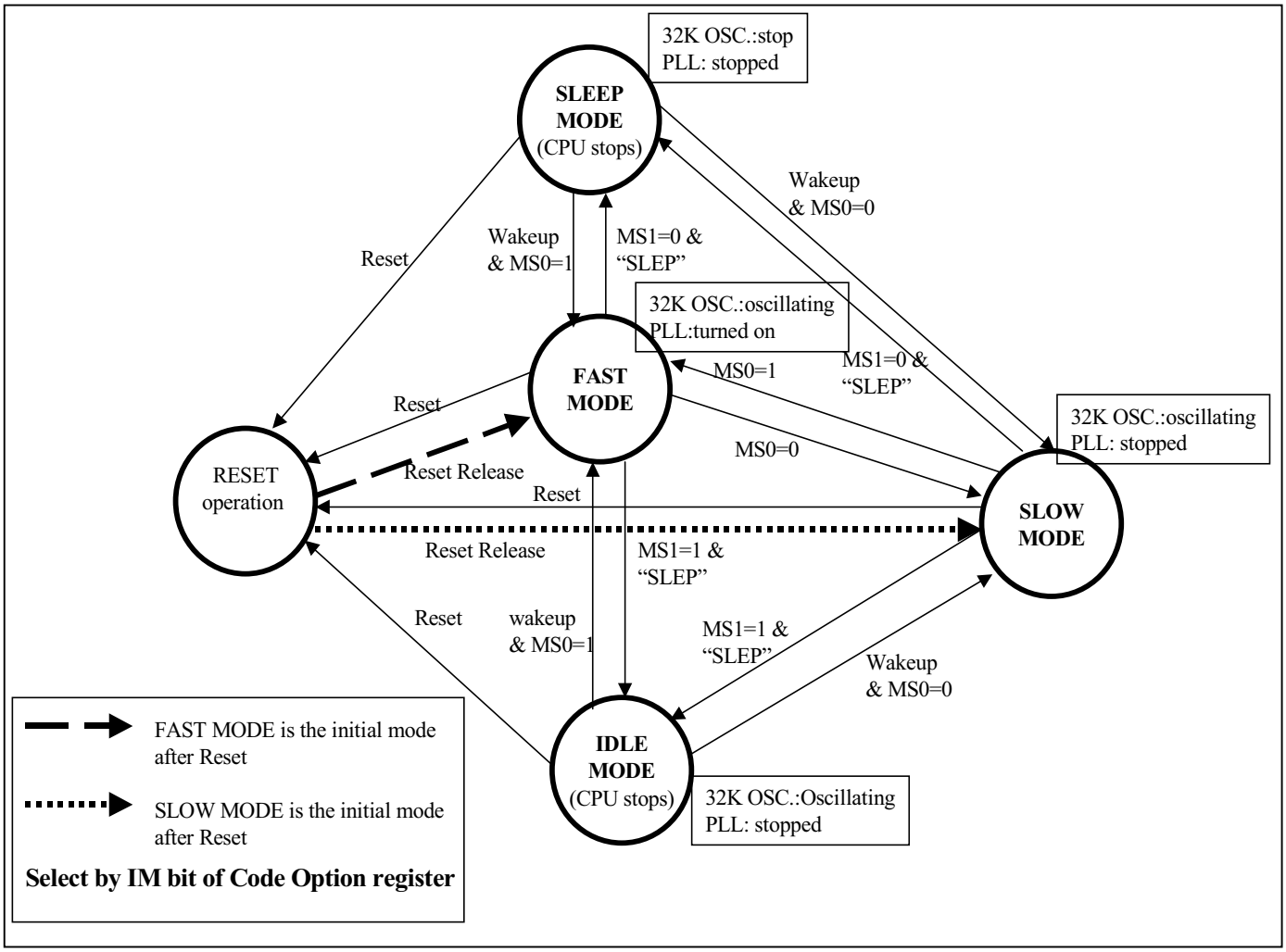
1: PS bit will be set when PLL frequency is within target +/- 3%.

*bit5(CSOP):Reserved.

*Bit6~15: Not use.

WORD2~WORD3 (0xBFFE~0xBFFF): Not use.

(2) CPU OPERATION MODE:



Mode / Device	SLEEP	IDLE	SLOW	FAST
Osc.(32768Hz)	X	O	O	O
PLL	X	X	X	O
CPU	X	X	O	O
LVD	O	O	O	O
CLOCK OUTPUT	X	O	O	O
Timer0,1,2, Melody Timer, EL Timer	X	O	O	O
INT	X(*2)	X(*2)	O	O
SPI	O(slave)	O(slave)	O	O
I/O wake up	O	O	X	X
SPI wake up	O	O	X	X
Timer1 wake up	X	O	X	X

(Note): *1: O: Function available if enable.

X: Function NOT available.

*2: Interrupt flag will be recorded but not be executed until CPU wake up.

Function Description:

1. SLEEP MODE: When set **MS1** bit of CPUCON register to '0' and execute "**SLEP"** instruction, the CPU will enter SLEEP MODE.

The SLEEP MODE suspends all system operation and holds the internal status immediately before the suspension with low power consumption. This mode will be released by CPU reset , I/O pins or SPI receive full wake up.

The **/PD** bit of STATUS Register(RFh) is cleared when entering SLEEP MODE. This bit will be set to 1 by "WDTC" instruction , Power on RESET or Reset pin low condition.

All register and LCD RAM unchanged in SLEEP MODE.

2.IDLE MODE: When set **MS1** bit of CPUCON register to '1' and execute "**SLEP"** instruction, the CPU will enter IDLE MODE.

The IDLE MODE suspends all operations except for the Oscillator , clock output . It retains the internal status with low power consumption without stopping the clock function.

The IDLE MODE will be waken up and return to the either SLOW MODE(**MS0**=0) or FAST MODE(**MS0**=1) by the timer 1 wake up ,SPI receive full or I/O pins wake up (if enable) .

All register and LCD RAM unchanged in IDLE MODE.

3.SLOW MODE: When set **MS0** bit of CPUCON register to '0' , the CPU will enter SLOW MODE. Except PLL and UART, every device can be turned on. System clock is at 32.768KHz. This feature allows all the internal operations to slow down and thus reduces power consumption.

4.FAST MODE: When set **MS0** bit of CPUCON register to '1' , the CPU will enter FAST MODE. After turning on PLL and wait 32 clocks from Oscillator, then system clock switched to high frequency of PLL(adjustable by PFS register).

This mode allows all the internal operations at fast speed. But it will consumes the most power .

Register Description:

- **CPUCON Register:**

bit 7 bit0

CLKOEN	CKS	LVDEN	/LV	/GLINTD	PS	**MS1**	**MS0**

- **MS0**: Mode select bit 0. Used to enter SLOW MODE or FAST MODE.
  0: SLOW MODE.
  1: FAST MODE.
- **MS1:** Mode select bit 1. Used to enter SLEEP MODE or IDLE MODE after executing "**SLEP**" instruction.
  0: SLEEP MODE
  1: IDLE MODE

(3) Reset and WAKE UP:

RESET:

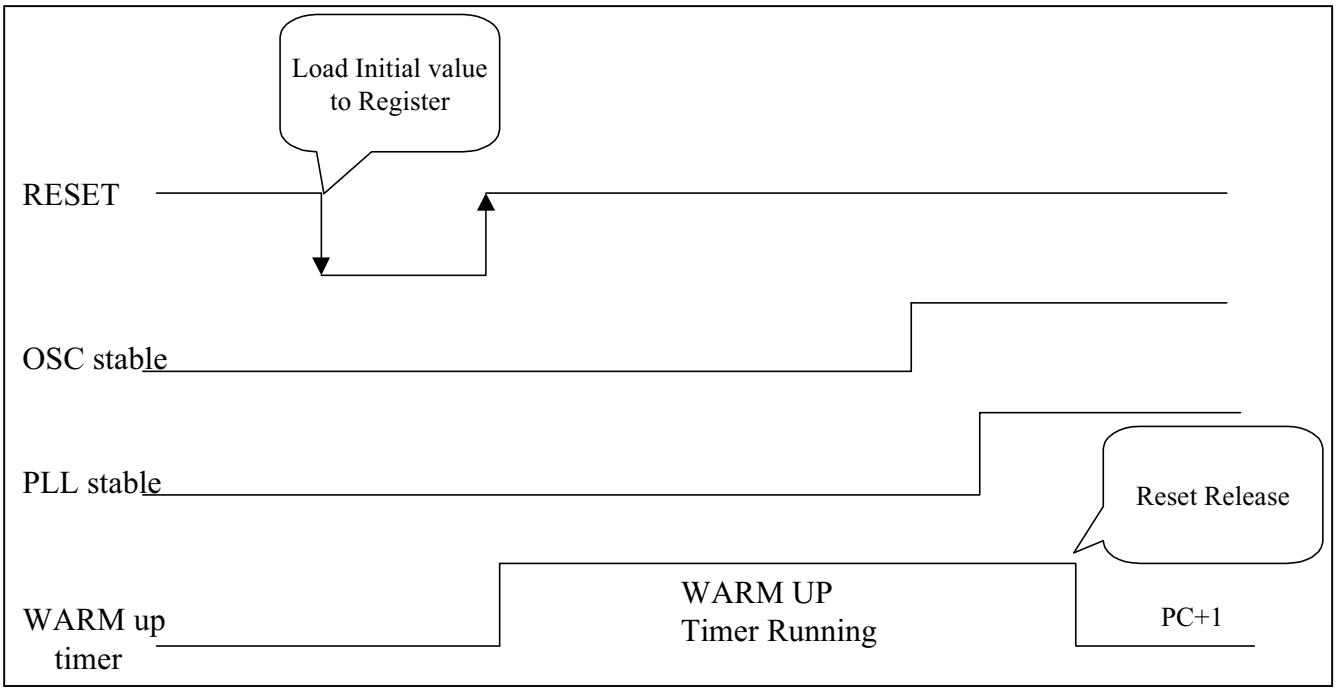
The reset can be caused by :

1. Power on reset.
2. Reset pin(SYSTEM RESET or Reset_key) is at low condition(level hold)
3. WDT time out(if WDT enable)

If the CPU reset is caused by WDT time out, the **/TO** bit of STATUS register will be cleared. Set to 1 during power up or by "WDTC" instruction or when entering SLEEP MODE.

If the CPU changed to SLEEP MODE, the **/PD** bit of STATUS register will be cleared. Set to 1 during power up or by "WDTC" instruction .

Once the RESET occurs, special function register will be reset to initial value except the **/TO, /PD** bit of STATUS register .



EVENT	/TO	/PD	REMARK
WDT time out reset from SLEEP MODE	0	0	
WDT time out reset (not SLEEP MODE)	0	1	
Wake up from SLEEP MODE by SPI or Input port	1	0	
Power up or RESET pin low condition	1	1	

Initialization after RESET occurs:

- The oscillator is running, or will be started.
- The Watchdog timer is cleared.

- If power on reset or RESET pin low condition, the **/TO** bit and **/PD** bit of RF(STATUS) are set to "1". If WDT time out reset, the **/TO** bit is cleared.
- The program counter(PCH:PCM:PCL) is clear to all "0".
- The other register initial value is as following.

Special Register:

Addr.	NAME	Initial value	Addr.	NAME	Initial value
00h	**INDF0**	---- ----(*1)	10h	**LCDDATA**	---- ----(*1)
01h	**FSR0**	0000 0000	11h	**TRL2**	uuuu uuuu
02h	**PCL**	0000 0000	12h	**PRODL**	uuuu uuuu
03h	**PCM**	0000 0000	13h	**PRODH**	uuuu uuuu
04h	**PCH**	---- ----	14h	**SPRL**	xxxx xxxx
05h	**BSR**	0000 0000	15h	**SPRM**	xxxx xxxx
06h	**STKPTR**	0000 0000	16h	**SPRH**	xxxx xxxx
07h	**BSR1**	0000 0000	17h	(reserved)	---- ----
08h	**INDF1**	---- ----(*1)	18h	(reserved)	---- ----
09h	**FSR1**	1000 0000	19h	**PORTA**	xxxx xxxx
0Ah	**ACC**	xxxx xxxx	1Ah	**PORTB**	xxxx xxxx
0Bh	**TABPTRL**	0000 0000	1Bh	(reserved)	---- ----
0Ch	**TABPTRM**	0000 0000	1Ch	(reserved)	---- ----
0Dh	**TABPTRH**	0000 0000	1Dh	(reserved)	---- ----
0Eh	**CPUCON**	000x 0x0c(*2)	1Eh	(reserved)	---- ----
0Fh	**STATUS**	cuxx xxxx (*3)	1Fh	(reserved)	---- ----

Control Register:

Addr.	NAME	Initial value	Addr.	NAME	Initial value
20h	**PFS**	0010 0000	30h	**POST_ID**	-111 -000
21h	**PACON**	0000 0110	31h	**TRL0L**	uuuu uuuu
22h	**STBCON**	-000 0000	32h	**TRL0H**	uuuu uuuu
23h	**DCRB**	1111 1111	33h	**TRL1**	uuuu uuuu
24h	(reserved)	---- ----	34h	**TRCON**	0000 0000
25h	(reserved)	---- ----	35h	**MTRL**	uuuu uuuu
26h	(reserved)	---- ----	36h	**MWTCON**	0000 0000
27h	(reserved)	---- ----	37h	**ELCON**	00uu uuuu
28h	**LCDCON**	0000 0000	38h	**PAINTSTA**	0000 0000
29h	(reserved)	---- ----	39h	**PAINTEN**	0000 0000
2Ah	(reserved)	---- ----	3Ah	**INTSTA**	---0 0000
2Bh	**SPICON**	0000 0000	3Bh	**INTCON**	---0 0000
2Ch	**SPISTA**	0000 0000	3Ch	(reserved)	---- ----
2Dh	**PAWAKE**	0000 0000	3Dh	(reserved)	---- ----
2Eh	**LCDARL**	0000 0000	3Eh	(reserved)	---- ----
2Fh	**LCDARH**	0000 0000	3Fh	**PBCON**	0000 0000

Legend: **x**=unknown , **-**= unimplemented read as "0", **u** = unchanged, **c** = value depends on condition

Note:

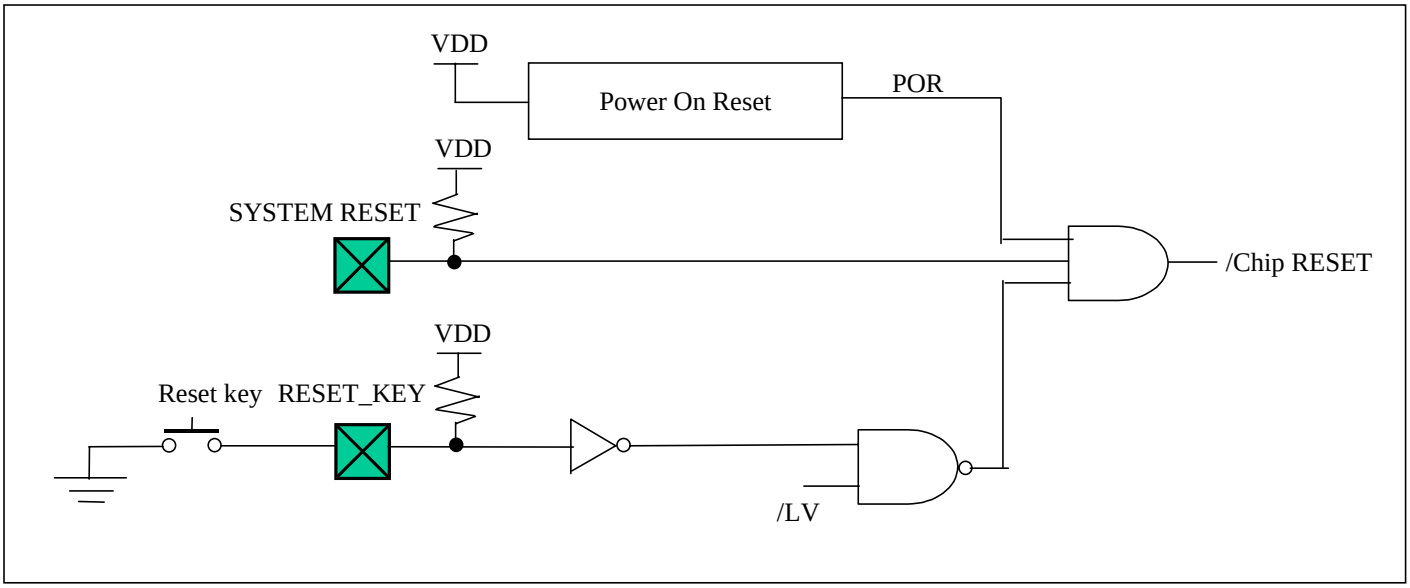
(*1)Not a physical register

(*2)Bit0(MS0) of RE(CPUCON) is reload from "**IM**" bit of code option when CPU reset..

(*3) If power on reset or RESET pin low condition, the **/TO** bit and **/PD** bit of RF(STATUS) are set to "1".

If WDT time out reset, the **/TO** bit is cleared and **/PD** bit unchanged.

Block Diagram of On-chip RESET circuit:



WAKE UP:

When SLEEP MODE , oscillator was off . CPU will be awaken by input port or SPI receive full then return to FAST MODE or SLOW MODE (determine by **MS0** bit of CPUCON register).

And when IDLE MODE, oscillator keeps running. CPU will be awaken by Timer1 , input port or SPI receive full then return to FAST MODE or SLOW MODE (determine by **MS0** bit of CPUCON register).

The **T1WKEN** bit of TRCON register can enable/disable Timer1 wake up function. The input port wake up function is enable/disable by PAWAKE register. And SPI wake function is enable/disable by **SPWKEN** bit of SPISTA register.

Register Description:

- **TRCON(Timer0 & Timer1 control register)**

bit 7 bit0

T1WKEN	T1EN	T1PSR1	T1PSR0	T0EN	T0CS	T0PSR1	T0PSR0

◆ **T1WKEN:** Enable bit of Timer1 underflow wake up function in IDLE MODE.
0: Disable Timer1 wake up function .
1: Enable Timer1 wake up function.

- **PAWAKE (Port A WAKE UP Control Register)**

bit 7 bit0

WKEN7	**WKEN6**	**WKEN5**	**WKEN4**	**WKEN3**	**WKEN2**	**WKEN1**	**WKEN0**

◆ **WKEN7~WKEN0**: Wake up enable control bit of Port A.
0: Disable Port A wake up function.
1: Enable Port A wake up function.

- **SPISTA(SPI status register):**

bit 7 bit0

LCDM1	LCDM0	SFR1	SFR0	**SPWKEN**	SMP	DCOL	RBF

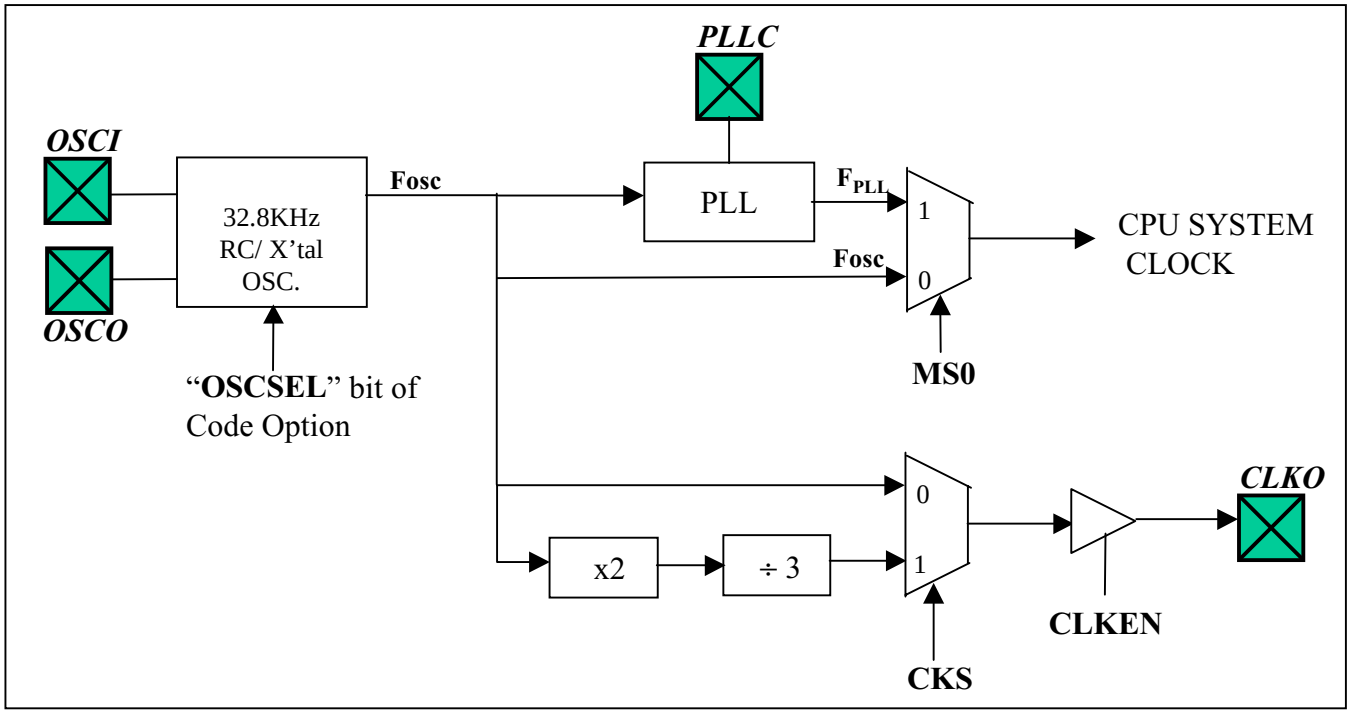
◆ **SPWKEN:** SPI wake up enable control bit.
0:Disable SPI (slave mode) read buffer full wakeup.
1: Enable SPI (slave mode) read buffer full wakeup.

(4) Oscillator System:

Feature:

- 32.8KHz RC OSC(Ext. R and Int. C) or 32768Hz Crystal.
- Built-in PLL, high frequency range can be selected from 262KHz to 10MHz by changing PFS register.
- Clock output with frequency selectable in IDLE MODE, SLOW MODE and FAST MODE.
- Operating voltage from VDD=2.2V~3.6V

Function Block Diagram:



Pin Description:

- **OSCI:** Input pin for 32.768KHz crystal oscillator or external Resistor- internal Capacitor 32.8KHz oscillator. Selected by Code Option.
- **OSCO:** Output pin for 32.768KHz crystal oscillator. If R-C oscillator is selected, this pin should be floating.

- **CLKO:** Clock output pin for external device(LCD Driver or slave CPU ,etc.). **This pin is tri-state when clock output disable.(CLKOEN=0)**
- **PLLC:** Phase lock loop capacitor, connect a capacitor with AVSS.

Register Description:

- **PFS:** PLL frequency select register. System clock can be fine tuned from 262KHz to 10MHz. The initial value of PFS register after RESET will be set to "20h" (F_{PLL}=2.097 MHz)

$$F_{PLL} = 2 * PFS * Fosc$$

PFS reg.	F_{PLL}(MHz)	PFS reg.	F_{PLL}(MHz)
0~3	*N.A.(*1)*	92	6.029
4	0.262	107	7.012
15	0.983	122	7.995
31	2.032	137	8.978
46	3.015	*150*	*9.83 (*3)*
61	3.998	153	10.027
76	4.981	255	16.712

Note: 1. PFS=0 ~ 3 is not available.
2. The Maximum range of PLL is from 262.144 K ~ 16.712 MHz
3. When enable UART, system clock should be 9.83MHz
4. The table is base on 32.768KHz oscillator frequency.

- **CPUCON Register:**

bit 7 bit0

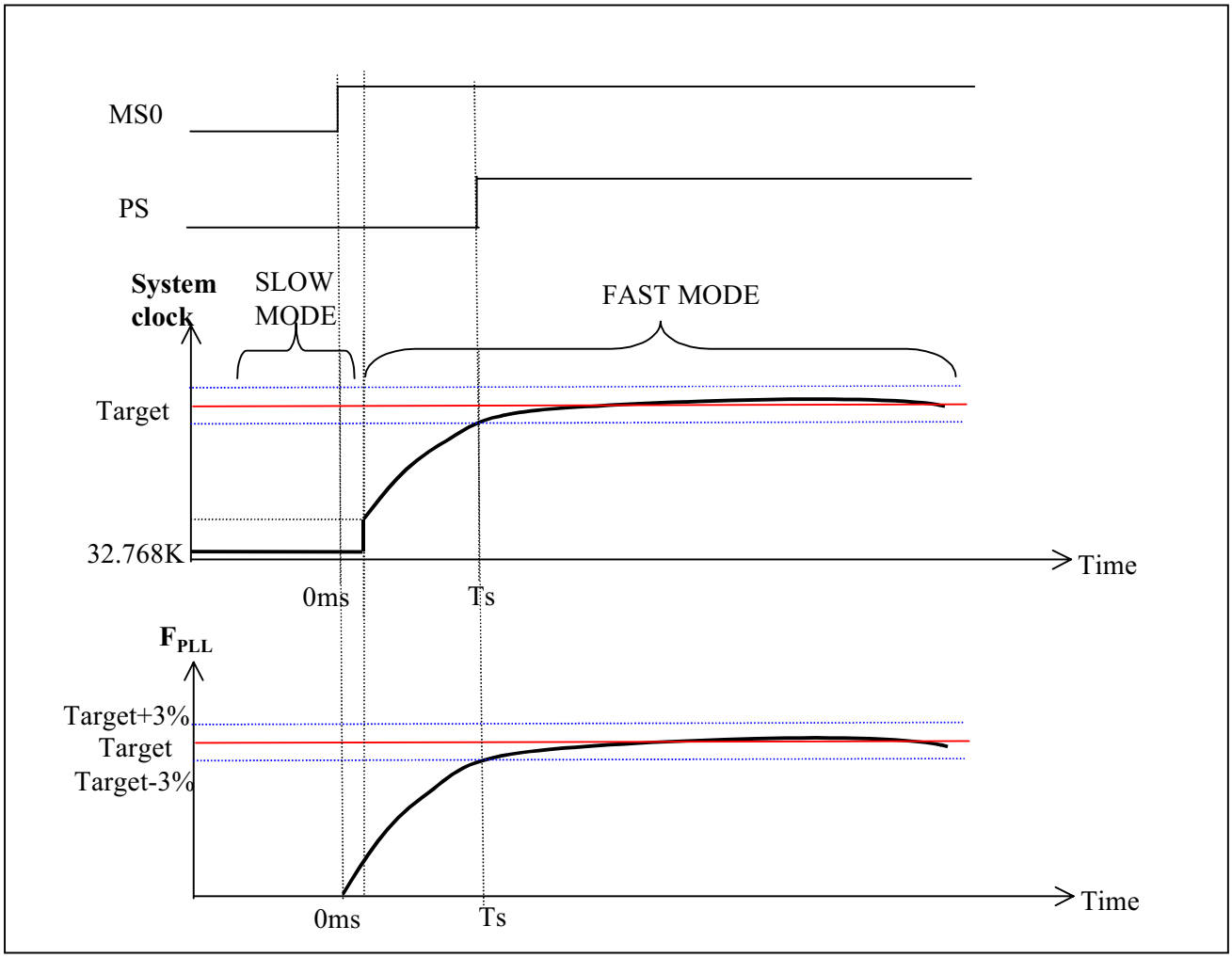
CLKOEN	CKS	LVDEN	/LV	/GLINTD	PS	MS1	MS0

◆ **CLKOEN**: Clock output enable control bit.
CLKO pin is tri-state when clock output disable.(**CLKOEN=0**)

◆ **CKS:** clock select bit of clock output pin (**CLKO**).
0: CLKO pin output frequency at 32.768KHz(Fosc)
1: CLKO pin output frequency at 21.845KHz(Fosc/1.5).

◆ **PS**: PLL stable flag. This bit will be cleared when PLL not turned on or PLL is turned on but not stable. And be set after PLL turned on and frequency stable.
PLL stable means actual frequency within target frequency +/- 3%.
0: PLL is not turned on or PLL frequency not yet stable .
1: PLL is turned on and frequency stable.

Timing Diagram:



Note: 1.Slow mode switch to Fast mode at Time=0ms
2.System clock will switch to F_{PLL} immediately,and system clock will be hundreds KHz then.
3. When PLLST_OPT code option =0, PLL frequency will be stable (+/-10%) less than 5ms.
And PLLST_OPT code option =1, PLL frequency will be stable (+/-3%) around 2 to 9ms.

(5) INTERRUPT:

There are 3 types of interrupt for the whole operation:

Level 1: Input port (Port A)interrupt .

Level 2: Timer interrupt. Include of Timer0(**TMR0I**), Timer1(**TMR1I**), Timer2 (**TMR2I**) interrupt.

Level 3: Peripheral interrupt. Include of Low voltage detected (**LVDI**), SPI read buffer full (**SRBFI**) .

The **/GLINTD** bit of CPUCON register disable all interrupts, include of LEVEL 1~LEVEL 3. Set this bit to 1 can enable all un-mask interrupt.

Interrupt vector :

Interrupt level	Interrupt source	Start address	Remark
	RESET	0x00000	
Level 1	Input Port	0x00002	PAINT
Level 2	Timer	0x00004	Timer0,Timer1,Timer2
Level 3	Peripheral	0x00006	SRBFI, LVDI

Register Description:

- **CPUCON(CPU control register)**

bit 7 bit0

CLKOEN	CKS	LVDEN	/LV	**/GLINTD**	PS	MS1	MS0

- **/GLINTD:** Global interrupt disable bit.
  0:Disable all interrupt.
  1:Enable all un-mask interrupt.

- **PAINTEN (Port A INTERRUPT Enable Control Register)**

bit 7 bit0

PA7IE	**PA6IE**	**PA5IE**	**PA4IE**	**PA3IE**	**PA2IE**	**PA1IE**	**PA0IE**

- **PA7IE~PA0IE**: Control bit of port A interrupt .
  0: Disable interrupt function.
  1: Enable interrupt function.

- **PAINTSTA (Port A INTERRUPT STATUS Register)**

bit 7 bit0

PA7I	**PA6I**	**PA5I**	**PA4I**	**PA3I**	**PA2I**	**PA1I**	**PA0I**

- **PA7I~PA0I**: INT status of Port A interrupt. Set to 1 when pin **falling edge** detected. Clear to 0 by software.

- **INTCON (INT Control Register)**

bit 7 bit0

-	-	-	SRBFIE	LVDIE	TMR2IE	TMR1IE	TMR0IE

0: Disable interrupt function.

1: Enable interrupt function.

- **TMR0IE**: Control bit of TIMER0 interrupt.
- **TMR1IE**: Control bit of TIMER1 interrupt.
- **TMR2IE**: Control bit of TIMER2 interrupt.
- **LVDIE**: Control bit of LVD interrupt.
- **SRBFIE**: Control bit of SPI read buffer full interrupt

- **INTSTA (INT STATUS Register)**

bit 7 bit0

-	-	-	SRBFI	LVDI	TMR2I	TMR1I	TMR0I

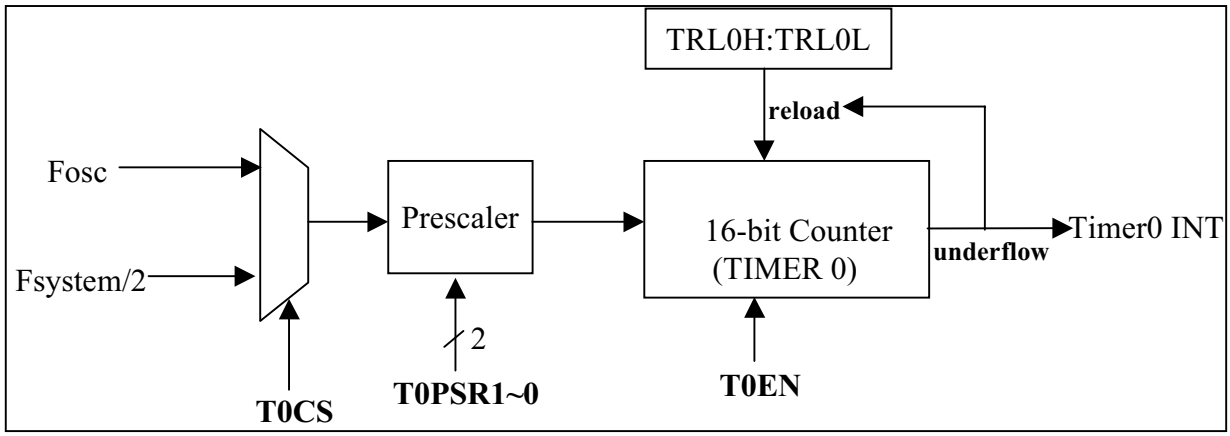
- **TMR0I**: Set to 1 when TMR0 underflow happened. Clear to 0 by software or Timer0 disable.
- **TMR1I**: Set to 1 when TMR1 underflow happened. Clear to 0 by software or Timer1 disable.
- **TMR2I**: Set to 1 when TMR2 underflow happened. Clear to 0 by software or Timer2 disable.
- **LVDI**: Set to 1 when LVD low level detected(**Falling edge**). Clear to 0 by software or LVD disable.
- **SRBFI**: Set to 1 when SPI read buffer full interrupt happened. Clear to 0 by software or SPI disable.

(6) PERIPHERAL :

A. Timer/Melody Timer/EL Timer/Watchdog Timer

1. Timer0(16 bits):

Function Block Diagram:



Function Description:

Timer0 is a general purpose 16 bits down counter for some applications required time counting. There is an interrupt available for user's application. The clock source is selectable from the oscillator clock or half of the system clock.

There is a prescaler for the timer. The **T0PSR1~T0PSR0** bit of TRCON register determine the prescale ratio and generate different clock rate as the clock source for the timer.

Counter value will be decreased by one(count down) according to the timer clock source. When underflow happens, the timer interrupt will be triggered if the global interrupt and timer0 interrupt are both enabled. At the same time,TRL0H:TRL0L will automatic reload into 16 bits counter .

The Timer0 frequency range is from 1/128 Hz(clock source is from Fosc, TRL0H:TRL0L=FFFFh, prescaler=1:64) to 5MHz(clock source is from Fsystem/2, system clock=10MHz, TRL0H:TRL0L=0h, prescaler=1:1).

$$T = \frac{1}{Freq.} * Prescale * (TRL0H:TRL0L+1)$$

Register Description:

- **TRL0H:TRL0L(Timer 0 reload register):**
  Used to store the auto reload value of TIMER0. When enabling Timer0 or underflow happens, TRL0H:TRL0L register will automatically reload into 16 bits counter .

- **TRCON(Timer0 & Timer1 control register)**

bit 7 bit0

T1WKEN	T1EN	T1PSR1	T1PSR0	**T0EN**	**T0CS**	**T0PSR1**	**T0PSR0**

◆ **T0PSR1~T0PSR0**: Timer0 Prescaler select bits.

T0PSR1:T0PSR0	Prescale value
00	1:1
01	1:4
10	1:16
11	1:64

◆ **T0CS:** Timer 0 clock source select bit.
0: Clock source is from Fosc.
1: Clock source is from half of the system clock.

◆ **T0EN:** Timer0 enable control bit
0: Disable Timer0(stop counting) .
1: Enable Timer0 .

- **INTCON (INT Control Register)**

bit 7 bit0

-	-	-	SRBFIE	LVDIE	TMR2IE	TMR1IE	**TMR0IE**

◆ **TMR0IE**: Control bit of TIMER0 interrupt.
0: Disable interrupt function.
1: Enable interrupt function.

- **INTSTA (INT STATUS Register)**

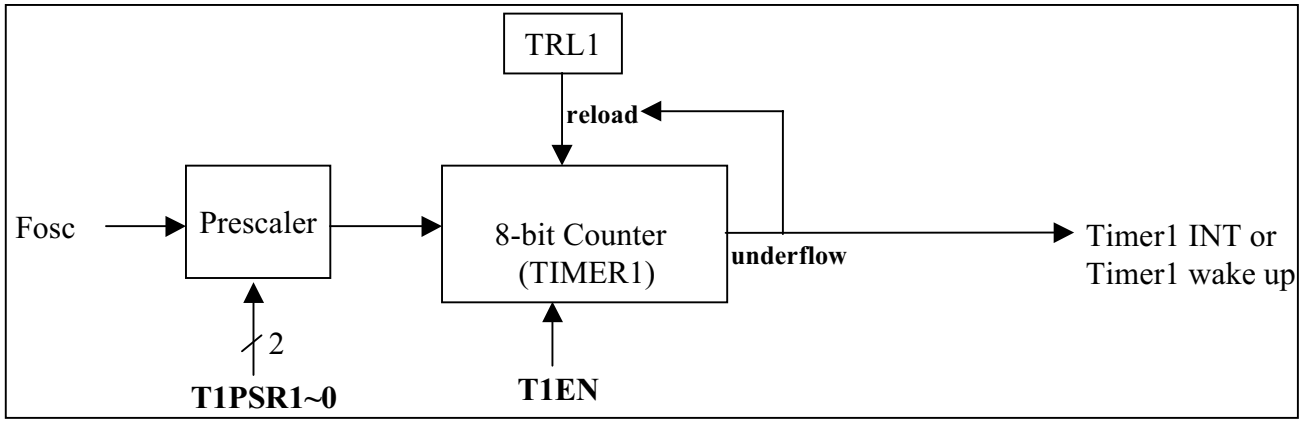
bit 7 bit0

-	-	-	SRBFI	LVDI	TMR2I	TMR1I	**TMR0I**

◆ **TMR0I**: Set to 1 when TMR0 underflow happened. Clear to 0 by software or Timer0 disable.

2.Timer1(8 bits):

Function Block Diagram:



Function Description:

Timer1 is a general purpose 8 bits down counter for some applications required time counting. There are interrupt and wake up function available for user's application. The clock source is from the oscillator clock.

There is a prescaler for the timer. The **T1PSR1~T1PSR0** bit of TRCON register determine the prescale ratio and generate different clock rate as the clock source for the timer. Set **T1WKEN** bit of TRCON register to 1 will enable Timer 1 underflow wake up function in IDLE MODE.

Counting value will be decreased by one(count down) according to the timer clock source. When underflow happens, the timer interrupt will be triggered if the global interrupt and timer1 interrupt are both enabled. At the same time,TRL1 will automatic reload into 8 bits counter.

The Timer1 frequency range is from 0.5 Hz(TRL1=FFh, prescaler=1:256) to 8.192KHz(TRL1=0h, prescaler=1:4).

$$T = \frac{1}{Fosc} * Prescale * (TRL1+1)$$

Register Description:

- **TRL1(Timer 1 reload register):**
  Used to store the auto reload value of TIMER1. When enabling Timer1 or underflow happens, TRL1 register will automatically reload into 8 bits counter .

- **TRCON(Timer0 & Timer1 control register)**

bit 7 bit0

T1WKEN	**T1EN**	**T1PSR1**	**T1PSR0**	T0EN	T0CS	T0PSR1	T0PSR0

◆ **T1PSR1~T1PSR0**: Timer1 Prescaler select bits.

T1PSR1:T1PSR0	Prescale value
00	1:4
01	1:16
10	1:64
11	1:256

◆ **T1EN:** Timer1 enable control bit

0: Disable Timer1(stop counting) .

1: Enable Timer1 .

◆ **T1WKEN:** Enable bit of Timer1 underflow wake up function in IDLE MODE.

0: Disable Timer1 wake up function .

1: Enable Timer1 wake up function.

- **INTCON (INT Control Register)**

bit 7 bit0

-	**-**	**-**	SRBFIE	LVDIE	TMR2IE	**TMR1IE**	TMR0IE

◆ **TMR1IE**: Control bit of TIMER1 interrupt.

0: Disable interrupt function.

1: Enable interrupt function.

- **INTSTA (INT STATUS Register)**

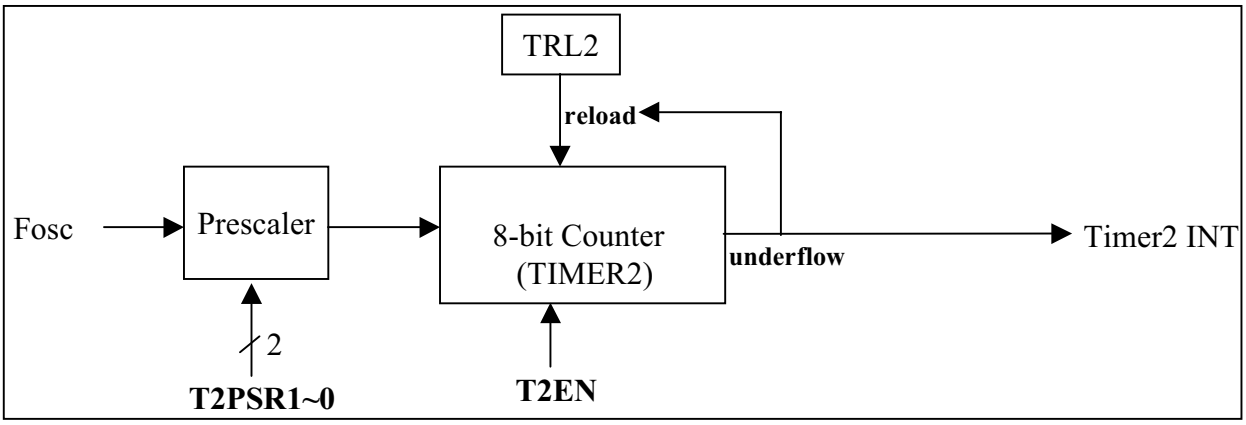
bit 7 bit0

-	**-**	**-**	SRBFI	LVDI	TMR2I	**TMR1I**	TMR0I

◆ **TMR1I**: Set to 1 when TMR1 underflow happened. Clear to 0 by software or Timer1 disable.

3.Timer2(8 bits):

Function Block Diagram:



Function Description:

Timer2 is a general purpose 8 bits down counter for some applications required time counting. There is an interrupt available for user's application. The clock source is from the oscillator clock.

There is a prescaler for the timer. The **T2PSR1~T2PSR0** bit of MWTCON register determine the prescale ratio and generate different clock rate as the clock source for the timer.

Counting value will be decreased by one(count down) according to the timer clock source. When underflow happens, the timer interrupt will be triggered if the global interrupt and timer2 interrupt are both enabled. At the same time,TRL2 will automatic reload into 8 bits counter

The Timer2 frequency range is from 16 Hz(TRL2=FFh, prescaler=1:8) to 32.768KHz(TRL2=0h, prescaler =1:1).

$$T = \frac{1}{Fosc} * Prescale * (TRL2+1)$$

Register Description:

- **TRL2(Timer 2 reload register):**
  Used to store the auto reload value of TIMER2. When enabling Timer2 or underflow happens, TRL2 register will automatically reload into 8 bits counter .

- **MWTCON(Melody Timer , WDT and Timer 2 control register)**

bit 7 bit0

T2EN	**T2PSR1**	**T2PSR0**	WDTEN	WDTPSR1	WDTPSR0	MTEN	MDO2EN

◆ **T2PSR1~T2PSR0**: Timer2 Prescaler select bits.

T2PSR1:T2PSR0	Prescale value
00	1:1
01	1:2
10	1:4
11	1:8

◆ **T2EN:** Timer2 enable control bit

0: Disable Timer2(stop counting) .

1: Enable Timer2 .

- **INTCON (INT Control Register)**

bit 7 bit0

-	-	-	SRBFIE	LVDIE	**TMR2IE**	TMR1IE	TMR0IE

◆ **TMR2IE**: Control bit of TIMER2 interrupt.

0: Disable interrupt function.

1: Enable interrupt function.

- **INTSTA (INT STATUS Register)**

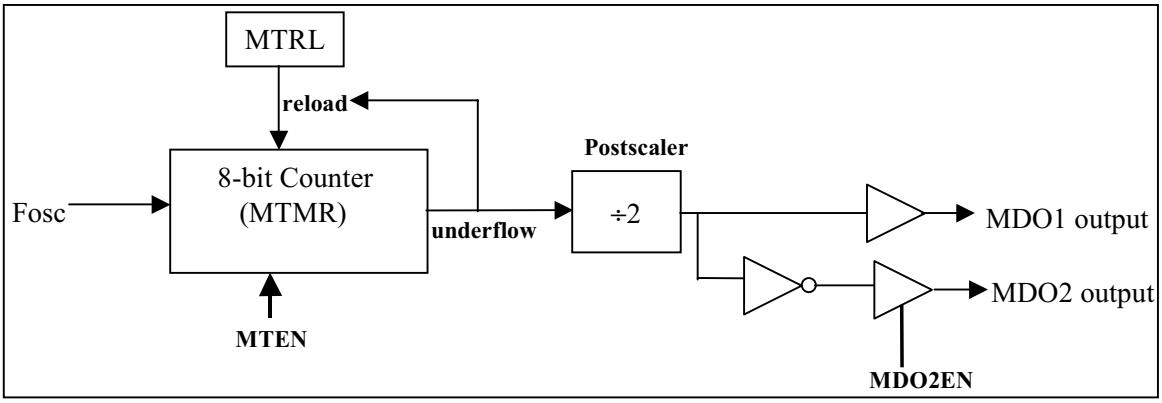
bit 7 bit0

-	-	-	SRBFI	LVDI	**TMR2I**	TMR1I	TMR0I

◆ **TMR2I**: Set to 1 when TMR2 underflow happened. Clear to 0 by software or Timer2 disable.

4.Melody Timer(8 bits):

Function Block Diagram:



Function Description:

Melody Timer is suitable for counting the tempo and rhythm of music. There are positive/negative output available for user's application. The clock source is from the oscillator clock(32.768KHz).

When set **MTEN to 1** will enable Melody Timer.

Counting value will be decreased by one(count down) according to the timer clock source. When enabling Melody Timer or underflow happens, MTRL will automatic reload into 8 bits counter. And **MDO1** and **MDO2** pin output level will toggle at the same time. **MDO2** pin output is the inverse of **MDO1** pin.

The frequency range of melody timer is from 64 Hz(MTRL=FFh, postscaler=1:2) to 16KHz(MTRL=0h, postscaler=1:2).

$$F = Fosc * \frac{1}{(MTRL+1)} * \frac{1}{2}$$

Pin Description:

- **MDO1(Melody positive output):** Melody positive output pin.
- **MDO2(Melody negative output):** Melody negative output pin.

Register Description:

- **MTRL(Melody Timer reload register):**
  Used to store the auto reload value of melody timer. When enabling Melody Timer or underflow happens, MTRL will automatically reload into 8 bits counter .

- **MWTCON(Melody Timer , WDT and Timer 2 control register)**

bit 7 bit0

T2EN	T2PSR1	T2PSR0	WDTEN	WDTPSR1	WDTPSR0	**MTEN**	**MDO2EN**

  - **MTEN**: Melody Timer enable control bit.
  - **MDO2EN**: Melody negative output port enable control bit.

Melody Table:

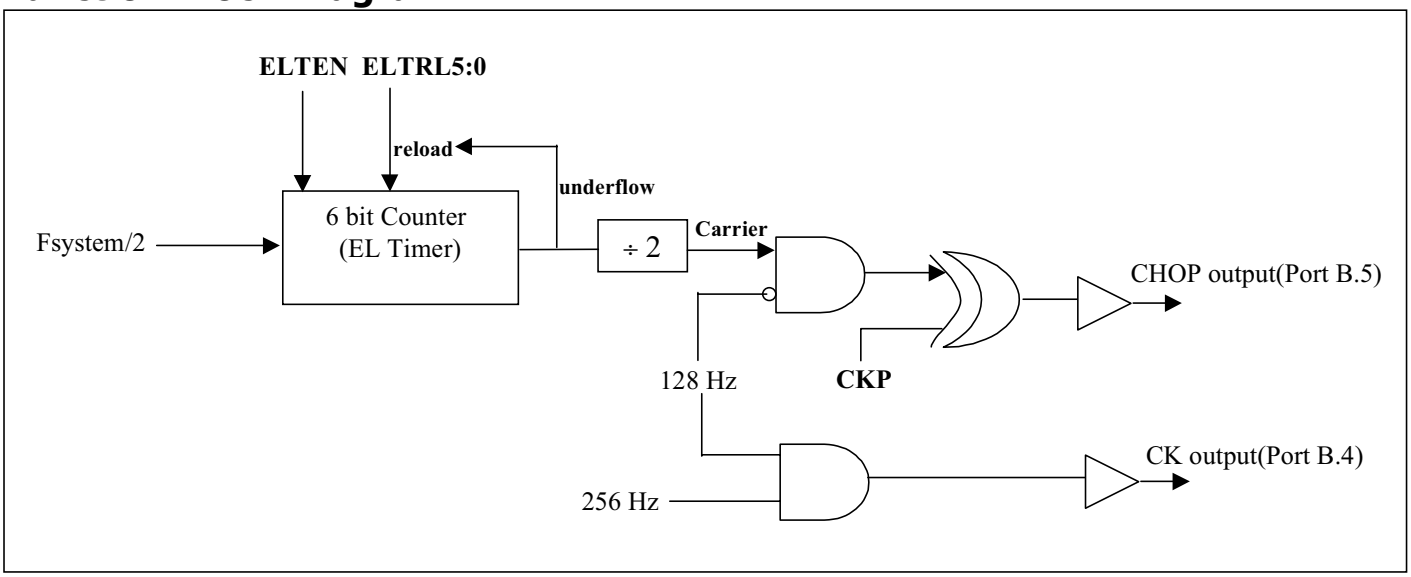
Clock source : 32768 Hz

Musical note	Standard Frequency(Hz)	MTRL	Postscaler	F_{MELODY}(Hz)	DEV(%)
L1	130.813	**124**	1:2	131.07	0.20%
L1#	138.591	**117**	1:2	138.85	0.18%
L2	146.832	**111**	1:2	146.29	-0.37%
L2#	155.563	**104**	1:2	156.04	0.31%
L3	164.814	**98**	1:2	165.49	0.41%
L4	174.614	**93**	1:2	174.30	-0.18%
L4#	184.997	**88**	1:2	184.09	-0.49%
L5	195.998	**83**	1:2	195.05	-0.48%
L5#	207.652	**78**	1:2	207.39	-0.13%
L6	220.000	**73**	1:2	221.41	0.64%
L6#	233.082	**69**	1:2	234.06	0.42%
L7	246.942	**65**	1:2	248.24	0.53%
M1	261.626	**62**	1:2	260.06	-0.60%
M1#	277.183	**58**	1:2	277.69	0.18%
M2	293.665	**55**	1:2	292.57	-0.37%
M2#	311.127	**52**	1:2	309.13	-0.64%
M3	329.628	**49**	1:2	327.68	-0.59%
M4	349.228	**46**	1:2	348.60	-0.18%
M4#	369.994	**43**	1:2	372.36	0.64%
M5	391.995	**41**	1:2	390.10	-0.48%
M5#	415.305	**38**	1:2	420.10	1.16%
M6	440.000	**36**	1:2	442.81	0.64%
M6#	466.164	**34**	1:2	468.11	0.42%
M7	493.883	**32**	1:2	496.48	0.53%
H1	523.251	**30**	1:2	528.52	1.01%
H1#	554.365	**29**	1:2	546.13	-1.48%
H2	587.330	**27**	1:2	585.14	-0.37%
H2#	622.254	**25**	1:2	630.15	1.27%
H3	659.255	**24**	1:2	655.36	-0.59%
H4	698.456	**22**	1:2	712.35	1.99%
H4#	739.989	**21**	1:2	744.73	0.64%
H5	783.991	**20**	1:2	780.19	-0.48%

H5#	830.609	**19**	1:2	819.20	-1.37%
H6	880.000	**18**	1:2	862.32	-2.01%
H6#	932.328	**17**	1:2	910.22	-2.37%
H7	987.767	**16**	1:2	963.76	-2.43%

5.EL Timer(6 bits):

Function Block Diagram:



Function Description:

EL Timer is a 6 bit down counter which is suitable for counting the CHOP signal output. The clock source is from 1/2 system clock(1MHz~10MHz).

Counting value will be decreased by one(count down) according to the timer clock source. When underflow happens, the CHOP output level will be toggled. When enabling EL timer or underflow happens , ELTRL will automatic reload into 6 bits counter.

ELTEN bit is used to enable EL timer and change Port B.5 and Port B.4 to CHOP and CK output pin. **CKP** bit is used to select clock polarity of CHOP output.(See timing diagram for detail)

The frequency range of CHOP carrier signal will be 128Hz(System clock at 32768Hz, ELTRL=3Fh) to 2.5MHz(System clock at 10MHz, ELTRL=0h).

$$Fchop = (Fsystem / 2) * \frac{1}{(ELTRL+1)} * \frac{1}{2}$$

Pin Description:

- **CHOP pin:** Chop output pin of EL driver.
- **CK pin:** CK output pin of EL driver.

Register Description:

- **ELCON(EL control register)**

bit 7 bit0

ELTEN	CKP	ELTRL5 ~ ELTRL0

◆ **ELTEN:** EL Timer enable control bit.

0: Disable EL Timer(stop counting) and recover CK and CHOP pin to general I/O pin.

1: Enable EL Timer and change Port B.4 and Port B.5 to CK and CHOP output pin.

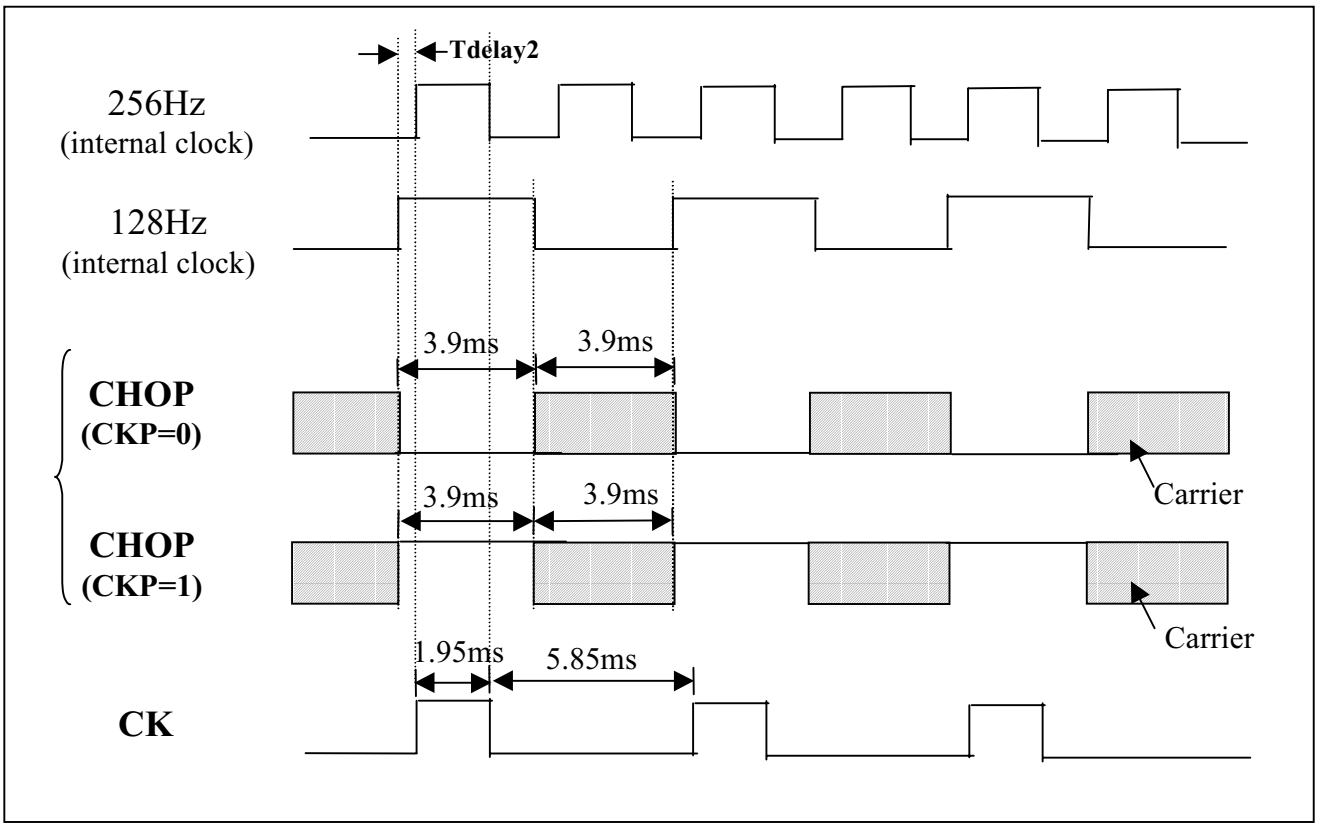
◆**CKP**: EL clock polarity select bit.

0: Idle state for CHOP pin is low level.

1: Idle state for CHOP pin is high level.

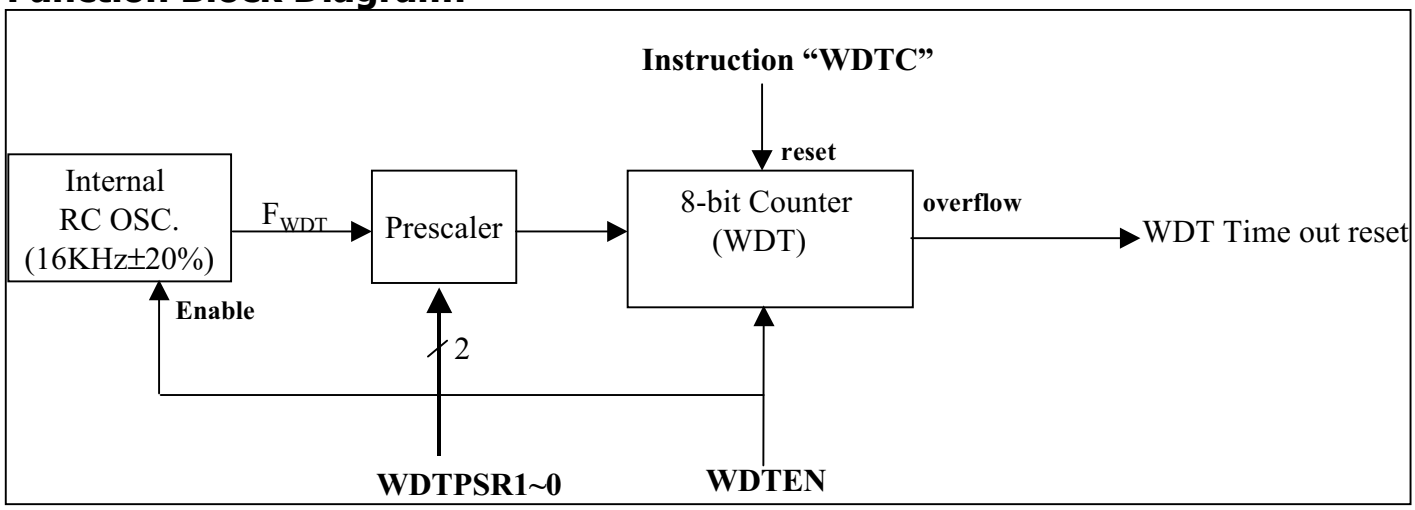
◆**ELTRL5~0:** Used to store the auto reload value of EL timer. When enabling EL timer or underflow happens, **ELTRL5~0** will automatically reload into 6 bits counter .

Timing Diagram:



6.Watch Dog Timer(WDT):

Function Block Diagram:



Function Description:

The clock source of watch dog timer(WDT) is from on-chip RC oscillator(16KHz±20%) . The WDT will keep running even the oscillator has been turned off (i.e. in SLEEP MODE).

WDT time-out will cause the CPU reset(if WDT enabled). To avoid the reset happens, user should clear the WDT value by using "WDTC" instruction before WDT time-out. Set **WDTEN** bit will enable WDT running. The initial state of WDT is disable.

There is also a prescaler to generate different clock rate for the clock source of WDT. The prescaler ratio is defined by **WDTPSR1 & WDTPSR0**.

The WDT time out range will be 64ms(prescaler=1:4) to 2.048 second (prescaler=1:128).

Register Description:

- **MWTCON(Melody Timer , WDT and Timer 2 control register)**

bit 7							bit0
T2EN	T2PSR1	T2PSR0	**WDTEN**	**WDTPSR1**	**WDTPSR0**	MTEN	MDO2EN

◆ **WDTPSR1~WDTPSR0**: Watch Dog timer Prescaler select bits.

WDTPSR1:WDTPSR0	Prescale value
00	1:4
01	1:16
10	1:64
11	1:128

◆ **WDTEN:** Watch Dog Timer enable bit

0: Disable watch dog timer(stop running) .

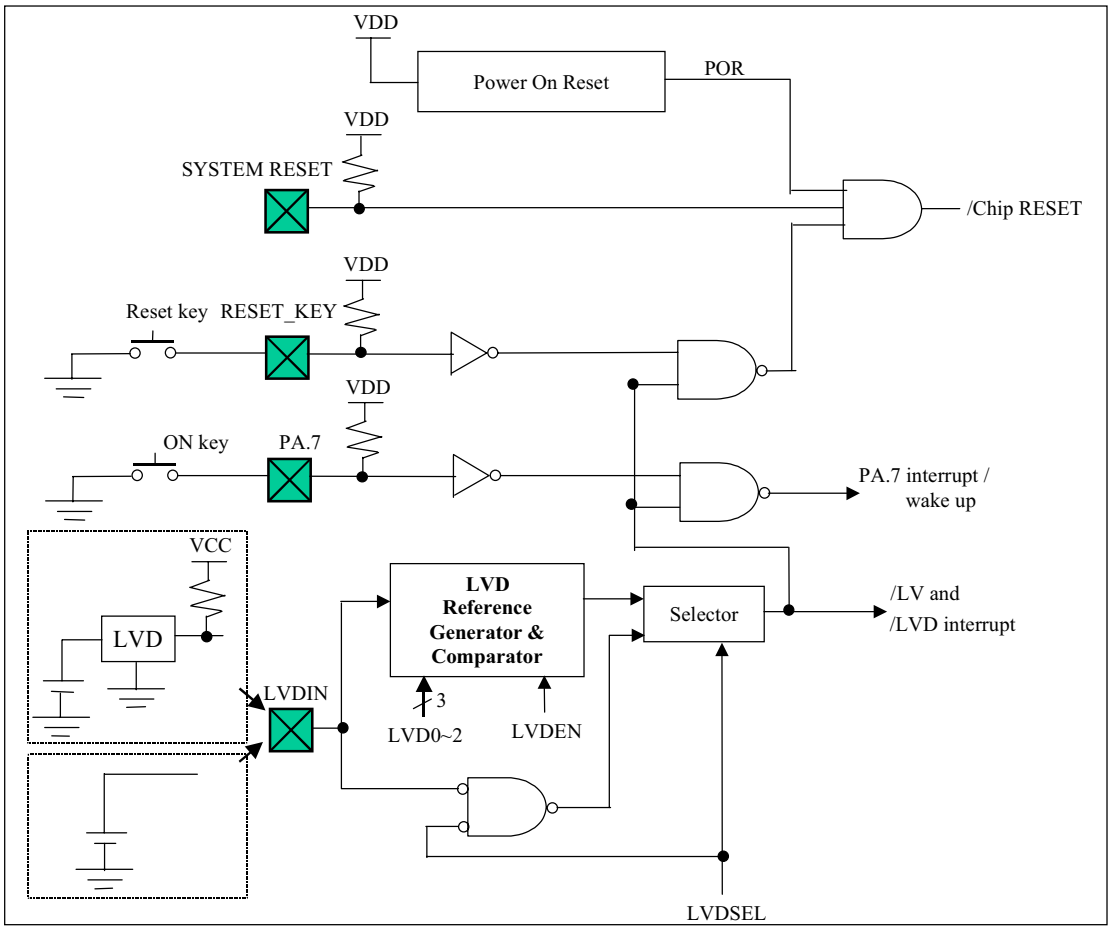
1: Enable watch dog timer .

B. LOW VOLTAGE DETECTION(LVD)

Feature:

- Built-in LVD (Low Voltage Detector),
  $V_{det(Vth-)}$=2.2V ~ 2.9V ±0.1V. selectable.
- When the voltage of LVDIN pin is lower than selected detection voltage(/LV=0),
  PA.7 interrupt/Wake up is disabled.
  And the reset function of RESET_KEY pin is unavailable.
- Built-in LVD/ External LVD selectable.
- LVD interrupt optional.

Block Diagram:



Function Description:

Low Voltage Detection function is used to detect Battery Low. When enable **LVDEN** bit of CPUCON Register, **/LV** bit is the voltage detection result of **LVDIN** pin. When the voltage of **LVDIN** pin is lower than Vdet(Vth-), **/LV** bit will be clear.

Setup **LVDSEL** bit of STBCON register to select either external LVD device or internal built-in LVD.

Setup **LVD2~LVD0** bit of PACON register to determine the detection voltage.

User can enable Low Voltage Detected Interrupt function. If **/LV** bit becomes low, interrupt will happen at the same time.

When low level detected(/LV=0), the PA.7 interrupt/wake up is disable. And the reset caused by RESET_KEY pin is disable.

Pin Description:

- **LVDIN:** Input pin of Low Voltage Detection to examine the voltage level higher than Vdet(Vth+) or lower than Vdet(Vth-).

Register Description:

- **CPUCON Register:**

bit 7 bit0

CLKOEN	CKS	**LVDEN**	**/LV**	/GLINTD	PS	MS1	MS0

◆**/LV**: Low voltage detected. This is a read only bits. When the voltage **LVDIN** pin is lower than Vdet(Vth-), this bit will be clear. Otherwise if higher than Vdet(Vth+) ,this bit will be set.

0: Low voltage is detected.

1: Low voltage is not detected or LVD is disable.

/LV bit will be set to 1 when LVD disable.

◆**LVDEN:** Enable Low Voltage Detector.

LVDEN bit will be clear after CPU reset.

- **PACON (Port A Control Register)**

bit 7 bit0

LVD2	**LVD1**	**LVD0**	**LVDSEL**	Bit7PU	R2EN	R1EN	KE

◆ **LVD2~0**: LVD detection voltage select bits.

The default value of LVD2~0 after CPU reset is "000".

LVD2~0	Vdet(Vth-)	Vdet(Vth+)	Deviation	LVD2~0	Vdet(Vth-)	Vdet(Vth+)	Deviation
000	2.2V	2.3V	±0.1V	100	2.6V	2.7V	±0.1V
001	2.3V	2.4V		101	2.7V	2.8V	
010	2.4V	2.5V		110	2.8V	2.9V	
011	2.5V	2.6V		111	2.9V	3.0V	

◆ **LVDSEL:** Built in LVD/External LVD select

0: External LVD selected.

1: Built-in LVD selected.

- **INTCON (INT Control Register)**

bit 7 bit0

-	-	-	SRBFIE	**LVDIE**	TMR2IE	TMR1IE	TMR0IE

◆ **LVDIE**: Control bit of LVD interrupt.

0: Disable interrupt function.

1: Enable interrupt function.

- **INTSTA (INT STATUS Register)**

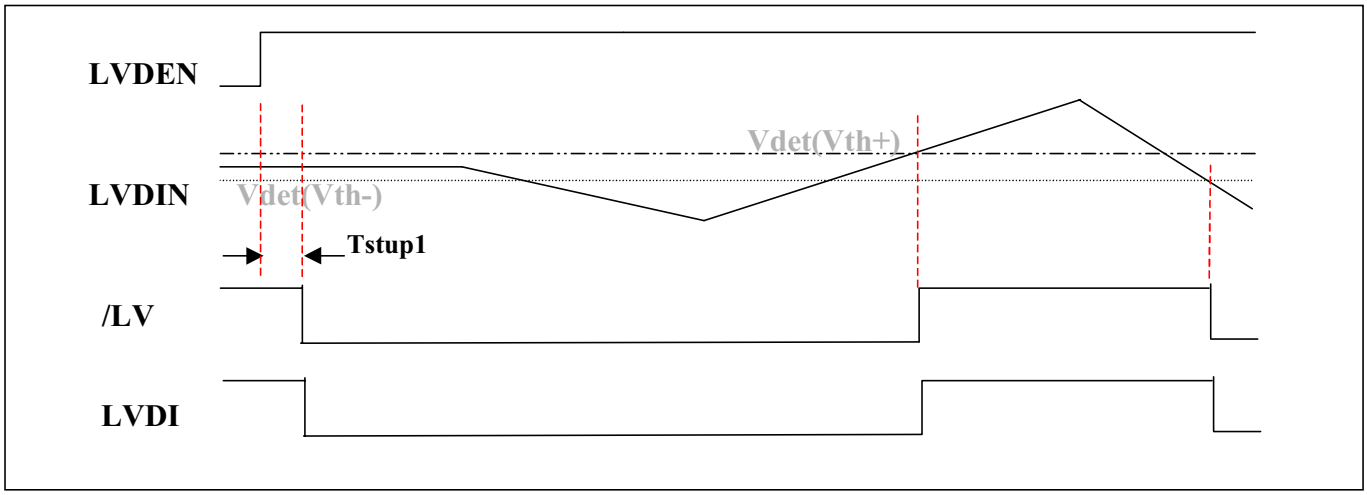
bit 7 bit0

-	-	-	SRBFI	**LVDI**	TMR2I	TMR1I	TMR0I

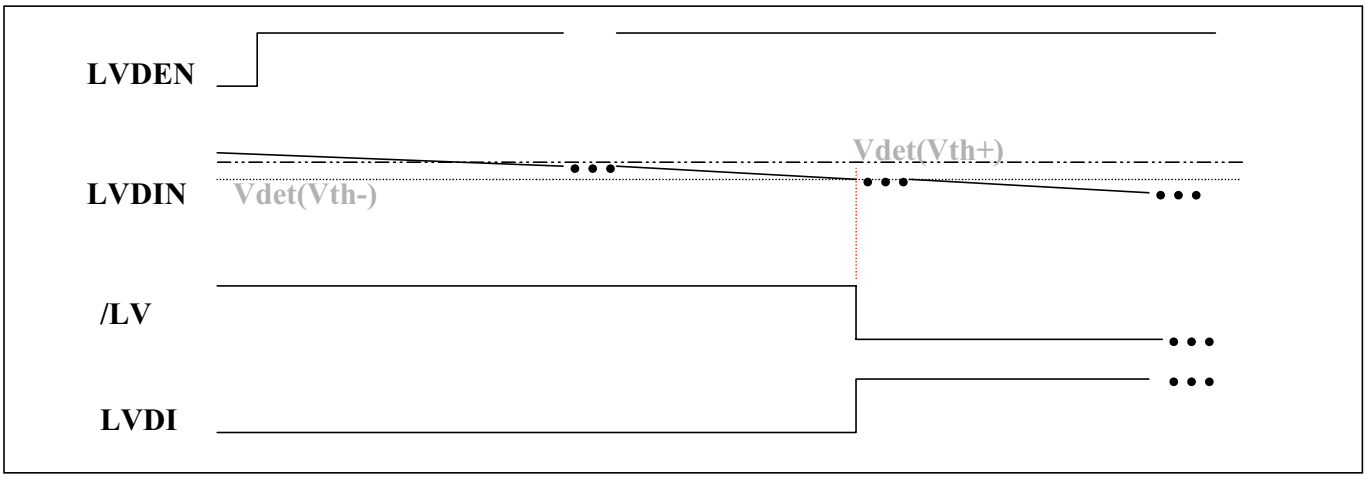
◆ **LVDI**: Set to 1 when LVD low level detected(**Falling edge**). Clear by software or LVD disable.

Timing diagram:

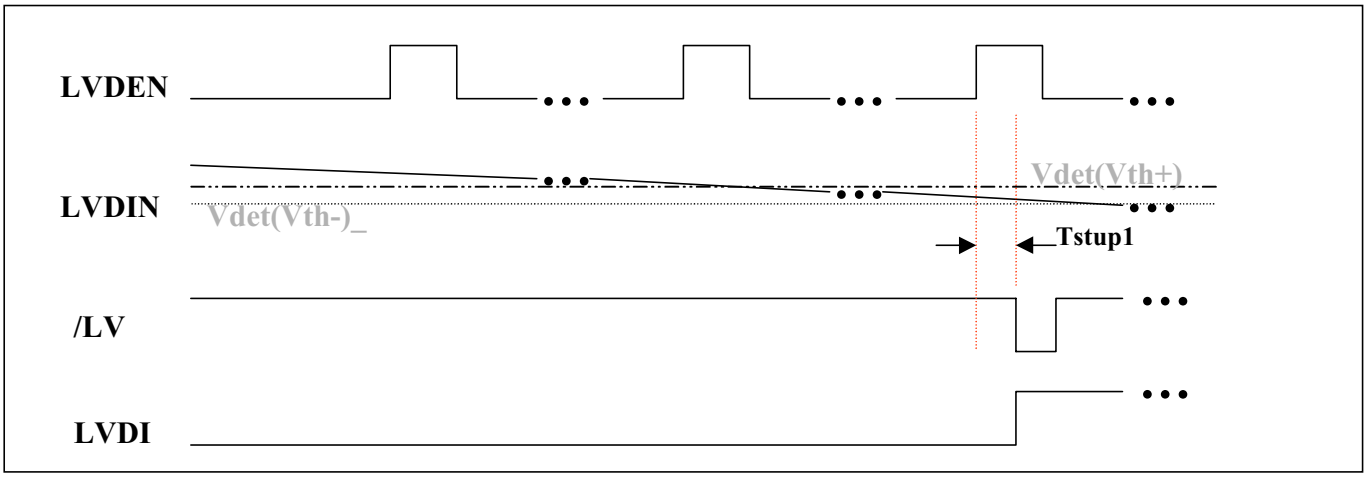
(1)LVDIN voltage is within Vdet threshold region when enabling LVD: *LOW voltage detected*



(2)Continuous LVD Detection



(3) Power Saving Control of LVD



C. SERIAL PERIPHERAL INTERFACE (SPI)

Features:

- Operation in either Master mode or Slave mode.
- Three-wire or Four-wire full duplex synchronous communication.
- Programmable Shift Register Length(24/16/8 bits).
- Programmable bit rates of communication.
- Programmable clock polarity.
- Programmable shift direction.
- Programmable sample phase
- Interrupt flag available for the read buffer full.
- Up to 2.5MHz (system clock at 10MHz) bit frequency.

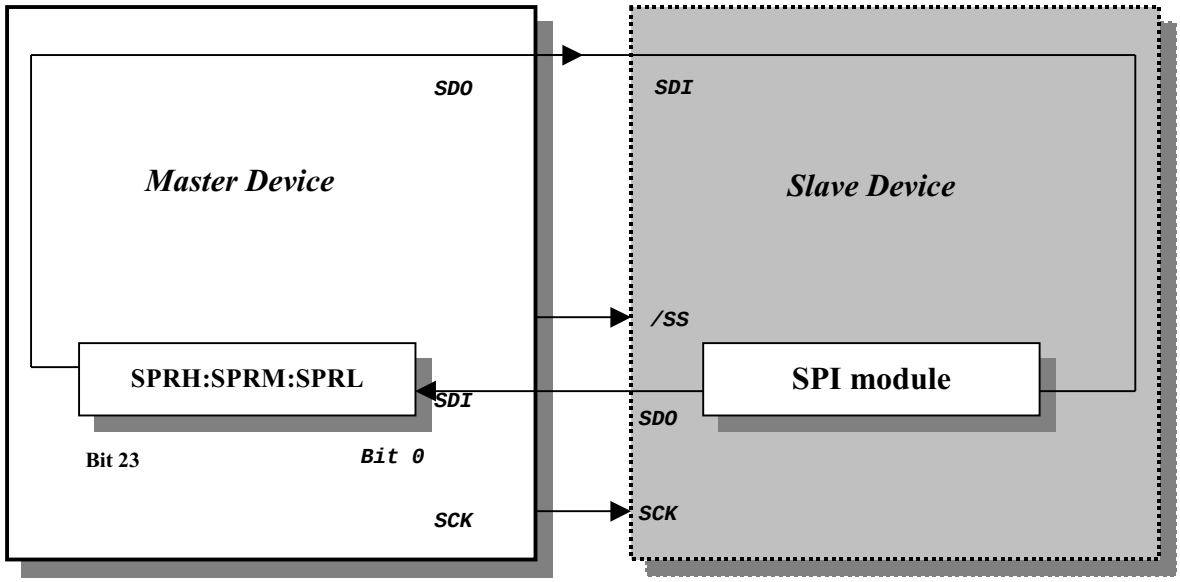


Fig 1 Single SPI Master / Slave Communication

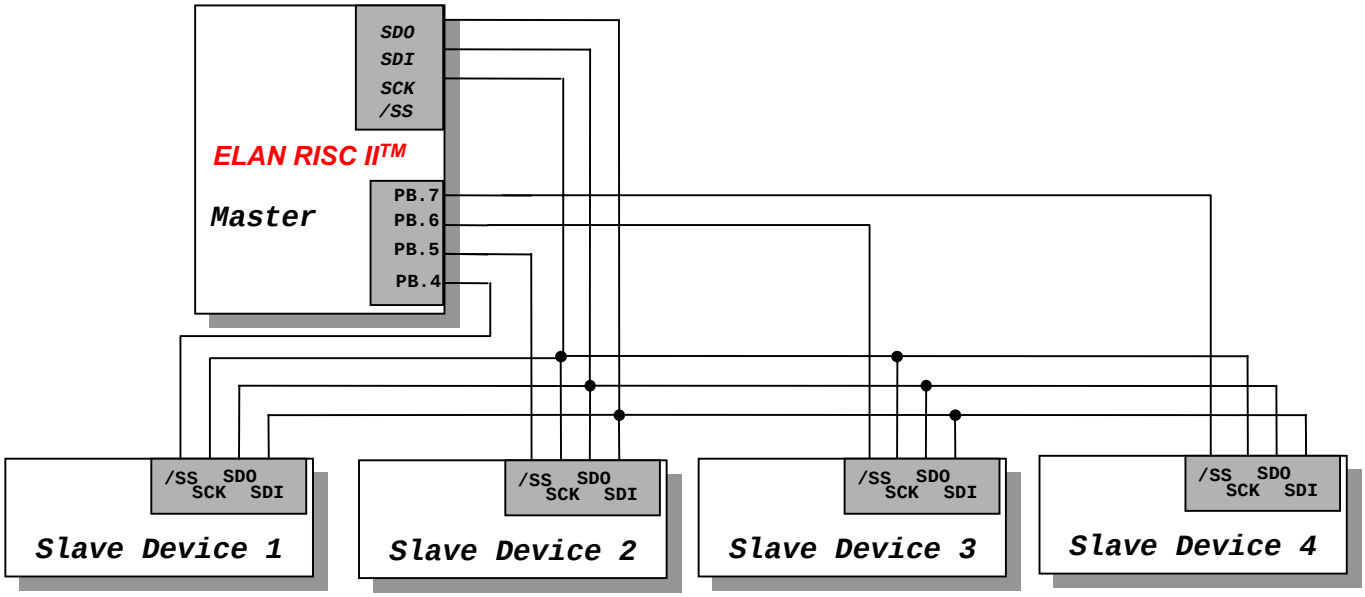


Fig 2 The SPI configuration example of Single-Master and Multi-Slaves

Function Block:

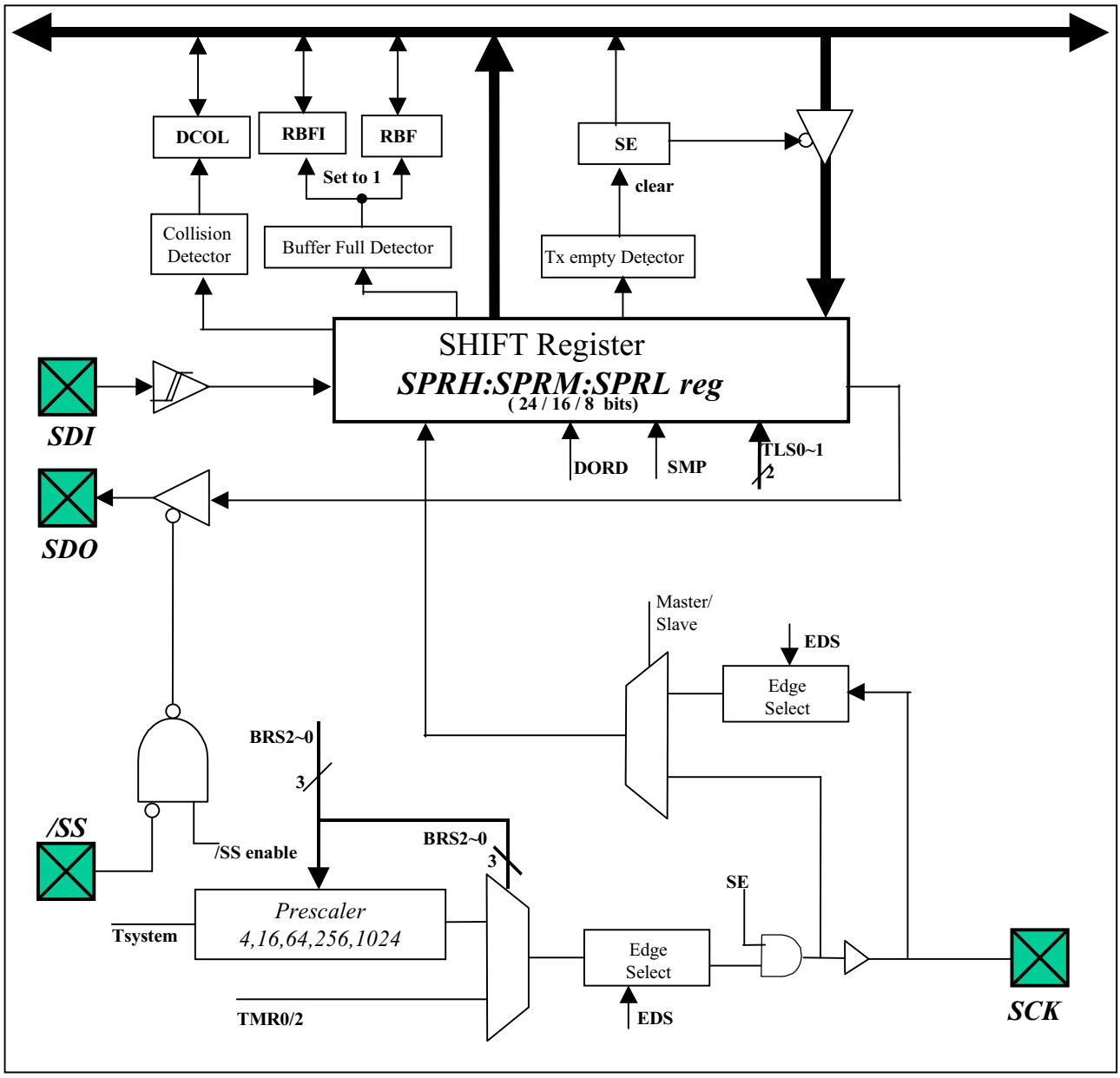


Fig 3 SPI block diagram

Function Description

Fig. 1 shows how MCU communicates with other devices by SPI module. If MCU is a master controller, it sends clock through the SCK pin. An 8-bit data is transmitted and received at the same time. If MCU, however, is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted at selected clock rate and the selected edge.

Setup **TLS1~TLS0** bit of SPICON register to select the shift register length of SPI and enable/disable SPI function. Setup **BRS2~BRS0** bit of SPICON register to select the SPI mode(master/slave) and Bit Rate. When master mode, the clock source can be selected from system clock or half of timer 0 interval. When slave mode, the /SS pin can be enable or disable. Set up the **DORD** bit of SPICON register can determine the shift direction. Set up the **EDS** bit of SPICON register can select raising edge or falling edge latch the data. Set up the **SMP** bit of SPISTA register can select the sample phase at middle or the end of data output time.

(1)MASTER MODE:

In master mode, SCK pin is as a clock output pin.

If select 24 bits shift register length, SPRH, SPRM and SPRL register is the high, middle and low byte of the shift register. (If select 8 bits shift register length, SPRL register is the content of the shift register.) During write data to SPRH, SPRM and SPRL register, after write data into SPRL register, **SE** bit of SPICON register will be set by hardware automatically and start shifting. After shift buffer empty, **SE** bit will be clear by hardware and stop clock output from **SCK** pin.

Receiver is active while SPI transfer. When receive buffer full, **RBF** flag will be set and interrupt happens(if enable). During read out the shift register content, after SPRL register has been read out, hardware will clear the **RBF** flag automatically. If SPRL register not been read out, **RBF** bit still remains set. Data collision will happens when next clock in.

(2)SLAVE MODE:

In slave mode, input clock is from MASTER device. SCK pin is as a clock input pin. The **SE** bit is not useful to control starting shift in this mode. But it is a Transfer buffer empty status bit.

The same as MASTER MODE, user can select shift register length. And write transfer data to SPRH, SPRM, SPRL register. After write data into SPRL register, **SE** bit of SPICON register will be set by hardware. But the start shifting is control by the MASTER device clock input.

While shift buffer empty the **SE** bit will be clear. At the same time, receive buffer was full, **RBF** flag will be set and interrupt happens(if enable). The received data is at SPRH, SPRM and SPRL register, user should read them out before next clock in. Otherwise the data was collision and **DCOL** bit of SPI STATUS register will be set.

Pin Description:

- **SDI(I):** Serial Data Input.
  Receive serially.
- **SDO(O):** Serial Data Output .
  Transmit serially.
  In slave mode, defined as high-impedance, if not selected.
- **SCK(I/O):** Serial Clock input/output . When Master mode, sends clock through the SCK pin. However, if defined as a slave, its SCK pin is programmed as an input pin .
- **/SS(I):** /Slave Select . This pin (/SS) will be active when enable /SS function (BRS=110),else /SS pin is a general purpose I/O.
  Master device remains low to /SS pin to signify the slave(s) for transmit/receive data. Ignores the data on the SDI and SDO pins while /SS is high, because the SDO is no longer driven.

Register Description:

- **SPRH:SPRM:SPRL:** SPI shift buffer for 24/16/8 bits length.
  The buffer will deny any write until the shifting is completed.
  If user select 24 bits shift buffer, SPRH:SPRM:SPRL register is the content of 24 bits shift buffer. Else if select 8 bits shift buffer, SPRL register is the content of the shift register.
  When write data into SPRL register, **SE** bit of SPICON will be set by hardware and start shifting.
  While shift buffer empty ,at the same time, receive buffer was full, the received data is shifted in SPRH, SPRM and SPRL register. After SPRL register has been read out, hardware will clear the **RBF** flag automatically.

- **SPICON(SPI Control register):**

bit 7 bit0

TLS1	TLS0	BRS2	BRS1	BRS0	EDS	DORD	SE

- **TLS1~TLS0:** Shift buffer length select. Shift buffer length is programmable.
  00: SPI disable
  01: Enable SPI and shift buffer length = 24 bits
  10: Enable SPI and shift buffer length = 16 bits
  11: Enable SPI and shift buffer length = 8 bits

◆ **BRS2~BRS0:** Bit rate select. Programming the clock frequency/rates and sources.

000:Master,TMR0/2
001:Master,Fsystem/4.
010:Master,Fsystem/16.
011:Master,Fsystem/64.
100:Master,Fsystem/256.
101:Master,Fsystem/1024.
110:Slave,/SS enable
111:Slave,/SS disable

Prescaler		Fsystem		
BRS2:0	**Bit rate**	**10MHz**	**4MHz**	**32.768KHz**
001	Fsystem/4	2500000	1000000	8196
010	Fsystem/16	625000	250000	2048
011	Fsystem/64	156250	62500	512
100	Fsystem/256	39063	15625	128
101	Fsystem/1024	9766	3906	32

Unit: bits/sec

Table. SPI bit rate table

◆ **EDS:** Select the raising / falling edges latch by programming the EDS bit
0: Falling edge
1: Raising edge

◆ **DORD:** Data transmission order.
0:Shift left (MSB first)
1:Shift right (LSB first)

◆ **SE:** Shift enable.
Set to 1 automatically when write data into SPRL register and begin to shift.
Reset to 0 when transfer buffer empty detected.
SE bit will be clear by hardware when enabling SPI.

● **SPISTA(SPI status register):**

bit 7 bit0

LCDM1	LCDM0	SFR1	SFR0	**SPWKEN**	**SMP**	**DCOL**	**RBF**

◆ **RBF:** Set to 1 by Buffer Full Detector, and clear to 0 automatically when read data from **SPRL** register.
RBF bit will be clear by hardware when enabling SPI. And **RBF** bit is read-only . Therefore, read SPRL register is necessary to avoid data collision happens(**DCOL**).

- **DCOL:** SPI Data collision.
  0:Data collision didn't occurs
  1:Data collision occurs. Should be cleared by software.
- **SMP:** SPI data input sample phase.
  0:Input data sampled at middle of data output time
  1:Input data sampled at the end of data output time
  In slave mode, data input sample is fixed at middle of data output time.
- **SPWKEN:** SPI wake up enable control bit.
  0:Disable SPI (slave mode) read buffer full wakeup.
  1: Enable SPI (slave mode) read buffer full wakeup.

- **INTCON (INT Control Register)**

bit 7							bit0
-	-	-	**SRBFIE**	LVDIE	TMR2IE	TMR1IE	TMR0IE

- **SRBFIE**: Control bit of SPI read buffer full interrupt .
  0: Disable interrupt function.
  1: Enable interrupt function.

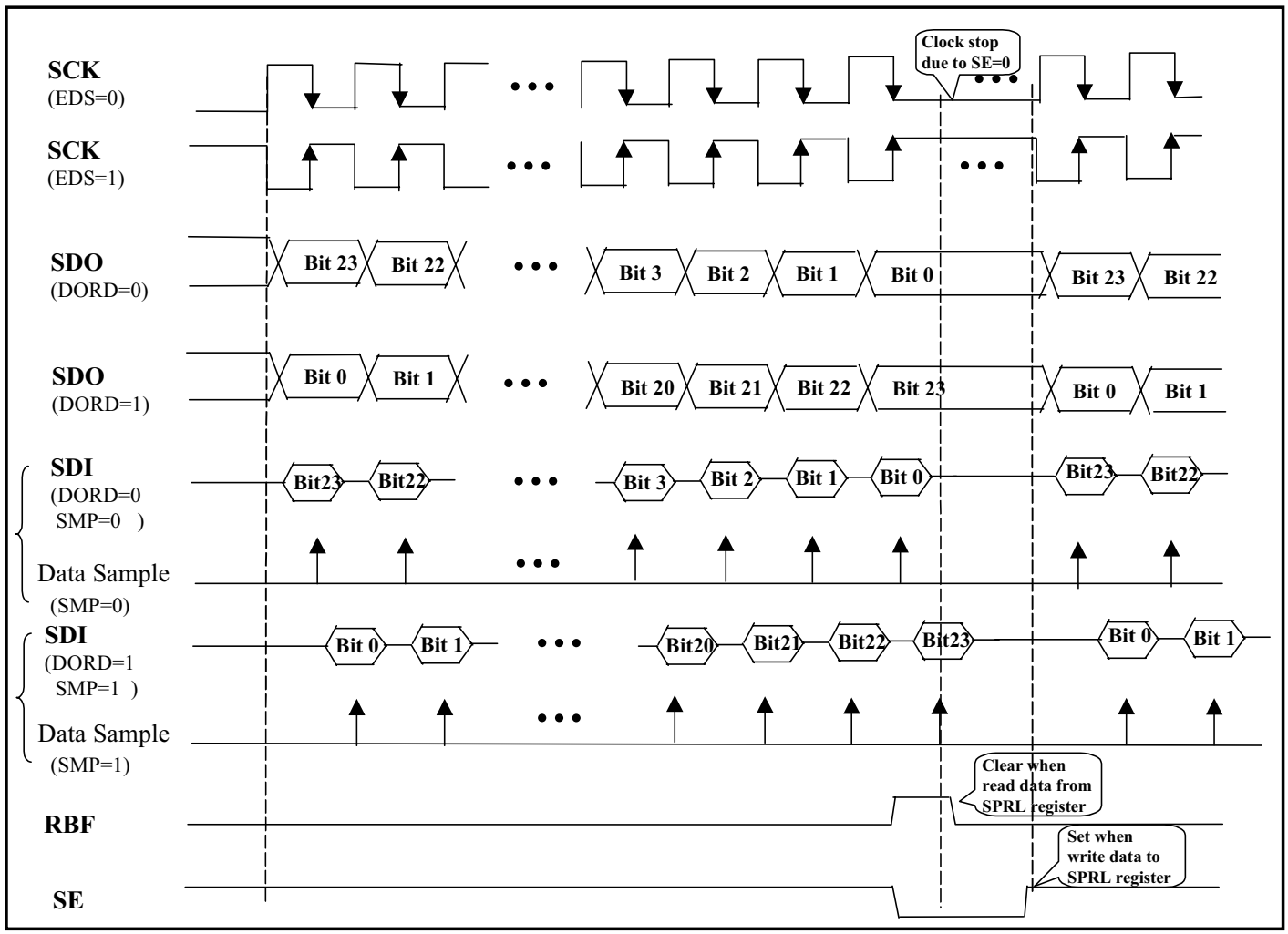
- **INTSTA (INT STATUS Register)**

bit 7							bit0
-	-	-	**SRBFI**	LVDI	TMR2I	TMR1I	TMR0I

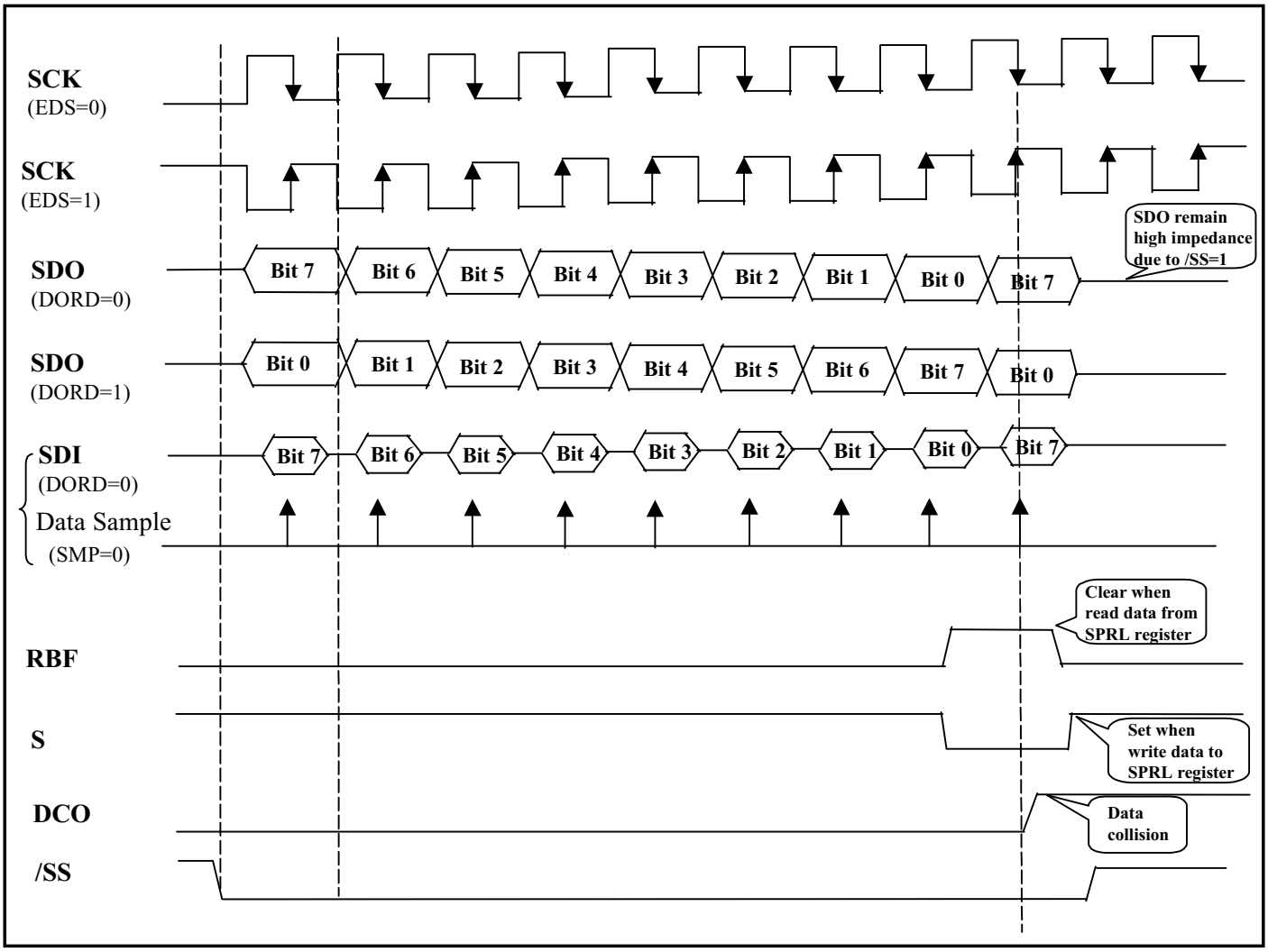
- **SRBFI**: Set to 1 when SPI read buffer full happened. Clear to 0 by software or SPI disable.

Timing Diagram:

(1)MASTER MODE: (Shift buffer Length = 24bits)



(2)SLAVE MODE: (Shift buffer Length = 8 bits , /SS enable)

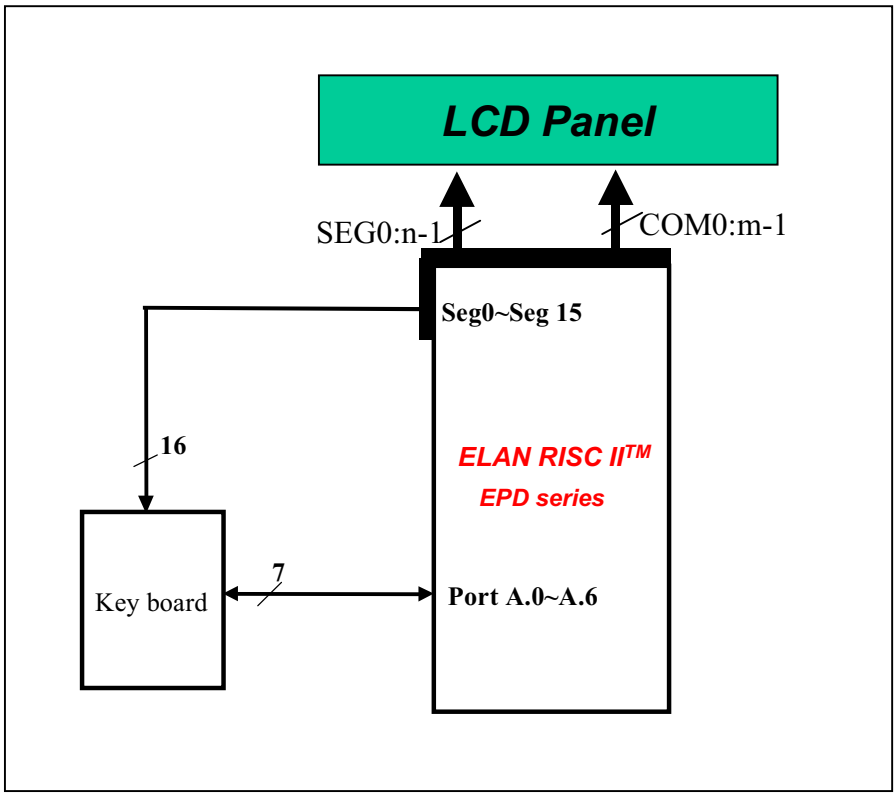


D. Key I/Os

Feature

- 7 pins key input(Port A) and 16 pins key strobe (share with LCD segment) can achieve maximum 112 keys matrix.
- Automatic key scan or software key scan.
- Interrupt available when automatic key scan(**SCAN**=1).
- Wakeup available when key input low level detected at automatic key scan mode(**SCAN**=1).

Function Block Diagram



Function Description

(1)Key Input:

As shown in the following figure, it is considered that Key strobe output has resistance $R_{ON,}$ and each key has resistance K_{ON} and the capacitance C.

Because longtime strobe output makes LCD display confused, strobe output should be as short as possible.

So R_{IN} (pull-up resistance) should be low enough for the Capacitance to be charged quickly.

But R_{IN} should be high enough for V_{IN} to be judged in "L" level. (R_{IN} >> R_{ON} + K_{ON})

Therefore the value of R_{IN} should be able to be changeable.

Refer to the following “Key input process”.

Key input process

1. Output the strobe signal
2. Pull up the input port by lowest resistance(R1 and R2 enable) : Capacitance is charged quickly.
3. Pull up the input port by highest resistance(R2 only enable).
4. Read the key.
5. Disable the pulled-up resistance.
6. Stop the strobe signal

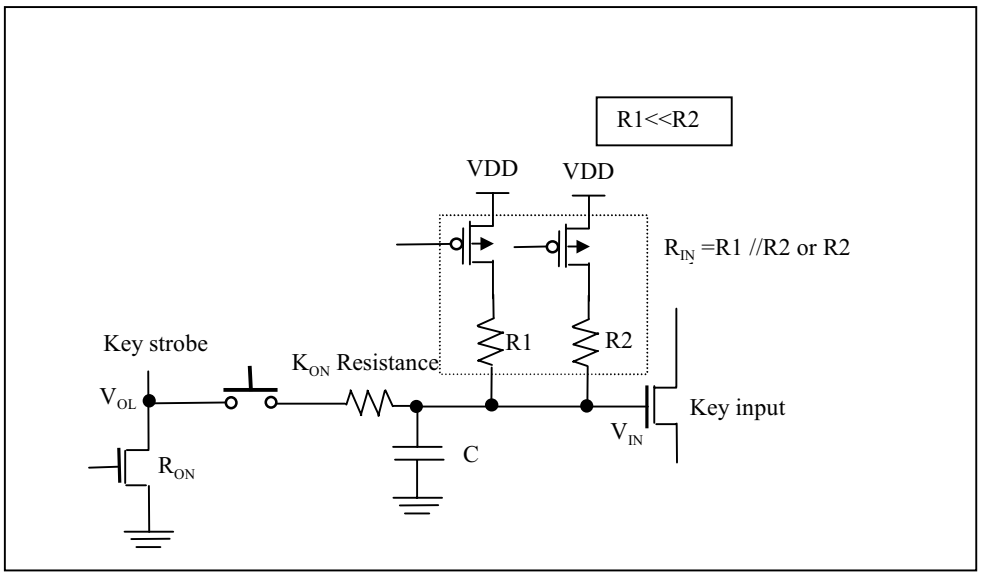


Fig. Key circuit

Functions:

SCAN	BitST	KE	/R1EN	/R2EN	SSCAN *1	SCAN *1	IEN *1	Total pullup resistor	PORTA.0~.A.6	Note
0	0	x	1	1	0	0	0	Floating	0	
	1	0	1	1			0	Floating	0	*A
			1	0			0	R2	0	
			0	1			0	R1	0	
			0	0			0	R1 // R2 *2	0	*B
		1	1	1			1	Floating	Floating	Prohibited
			1	0			1	R2	PA.0~.6	*C
			0	1			1	R1	PA.0~.6	
			0	0			1	R1 // R2 *2	PA.0~.6	
1	x	x	1	1	0	0	0	Floating	0	*A
			0	0	0	1	0	R1//R2 *2	0	*B
			1	0	1	1	1	R2	PA.0~.6	*C

*1 : Internal signal - Refer the following "Automatic KeyScan Timing"

*2 R1 // R2 = R1R2 / (R1+R2)

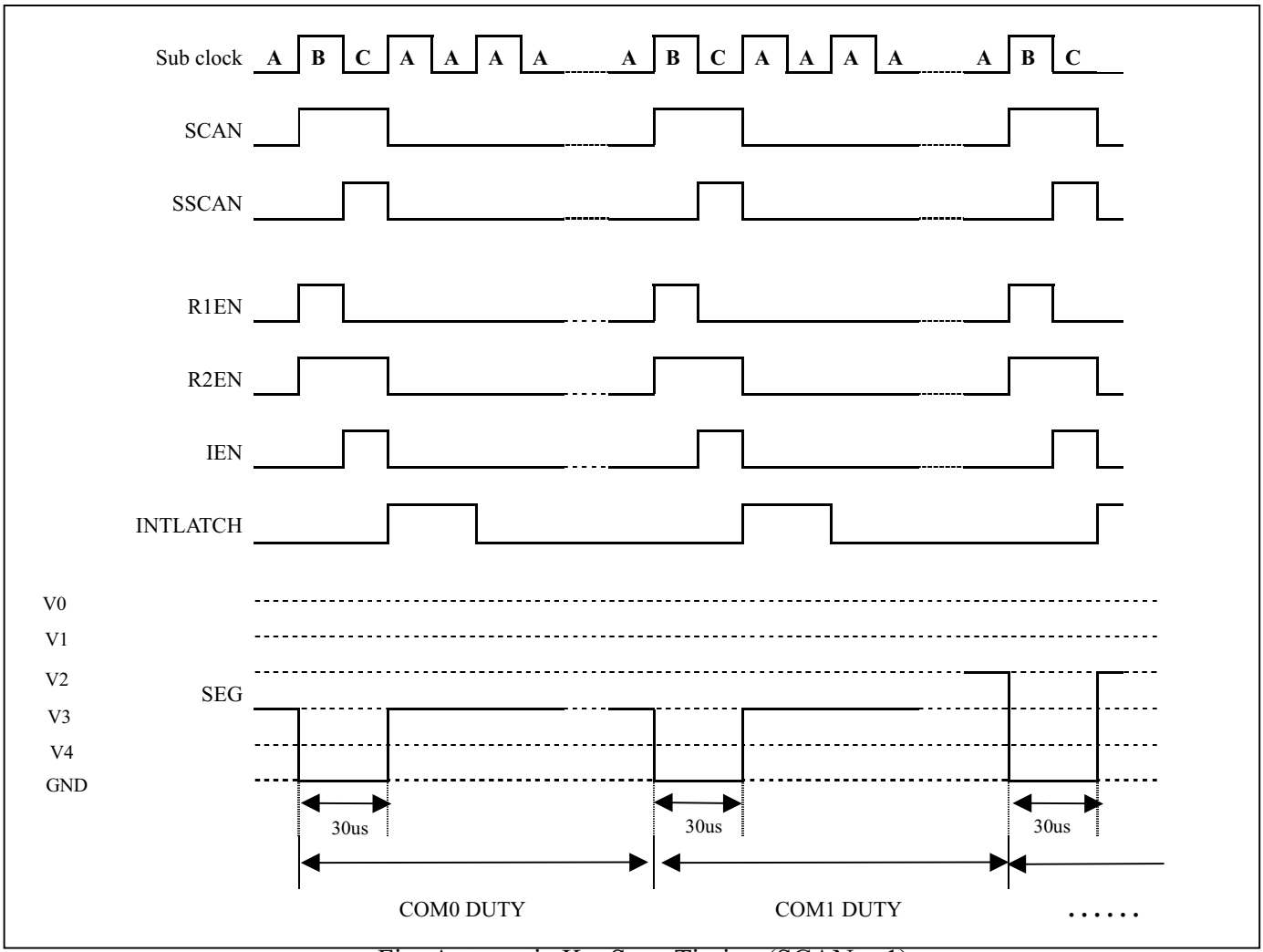


Fig. Automatic KeyScan Timing (SCAN = 1)

(2) Key Strobe :

Key strobe pin share with LCD segment pin in CPU with embedded LCD driver model .

When shared with LCD segment, to prevent LCD display confused, strobe output should be as short as possible.

The strobe signal can output in the following two ways.

(1) Automatic key scan:

LCD waveform has a 30us low pulse at the beginning of every common duty signal by setting **SCAN** bit of STBCON register. The strobe timing is as the following figure.

When automatic key scan mode, the PAINT or PORT A wakeup must enable. During Key scan, wakeup and interrupt will happens if key input pin(Port A) low level detected.

(2) Software key scan :

Segment is switched to strobe signal temporally by setting **BitST** bit of STBCON register to 1 and **SCAN** bit to 0.

Setup **STB3~STB0** bit of STBCON register to select which pin will be strobed.

In this mode user can set **ALL** bit of STBCON register to let segment 0~15 to hold at GND level.

In IDLE MODE, when automatic key scanning, if PA.0~.6 pin low level detected(when IEN=1), wake up will happen. Then CPU running and interrupt happened (If enable) .

In SLOW MODE or FAST MODE, both automatic key scan and software key scan will be used.

Step 1:Automatic key scan will be used to examine "**Is there any key pressed?** ". If key pressed, PA.0~.6 pin low level detected **,** then **interrupt will happen** .

Step 2: Software key scan will examine "**which key was pressed**".

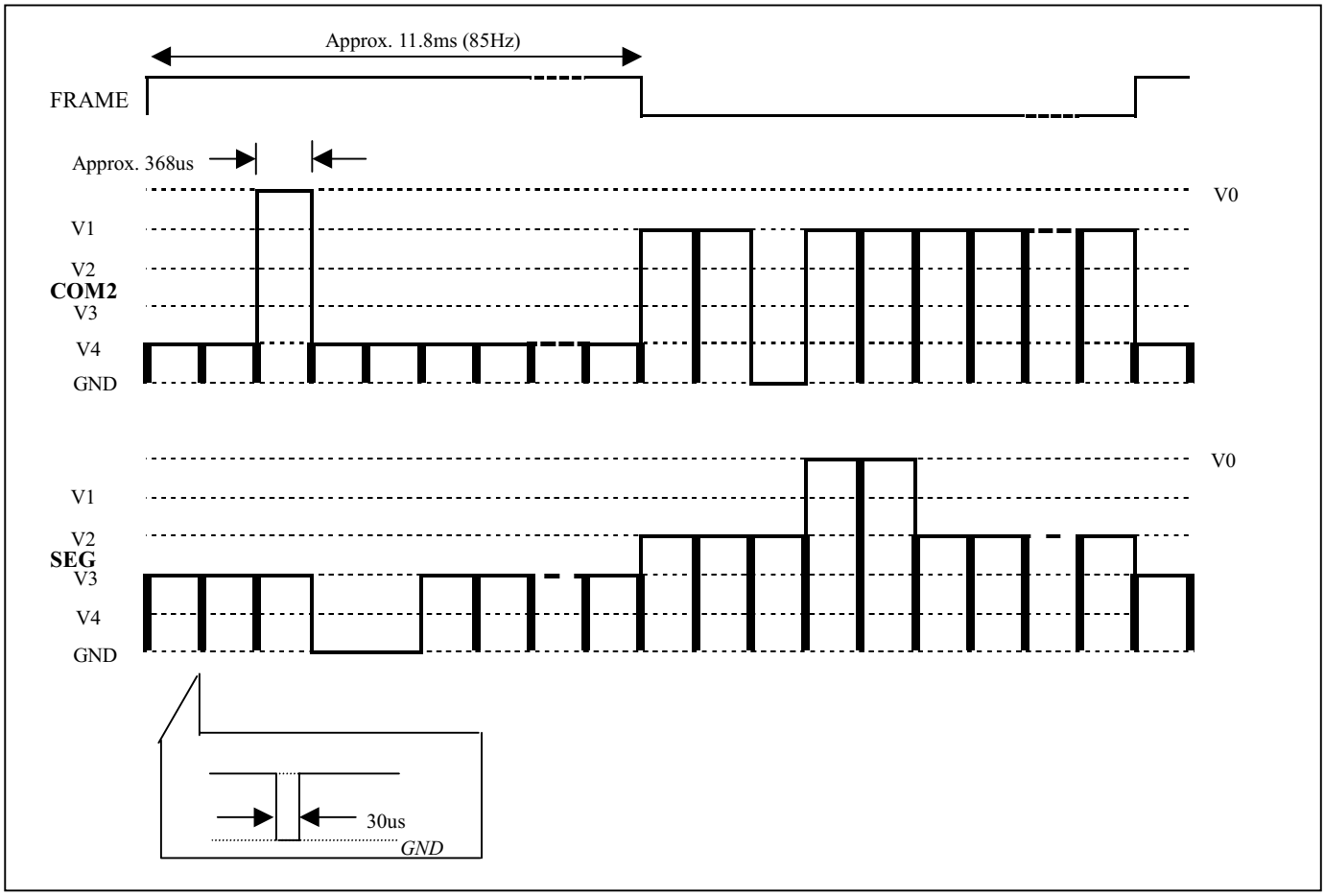


Fig. Automatic strobe signal (SCAN = 1)

The function of key strobe pin is as following table.

STBCON				Key Strobe (Share with Segment 0~15)																LCD	
SCAN	**BitST**	**ALL**	**STB3~0**	**seg 0**	**seg 1**	**seg 2**	**seg 3**	**seg 4**	**seg 5**	**seg 6**	**Seg 7**	**seg 8**	**seg 9**	**seg 10**	**Seg 11**	**seg 12**	**seg 13**	**seg 14**	**seg 15**	**seg 16: n-1**	**com 0:m -1**
0	0	x	xxxx	Display waveform																	
0	1	0	0000	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Display waveform	
			0001	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1		
			0010	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1		
			0011	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1		
			0100	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1		
			0101	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1		
			0110	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1		
			0111	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1		
			1000	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1		
			1001	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1		
			1010	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1		
			1011	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1		
			1100	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1		
			1101	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1		
			1110	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1		
			1111	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0		
		1	xxxx	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
1	x	x	xxxx	Display waveform with automatic key scan																	

Register Description

- **PortA register (Port A register)**

bit 7 bit0

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

◆ **Bit6~Bit0** : Key input , input interrupt or wake up pin. The input structure and 2 stage pull up resistor is controlled together by **/R1EN**,**/R2EN** and **KE** bit of PACON register.

- **PACON (Port A Control Register)**

bit 7 bit0

LVD2	LVD1	LVD0	LVDSEL	Bit7PU	/R2EN	/R1EN	KE

◆ **KE:** Key input enable/disable control bit.

0: Disable Key input function (PORTA register is ***NOT*** correspondence with Key input in software scan mode).

1: Enable Key input function (PORTA register is correspondence with Key input in software scan mode).

◆ **/R1EN:** R1 pull up resistor(small resistor) control bit.

0: Enable R1 pull up resistor.

1: Disable R1 pull up resistor.

◆ **/R2EN:** R2 pull up resistor(large resistor) control bit.

0: Enable R2 pull up resistor.

1: Disable R2 pull up resistor.

- **PAINTEN (Port A INTERRUPT Enable Control Register)**

bit 7 bit0

PA7IE	PA6IE	PA5IE	PA4IE	PA3IE	PA2IE	PA1IE	PA0IE

◆ **PA7IE~PA0IE**: Control bit of interrupt .

0: Disable interrupt function.

1: Enable interrupt function.

- **PAINTSTA (Port A INTERRUPT STATUS Register)**

bit 7 bit0

PA7I	PA6I	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I

◆ **PA7I~PA0I**: INT status of Port A interrupt. Set to 1 when pin **falling edge** detected. Clear to 0 by software.

- **STBCON (Strobe output control Register)**

bit 7 bit0

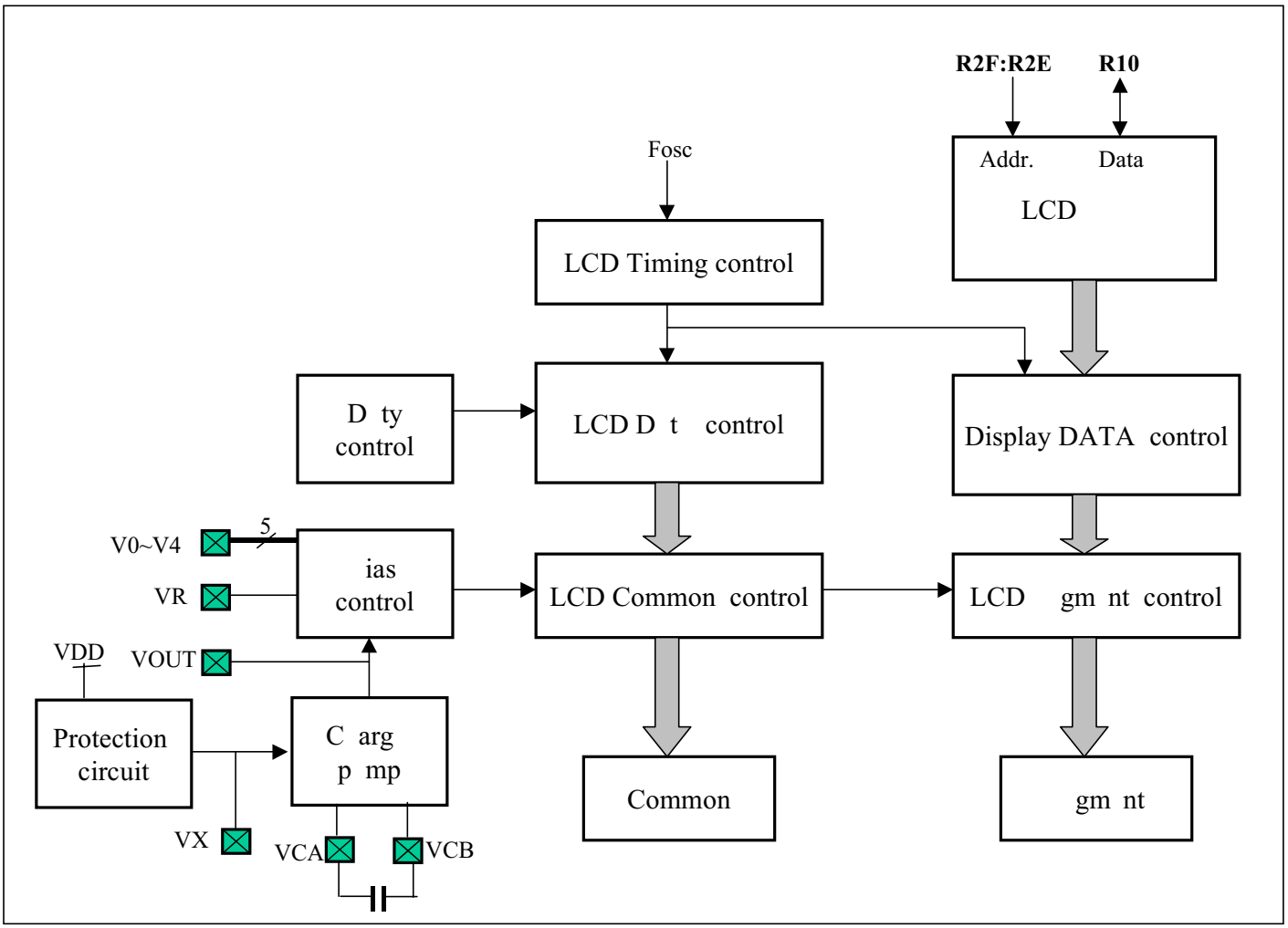
-	SCAN	BitST	ALL	STB3	STB2	STB1	STB0

- **STB0~3:** Strobe output selector bit.
- **ALL:** Set All strobe.
  0 : Bit strobe.
  1 : All strobe.
- **BitST** : Enable Bit strobe
  0 : Display waveform.
  1 : Strobe signal as **STB3~0** defined.
- **SCAN** : Automatic key scan or specify the scan signal bit by bit.
  0 : Key scan was specified as the bit **STB3~0** defined.
  1 : Auto strobe scanning.

E. Embedded LCD DRIVER

ELAN RISC II™ series provide directly drive LCD . It supports 98 segments 32 commons. There are LCD RAM for direct correspondence with LCD Pixel. Charge pump can pump to 2 times of VDD. The LCD contrast has 32 level adjustable. And the LCD bias are selectable. The maximum LCD operating voltage can be determined by external resistor RA and RB .

Function Block Diagram



Register Description:

- **LCDCON register (LCD control register A)**

bit 7 bit0

BSEL2	BSEL1	BSEL0	ADJ4	ADJ3	ADJ2	ADJ1	ADJ0

◆ **ADJ4~0:** LCD contrast adjustment .

ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	α	VEV	Contrast
0	0	0	0	0	0	0.75 Vref	Low
0	0	0	0	1	1	0.758 Vref	
.	.	.	.	.	.	.	
.	.	.	.	.	.	.	
1	1	1	1	0	30	0.992Vref	
1	1	1	1	1	31	Vref	High

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV$$

$$VEV = (1 - \frac{(31 - \alpha)}{124}) \times VREF$$

(Vref=2V at 25°C)

◆ **BSEL2~0 :** LCD Bias select

BSEL2	BSEL1	BSEL0	LCD Bias
0	0	0	1/3
0	0	1	1/3.5
0	1	0	1/4
0	1	1	1/4.5
1	0	0	1/5
1	0	1	1/5.5
1	1	0	1/6
1	1	1	1/6.5

- **SPISTA(SPI status register):**

bit 7 bit0

LCDM1	LCDM0	SFR1	SFR0	SPWKEN	SMP	DCOL	RBF

◆ **SFR1~0 :** Frame frequency adjustment.

SFR1	SFR0	CL frequency	Frame frequency (Hz)		
			Min	Typ	Max
0	0	Fosc /13	59.1	78.8	98.6
0	1	Fosc / 14	54.9	73.2	91.5
1	0	Fosc / 15	51.3	68.3	85.4
1	1	Fosc / 16	48.0	64.1	80.1

Note:1. Fosc = 32.8kHz +/- 25% (all conditions)

2.This table is based on 1/32 duty.

◆ **LCDM1~0:** LCD operation mode control register.

LCDM1:LCDM0	Operation mode
00	Disable(LCD off)
01	Blanking
10	LCD enable
11	

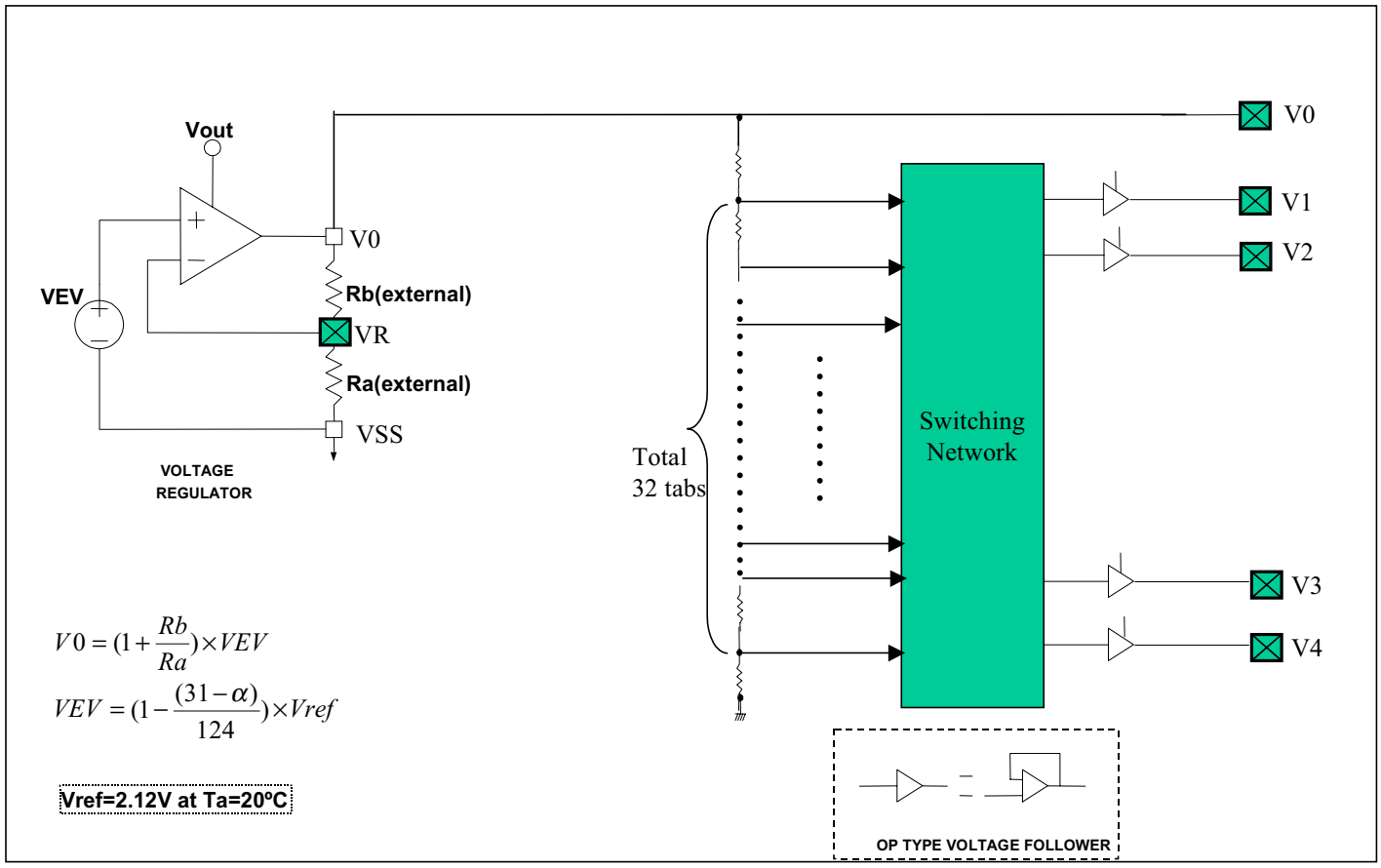
Note: Blanking means All COM & SEG pin are tied to ground.

LCD Power circuit:

- **LCDARH:LCDARL(LCD RAM address):**

  *LCDARH: Page address for LCD RAM.

  *LCDARL: Column address for LCD RAM.



LCD RAM MAP:

PAGE 00 (LCDARH=00H)

RAM address		COM0	COM1	COM2	COM3	COM4	COM5	COM6	COM7
	LCDARL	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
SEG0	00H								
SEG1	01H								
SEG2	02H								
:	:								
:	:								
SEG96	60H								
SEG97	61H								

PAGE 01 (LCDARH=01H)

RAM address		COM8	COM9	COM10	COM11	COM12	COM13	COM14	COM15
	LCDARL	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
SEG0	00H								
SEG1	01H								
SEG2	02H								
:	:								
:	:								
SEG96	60H								
SEG97	61H								

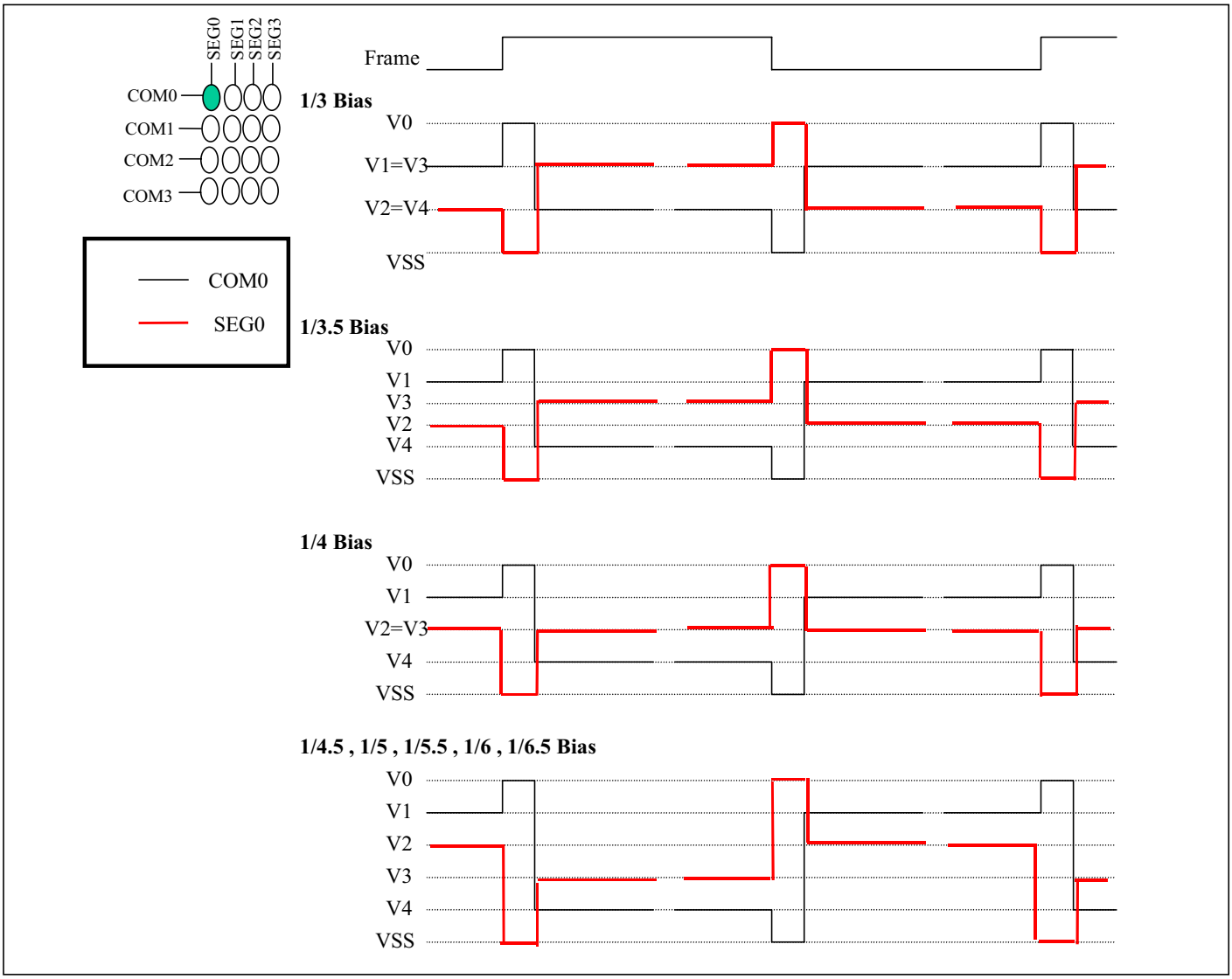
PAGE 02 (LCDARH=02H)

RAM address		COM16	COM17	COM18	COM19	COM20	COM21	COM22	COM23
	LCDARL	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
SEG0	00H								
SEG1	01H								
SEG2	02H								
:	:								
:	:								
SEG96	60H								
SEG97	61H								

PAGE 03 (LCDARH=03H)

RAM address		COM24	COM25	COM26	COM27	COM28	COM29	COM30	COM31
	LCDARL	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
SEG0	00H								
SEG1	01H								
SEG2	02H								
:	:								
:	:								
SEG96	60H								
SEG97	61H								

LCD WAVEFORM:



VIII. Electrical characteristic

ABSOLUTE MAXIMUM RATINGS

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD		-0.3 to +3.6	V
Input voltage (general input port)	VIN		-0.5 to VDD +0.5	V
Input voltage(PA[0:6])	VINA		-0.5 to **V0**+0.5	V
Operating temperature range	TOPR		-10 to +60	°C
Storage temperature range	TSTR		-55 to +125	°C

RECOMMANDED OPERATING CONDITIONS

Items	Sym.	Condition	Limits	Unit
Supply voltage	VDD		2.6 to 3.2	V
Input voltage	VIH		VDD*0.9 to VDD	V
	VIL		0 to VDD*0.1	V
LVDIN voltage	V_{LVD}	LVDSEL=1 (Internal LVD)	2.0V~3.6V	V
Vo voltage	V0	Internal Charge pump	5.3V(Max)	V
Operating temperature	TOPR		0 to +40	°C

DC ELECTRICAL CHARACTERISTICS (condition : Ta=0~+40 °C, VDD= 2.9 +/- 0.3V)

Parameter	Sym.	Condition		Min	Typ	Max	Unit
CLOCK	Fmain	Main-clock frequency		1	-	10	MHz
	Fsub	Sub-clock frequency	RC OSC	24.6	32.8	41	KHz
			X'tal OSC.	-	32.768	-	
Supply current	Idd1	SLEEP mode	VDD=3V,no load(Ta=25 °C)	-	-	1	µA
	Idd2	IDLE mode	VDD=3V, LCD disable, RC OSC	-	8	12	
	Idd3		VDD=3V, LCD disable, X'tal OSC	-	5	8	
	Idd4		VDD=3V, LCD enable, Auto Scan on, RC/X'tal OSC (Vo=3.8V, 1/3 Bias, V1 & V4 OP=*1, V2 & V4 OP=Off ,no load)	-	80	100	
	Idd5	SLOW mode	VDD=3V, LCD disable, RC/X'tal OSC ,no load	-	20	30	
	Idd6	FAST mode	VDD=3V, Fmain=4MHz,no load	-	750	900	
	Idd7		VDD=3V, Fmain=10MHz, ,no load	-	1400	1600	
Input voltage	VIH1	PA[7],PB[0:7] (as general input port)		VDD×0.7	-	VDD	
	VIL1			0	-	VDD×0.3	
	VIH2	PA[0:6](as general input port, LCD enable)		VDD×0.7	-	V0	V
	VIL2			0	-	VDD×0.3	
Input threshold voltage (Schmitt)	VT+	Port A interrupt, SYSTEM RESET and RESET_Key		0.5×VDD	-	0.75×VDD	V
	VT-			0.2×VDD	-	0.4×VDD	
Output current	IOH1	PB[0:3] (as general output port)	VDD=3V , VOH=2.4V	-1	-2	-3	mA
	IOL1		VDD=3V , VOL=0.2V	+1	+2	+3	
	IOH2	PB[6:7]	VDD=3V , VOH=2.5V	-1	-2	-3	
	IOL2		VDD=3V , VOL=0.5V	+1	+2	+3	
	IOH3	PB[4:5]	**VDD=3V, VOH=1V**	-3	-6	-9	
	IOL3		**VDD=3V, VOL=0.5V**	+1.5	+3	+4.5	
Input leakage current	IIL	ALL Input port(without pull up/down resistor) Vin= VDD or GND		-	-	+/-1	µA
Large Pull up resistance	RPU1	PA[0:6]	Key high resistance, pulled up by R2 ,LCD enable	150.	300	450	KΩ
	RPU3	PA[7], PB[0:7],	Vin=GND	500	1000	1500	
	RPU5	SYSTEM RESET And RESET_Key	Vin=GND	200	400	800	
Small Pull up resistance	RPU2	PA[0:6]	Key low resistance, pulled up by R1//R2 ,LCD enable	40	75	110	KΩ
	RPU4	PA[7], PB[0:7],	Vin=2V	50	100	200	
	RPU6	SYSTEM RESET And RESET_Key	Vin=2V	50	100	200	
Large Pull down resistance	RPD1	TEST	Vin=VDD	250	500	750	KΩ
Small Pull down resistance	RPD2	TEST	Vin=1V	10	20	30	
Low battery detect voltage	Vdet	Ta=0 to 40 °C		Vdet –0.1v	Vdet(*1)	Vdet +0.1v	V
LVD supply current	Ilvd	LVDIN=2V		-	3	5	µA
Data retention voltage	Vret			1.6	-	-	V
Power ON reset voltage	Vpor			1.4	1.5	1.6	V
Charge pump output	Vout	Capacitance of charge pump C1 and C2:0.1µF		2×VX-5%	VX×2	-	V
Regulated voltage	V0	VDD=2.3V~3.3V, Ta=0 to 40 °C		V0-4%	V0(*2)	V0+4%	V
Protection circuit voltage	VX			2.6	2.75	2.9	V
Reference voltage	Vref1	Ta=20 °C (*2)		2.035	2.12	2.205	V
	Vref2	Ta=0 °C (*2)		2.169	2.26	2.351	
	Vref3	Ta=40 °C (*2)		1.900	1.98	2.060	
LCD display output ON-resistance	ROC	Com[0:31]	VOH=V0 +/- 0.2V	-	2	3	KΩ
			VOM=V1 +/- 0.2V				
			VOM=V4 +/- 0.2V				
			VOL=0.2V				
	ROS	Seg[0:97]	VOH=V0 +/- 0.2V	-	2	3	KΩ
			VOM=V2 +/- 0.2V				
			VOM=V3 +/- 0.2V				
			VOL=0.2V				
Strobe output ON-resistance	ROP	Seg[0:15]	V=VDD-0.2V	85	165	250	KΩ

	RON		V=0.2V	0.7	1.3	2	
Display frame frequency	Frame	Sub-Clock : RC OSC		57.6	-	87.8	Hz
		Sub-Clock : X'tal OSC		64	-	78.8	
Op. Amp voltage output of LCD power supply	Vout0	V0	No load	-(*4)	V0 (*3)	-(*4)	mV
	Vout1	V1		-(*4)	V1 (*3)	-(*4)	
	Vout2	V2		-(*4)	V2 (*3)	-(*4)	
	Vout3	V3		-(*4)	V3 (*3)	-(*4)	
	Vout4	V4		-(*4)	V4 (*3)	-(*4)	

*1 : Typical detected voltage is chosen by software from the following.

LVD2~0	Vdet(Vth-)	Vdet(Vth+)	Deviation	LVD2~0	Vdet(Vth-)	Vdet(Vth+)	Deviation
000	2.2V	2.3V	±0.1V	100	2.6V	2.7V	±0.1V
001	2.3V	2.4V		101	2.7V	2.8V	
010	2.4V	2.5V		110	2.8V	2.9V	
011	2.5V	2.6V		111	2.9V	3.0V	

*2 : Typical regulated voltage for V0 is chosen by software from the following.

$$V\max = (1 + \frac{Rb}{Ra}) \times Vref$$

$$V0 = (1 - \frac{(31 - \alpha)}{124}) \times V\max$$

0.75 Vmax ≦ V0 ≦ Vmax (32 steps)

Note: Vref temperature coefficient = -7mV/ ℃ (Please refer to Vref1, Vref2, Vref3 DC spec.)

*3 :V0~V4 Theoretical value

Bias	V0	V1	V2	V3	V4
1/3	V0	2/3 * V0	1/3 * V0	2/3 * V0	1/3 * V0
1/3.5		2.5/3.5 * V0	1.5/3.5 * V0	2/3.5 * V0	1/3.5 * V0
1/4		3/4 * V0	2/4 * V0	2/4 * V0	1/4 * V0
1/4.5		3.5/4.5 * V0	2.5/4.5 * V0	2/4.5 * V0	1/4.5 * V0
1/5		4/5 * V0	3/5 * V0	2/5 * V0	1/5 * V0
1/5.5		4.5/5.5 * V0	3.5/5.5 * V0	2/5.5 * V0	1/5.5 * V0
1/6		5/6 * V0	4/6 * V0	2/6 * V0	1/6 * V0
1/6.5		5.5/6.5 * V0	4.5/6.5 * V0	2/6.5 * V0	1/6.5 * V0

*3 : The Target value of V0~V4 is Theoretical value +/- 20mV.

AC ELECTRICAL CHARACTERISTICS (condition : Ta= 0~40 °C, VDD= 2.9 +/- 0.3V)

Parameter	Sym.	Condition	Min	Typ	Max	Unit
Strobe output duration	Tst	Automatic key scan mode(SCAN=1), RC OSC.	22.9	30.5	38.2	µs
		Automatic key scan mode(SCAN=1), X'tal OSC.	-	30.52	-	
LVD stable time	Tstup1	LVDEN ↑ to /LV ↓ (LVDIN=2.0V)	-	30	100	µs
SDI data setup time	Tstup2	Setup time of SDI data input to SCK ↑ or SCK ↓	-	25	50	ns
SDI data hold time	Thold2	Hold time of SDI data input to SCK ↓ or SCK ↑	-	25	50	ns
SDO output valid time	Tvalid1	SCK ↑ or SCK ↓ to SDO data output	-	25	50	ns
SCK input high time	Tsckh	Slave mode (Fmain=10MHz)	200	-	-	ns
SCK input low time	Tsckl	Slave mode (Fmain=10MHz)	200	-	-	ns
Slave mode setup time	Tsetup3	/SS ↓ to SCK ↑ or SCK ↓ (Fmain=10MHz)	400	-	-	ns
Slave mode unselect delay time	Tdelay1	/SS ↑ to SDO output hi-impedance delay time	-	25	50	ns
CK delay time	Tdelay2	CHOP carrier stop to CK ↑ delay time	22.9	30.5	38.2	µs
Instruction cycle time	Tcycle	Fmain=1MHz	-	2(*1)	-	µs
		Fmain=4MHz	-	0.5(*1)	-	
		Fmain=10MHz	-	0.2(*1)	-	

*1: Instruction cycle time= 2 * System clock time

Figure VIII-1: Low voltage detection timing

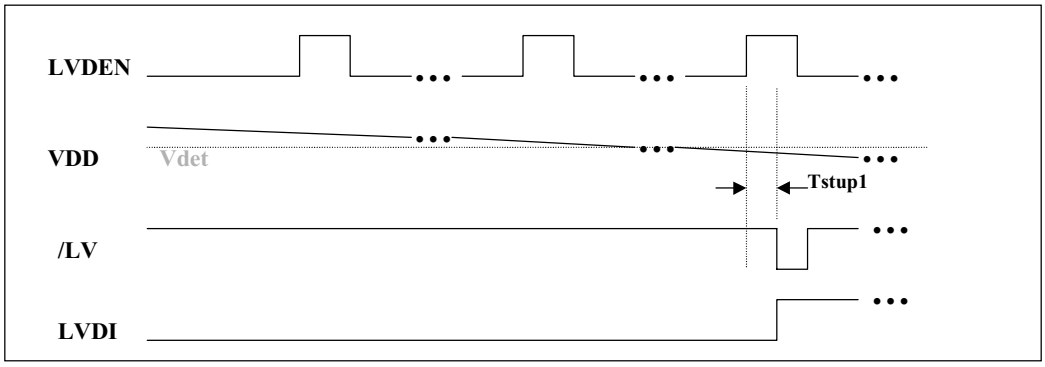


Figure VIII-2: EL timing

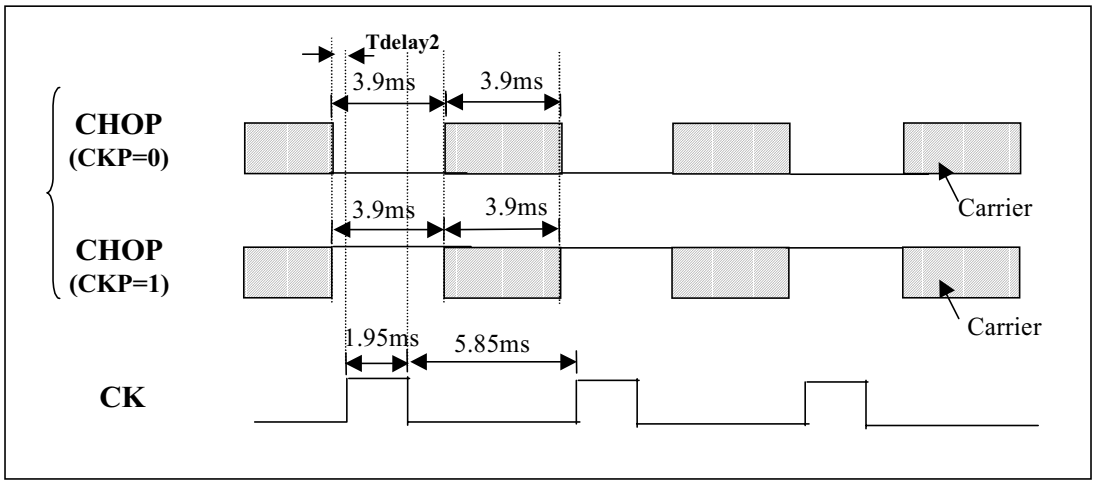


Figure VIII-3: SPI master mode timing

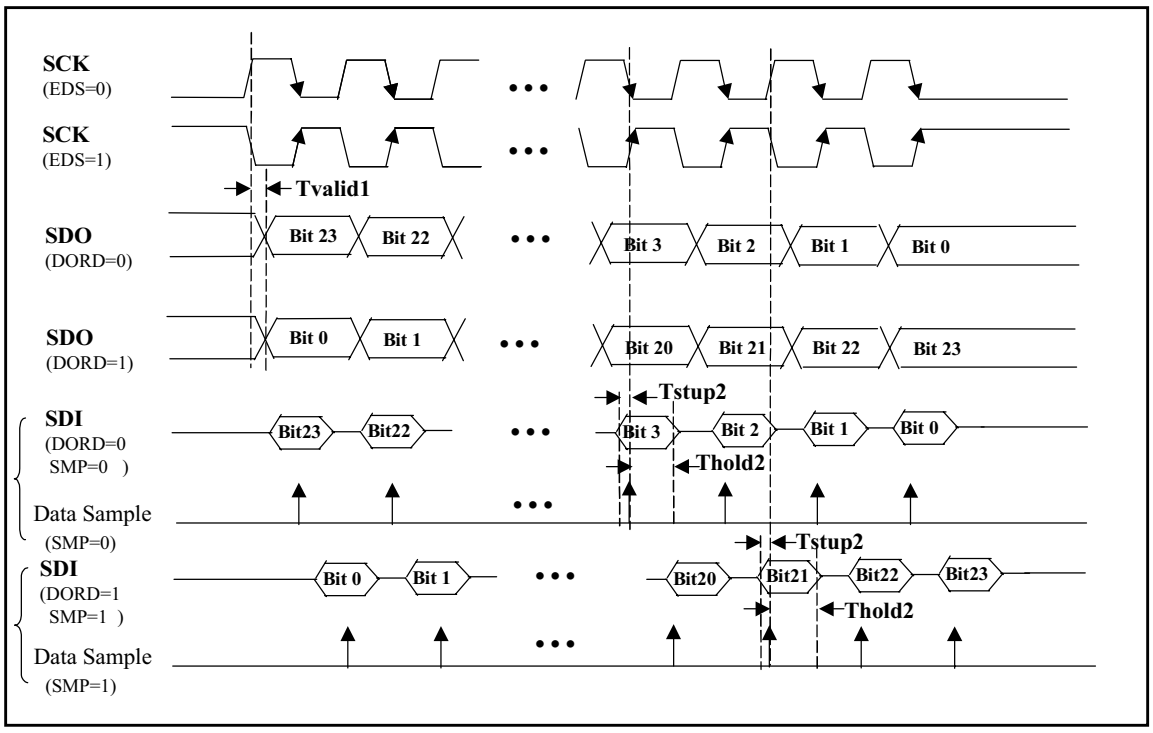
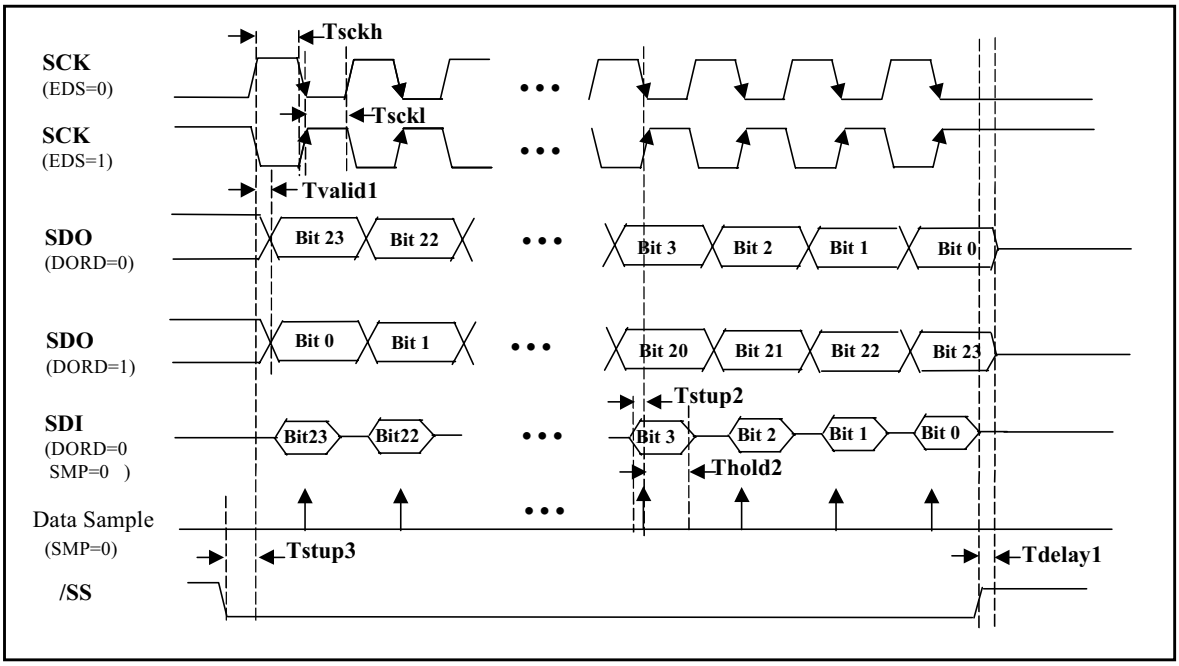
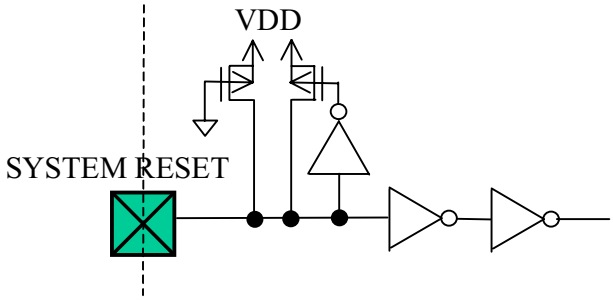


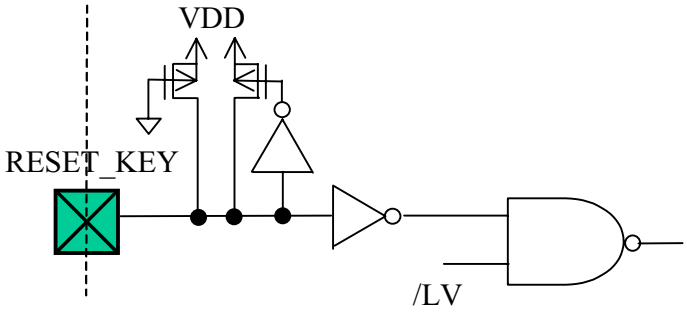
Figure VIII-4: SPI slave mode timing



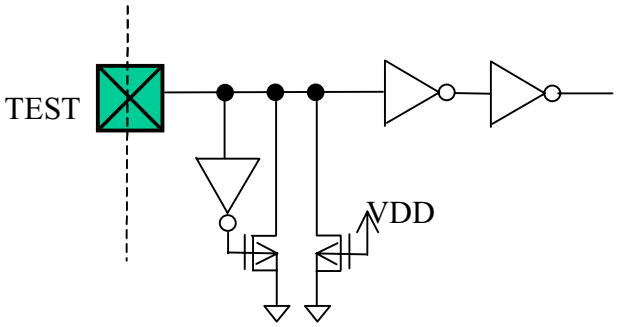
IX. Pin Type Circuit Diagrams

IX.1 Reset Pin Type

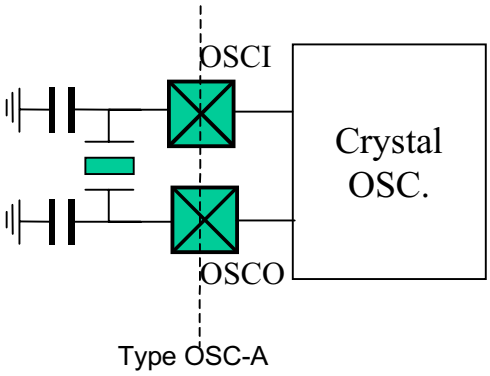


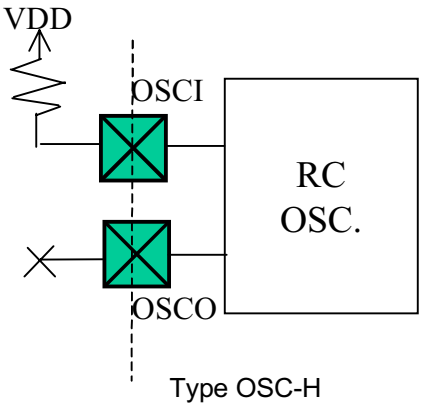


IX.2 TEST Pin Type

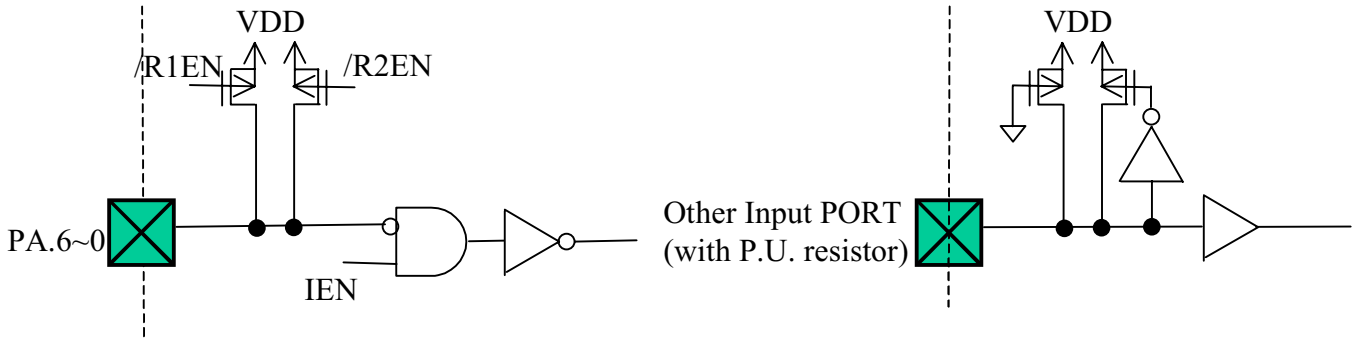


IX.3 Oscillator Pin Type

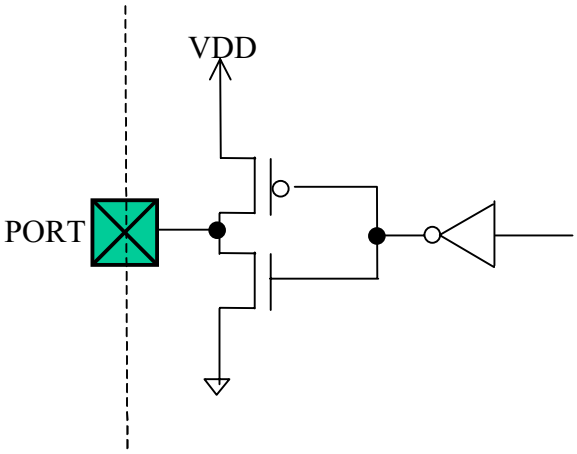




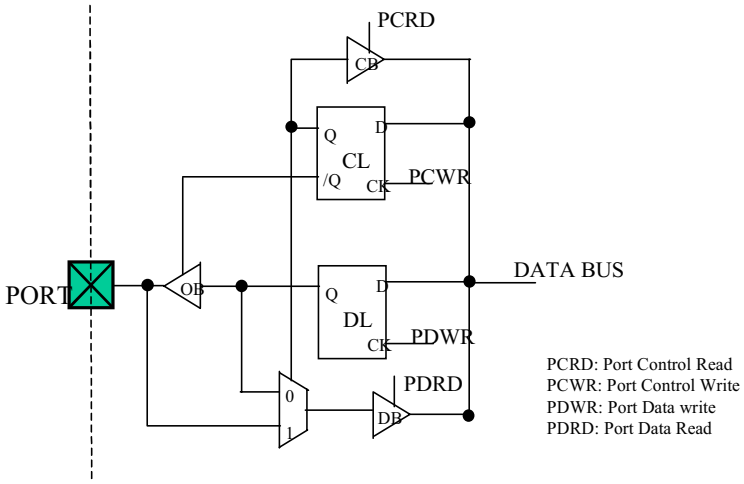
IX.4 Input Pin Type



IX.5 Output Pin Type

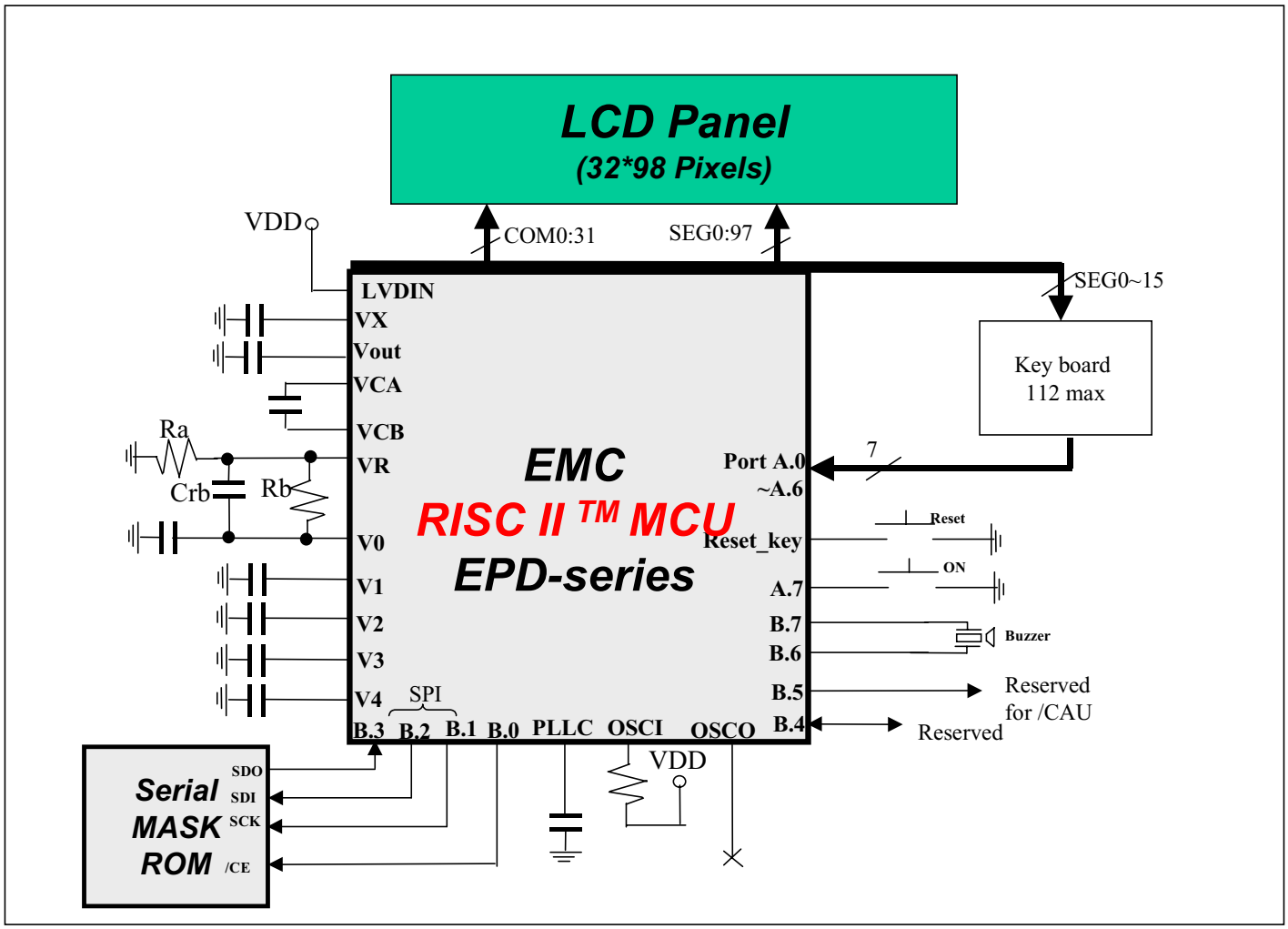


IX.6 General I/O Pin Type

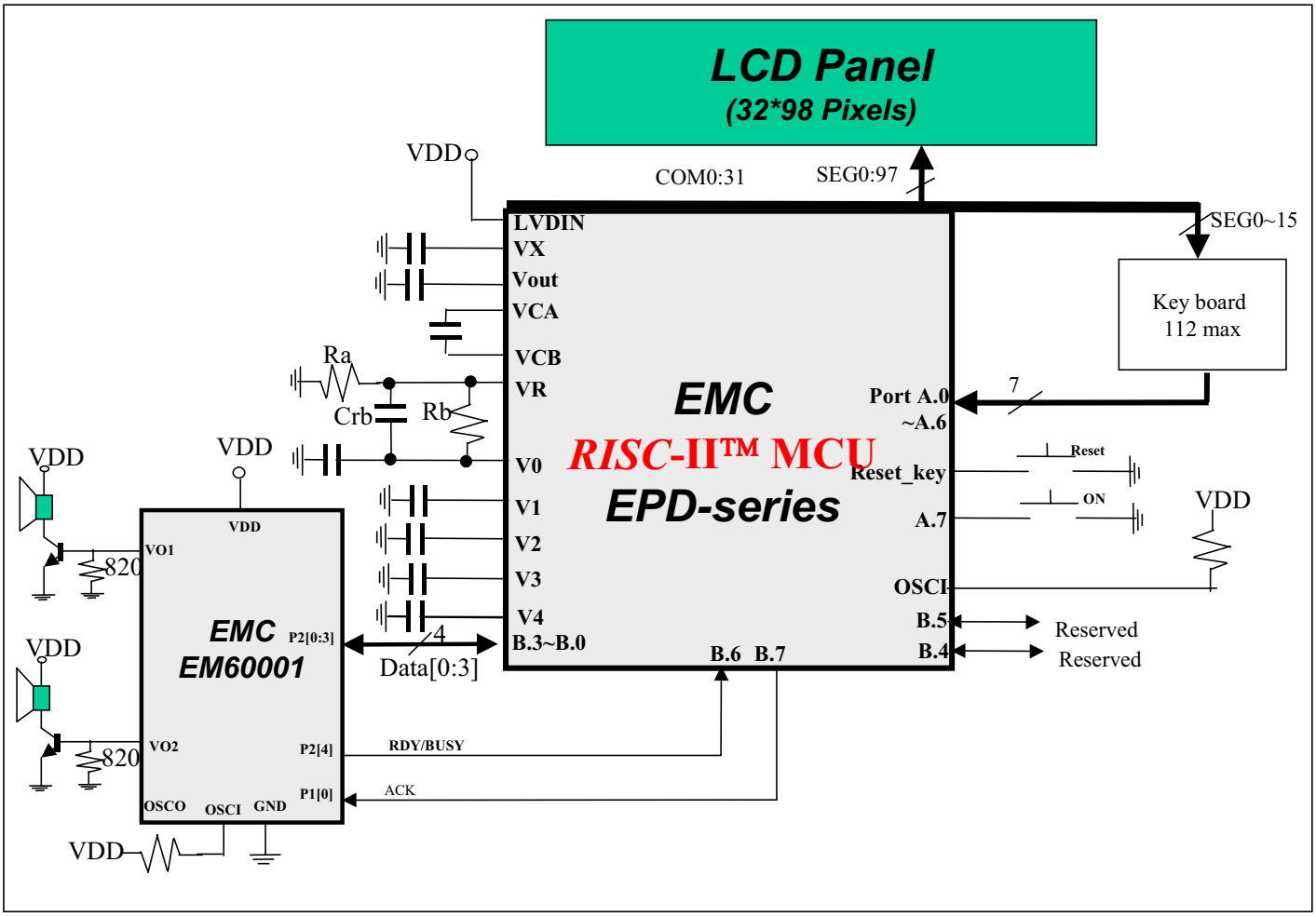


X. Application Circuit

(1)Dictionary



(2)ELA Product



XI. Instruction Set

Remark:

***k**: constant* ***r**: File Register* ***addr**: address* ***b**:bit*
***p**:special file register(0h~1Fh)* ***i**:Table pointer control*

Type	Instruction Binary	Mnemonic	Operation	Status Affected	Cycles
SYSTEM CONTROL	0000 0000 0000 0000	NOP	No operation	None	1
	0000 0000 0000 0001	WDTC	WDT ← 0 /TO←1,/PD←1	None	1
	0010 1011 1111 1110	RET	PC ← (Top of Stack)	None	1
	0010 1011 1111 1111	RETI	PC ← (Top of Stack); Enable Interrupt	None	1
	0000 0000 0000 0010	SLEP	Enter IDLE MODE if MS1=1 Enter SLEEP MODE if MS1=0	None	1
	0100 0011 kkkk kkkk	BANK #k	BSR← k	None	1
TABLE LOOK UP	0100 0000 kkkk kkkk	TBPTL #k	TABPTRL ← k	None	1
	0100 0001 kkkk kkkk	TBPTM #k	TABPTRM ← k	None	1
	0100 0010 kkkk kkkk	TBPTH #k	TABPTRH ← k	None	1
	0010 11ii rrrr rrrr	TBRD i,r	r←ROM[(TABPTR)]; (*1)(*2)	None	1 or 2 (*3)
	0010 1111 rrrr rrrr	TBRD A,r	r←ROM[(TABPTR+ACC)]; (*2)	None	1 or 2 (*3)
LOGIC	0000 0010 rrrr rrrr	OR A,r	A ← A .or. r	Z	1
	0000 0011 rrrr rrrr	OR r,A	r ← r .or. A	Z	1
	0100 0100 kkkk kkkk	OR A,#k	A ← A .or. k	Z	1
	0000 0100 rrrr rrrr	AND A,r	A ← A .and. r	Z	1
	0000 0101 rrrr rrrr	AND r,A	r ← r .and. A	Z	1
	0100 0101 kkkk kkkk	AND A,#k	A ← A .and. k	Z	1
	0000 0110 rrrr rrrr	XOR A,r	A ← A .xor. r	Z	1
	0000 0111 rrrr rrrr	XOR r,A	r ← r .xor. A	Z	1
	0100 0110 kkkk kkkk	XOR A,#k	A ← A .xor. k	Z	1
	0000 1000 rrrr rrrr	COMA r	A ← /r	Z	1
	0000 1001 rrrr rrrr	COM r	r ← /r	Z	1
	0000 1010 rrrr rrrr	RRCA r	A(n-1) ← r(n); C ← r(0);A(7) ← C	C	1
	0000 1011 rrrr rrrr	RRC r	r(n-1) ← r(n) C ← r(0), r(7) ← C	C	1
	0000 1100 rrrr rrrr	RLCA r	A(n+1) ← r(n); C ← r(7) ; A(0) ← C	C	1
LOGIC	0000 1101 rrrr rrrr	RLC r	r(n+1) ← r(n); C ← r(7) ; r(0) ← C	C	1
	0010 0010 rrrr rrrr	SHRA r	A(n-1) ← r(n) A(7) ← C	None	1
	0010 0011 rrrr rrrr	SHLA r	A(n+1) ← r(n) A(0) ← C	None	1

Compare Branch	0101 1bbb rrrr rrrr aaaa aaaa aaaa aaaa	JBC r,b,addr	If r(b)=0,jump to addr PC[15:0] ← addr (*4)	None	2
	0110 0bbb rrrr rrrr aaaa aaaa aaaa aaaa	JBS r,b,addr	If r(b)=1,jump to addr PC[15:0] ← addr (*4)	None	2
	0101 0000 rrrr rrrr aaaa aaaa aaaa aaaa	JDNZ A,r,addr	A ← r-1, jump to addr if not zero PC[15:0] ← addr (*4)	None	2
	0101 0001 rrrr rrrr aaaa aaaa aaaa aaaa	JDNZ r,addr	r ← r-1, jump to addr if not zero PC[15:0] ← addr (*4)	None	2
	0101 0010 rrrr rrrr aaaa aaaa aaaa aaaa	JINZ A,r,addr	A ← r+1,jump to addr if not zero PC[15:0] ← addr (*4)	None	2
	0101 0011 rrrr rrrr aaaa aaaa aaaa aaaa	JINZ r,addr	r ← r+1,jump to addr if not zero PC[15:0] ← addr (*4)	None	2
	0100 0111 kkkk kkkk aaaa aaaa aaaa aaaa	JGE A,#k,addr	Jump to addr if A≧k PC[15:0] ← addr (*4)	None	2
	0100 1000 kkkk kkkk aaaa aaaa aaaa aaaa	JLE A,#k,addr	Jump to addr if A≦k PC[15:0] ← addr (*4)	None	2
	0100 1001 kkkk kkkk aaaa aaaa aaaa aaaa	JE A,#k,addr	Jump to addr if A=k PC[15:0] ← addr (*4)	None	2
	0101 0101 rrrr rrrr aaaa aaaa aaaa aaaa	JGE A,r,addr	Jump to addr if A≧r PC[15:0] ← addr (*4)	None	2
	0101 0110 rrrr rrrr aaaa aaaa aaaa aaaa	JLE A,r,addr	Jump to addr if A≦r PC[15:0] ← addr (*4)	None	2
	0101 0111 rrrr rrrr aaaa aaaa aaaa aaaa	JE A,r,addr	Jump to addr if A=r PC[15:0] ← addr (*4)	None	2
PROCESS	0110 1bbb rrrr rrrr	BC r,b	r(b) ← 0	None	1
	0111 0bbb rrrr rrrr	BS r,b	r(b) ← 1	None	1
	0111 1bbb rrrr rrrr	BTG r,b	r(b) ← /r(b)	None	1
	0000 1111 rrrr rrrr	SWAP r	r(0:3)←→r(4:7)	None	1
	0000 1110 rrrr rrrr	SWAPA r	r(0:3)→A(4:7) r(4:7)→A(0:3)	None	1
	0010 0100 rrrr rrrr	CLR r	r ← 0	Z	1
	0010 0101 rrrr rrrr	TEST r	Z ← 0 if r<>0; Z ← 1 if r=0	Z	1
PROCESS	0010 0111 rrrr rrrr	RPT r	Single repeat *(r) times on next instruction *(r) is the content of register r	None	1
ARITH-METIC	0001 0000 rrrr rrrr	ADD A,r	A ← A+r	C,DC,Z, OV,SGE, SLE	1
	0001 0001 rrrr rrrr	ADD r,A	r ← r+A (*5)	C,DC,Z, OV,SGE, SLE	1
	0100 1010 kkkk kkkk	ADD A,#k	A ← A+k	C,DC,Z, OV,SGE, SLE	1

	0001 0010 rrrr rrrr	ADC A,r	A ← A+r+C	C,DC,Z, OV,SGE, SLE	1
	0001 0011 rrrr rrrr	ADC r,A	r ← r+A+C	C,DC,Z, OV,SGE, SLE	1
	0100 1011 kkkk kkkk	ADC A,#k	A ← A+k+C	C,DC,Z, OV,SGE, SLE	1
	0001 0110 rrrr rrrr	SUB A,r	A ← r-A	C,DC,Z, OV,SGE, SLE	1
	0001 0111 rrrr rrrr	SUB r,A	r ← r-A	C,DC,Z, OV,SGE, SLE	1
	0100 1100 kkkk kkkk	SUB A,#k	A ← k-A	C,DC,Z, OV,SGE, SLE	1
	0001 1000 rrrr rrrr	SUBB A,r	A ← r-A-/C	C,DC,Z, OV,SGE, SLE	1
	0001 1001 rrrr rrrr	SUBB r,A	r ← r-A-/C	C,DC,Z, OV,SGE, SLE	1
	0100 1101 kkkk kkkk	SUBB A,#k	A ← k-A-/C	C,DC,Z, OV,SGE, SLE	1
	0001 0100 rrrr rrrr	ADDDC A,r	A ← (Decimal ADD) A+r+C	C,DC,Z	1
	0001 0101 rrrr rrrr	ADDDC r,A	r ← (Decimal ADD) r+A+C	C,DC,Z	1
	0001 1010 rrrr rrrr	SUBDB A,r	A ← (Decimal SUB) r-A-/C	C,DC,Z	1
	0001 1011 rrrr rrrr	SUBDB r,A	r ← (Decimal SUB) r-A-/C	C,DC,Z	1
	0010 0110 rrrr rrrr	MUL A,r	PRODH:PRODL ← A*r	None	1
ARITH-METIC	0100 1111 kkkk kkkk	MUL A,#k	PRODH:PRODL ← A*k	None	1
	0001 1100 rrrr rrrr	INCA r	A ← r+1	C,Z	1
	0001 1101 rrrr rrrr	INC r	r ← r+1	C,Z	1
	0001 1110 rrrr rrrr	DECA r	A ← r-1	C,Z	1
	0001 1111 rrrr rrrr	DEC r	r← r-1	C,Z	1
Move	0010 0000 rrrr rrrr	MOV A,r	A←r	Z	1
	0010 0001 rrrr rrrr	MOV r,A	r←A	None	1
	100p pppp rrrr rrrr	MOVRP p,r	Register p ← Register r	None	1
	101p pppp rrrr rrrr	MOVPR r,p	Register r ← Register p	None	1
	0100 1110 kkkk kkkk	MOV A,#k	A← k	None	1
Branch	110a aaaa aaaa aaaa	SJMP addr	PC ← addr PC[13..16] unchange	None	1
	0011 aaaa aaaa aaaa	S0CALL addr	Top of Stack]←PC+1 PC[11:0] ← addr PC[12:16] ← 00000 (*6)	None	1

	111a aaaa aaaa aaaa	SCALL addr	[Top of Stack]←PC+1 PC[12:0] ← addr PC[13:16] unchange	None	1
	0000 0000 0010 aaaa aaaa aaaa aaaa aaaa	LJMP addr (2 words)	PC ← addr	None	2
	0000 0000 0011 aaaa aaaa aaaa aaaa aaaa	LCALL addr (2 words)	[Top of Stack]←PC+1 PC ← addr	None	2

(*1) TBRD i,r :

r← ROM[(TABPTR)];

i=00: TABPTR not change

i=01: TABPTR←TABPTR+1

i=10: TABPTR←TABPTR-1

(*2) TABPTR=(TABPTRH:TABPTRM:TABPTRL).

*Bit 7 of TABPTRH use to select internal ROM space or external memory space.

Bit7=0: internal ROM space

Bit7=1:external memory space.

*Bit 0 of TABPTRL use to select low byte or high byte of pointed ROM data.

Bit0=0: Low byte of pointed ROM data

Bit0=1:High byte of pointed ROM data.

*The maximum table look up space is internal 8Mbytes and external 8Mbytes.

(*3) **TBRD** instruction will take 2 cycles at first time, and then 1 cycle at following **TBRD** instructions.

Ex1. TBRD 1,reg1 ➔ **Take 2 cycles**

TBRD 1,reg2 ➔ Take 1 cycle

TBRD 1,reg3 ➔ Take 1 cycle

.....

TBRD 1,reg99 ➔ Take 1 cycle

NOP

TBRD 1,reg100 ➔ **Take 2 cycles**

TBRD 1,reg101 ➔ Take 1 cycle

Ex2. MOV A,#10

RPT ACC

TBRD 1,INDF1 ➔ Repeat 10 times, total take 11 cycles

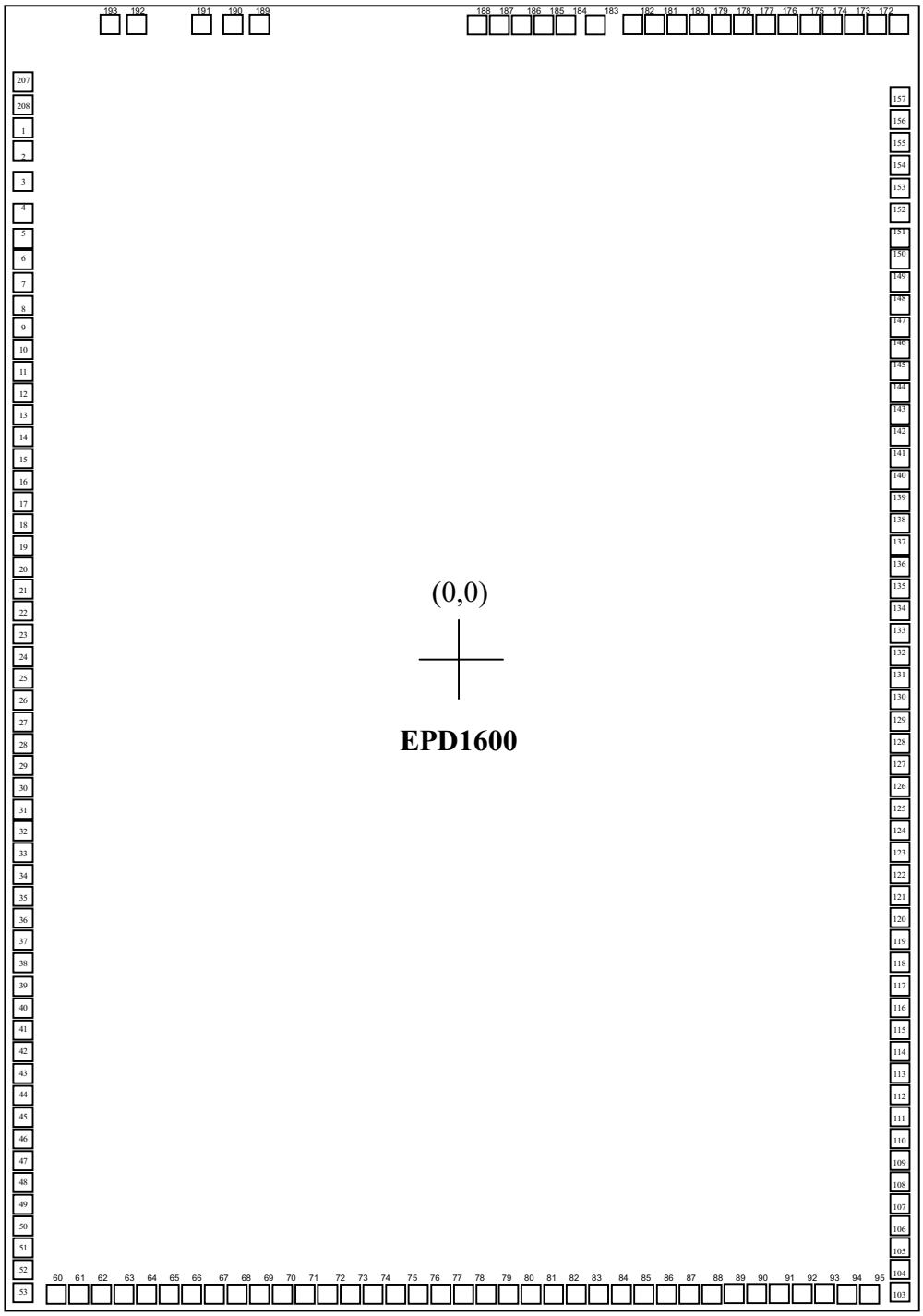
(*4)The maximum jump range is 64K absolute address, means only can jump within the same 64K range, i.e. 0~64K or 64K~128K.

(*5)Carry bit of ADD PCL,A or ADD TABPTRL,A will automatic carry into PCH or TABPTR.

The Instruction cycle of write to PC(program counter) takes TWO cycle.

(*6) S0CALL addressing ability is from 0x000 to 0xFFF(4K space).

XII. Pad Diagram



Pin NO.	Symbol	X	Y	Pin NO.	Symbol	X	Y
1	V4	-2060.0	2516.3	41	SEG81	-2060.0	-1825.0
2	VR	-2060.0	2406.3	42	SEG80	-2060.0	-1930.0
3	V0	-2060.0	2264.5	43	SEG79	-2060.0	-2035.0
4	VOUT	-2060.0	2095.2	44	SEG78	-2060.0	-2140.0
5	V1	-2060.0	1955.0	45	SEG77	-2060.0	-2245.0
6	V2	-2060.0	1850.0	46	SEG76	-2060.0	-2350.0
7	V3	-2060.0	1745.0	47	SEG75	-2060.0	-2455.0
8	VCB	-2060.0	1640.0	48	SEG74	-2060.0	-2560.0
9	COM31	-2060.0	1535.0	49	SEG73	-2060.0	-2665.0
10	COM30	-2060.0	1430.0	50	SEG72	-2060.0	-2775.0
11	COM29	-2060.0	1325.0	51	SEG71	-2060.0	-2885.0
12	COM28	-2060.0	1220.0	52	SEG70	-2060.0	-2995.0
13	COM27	-2060.0	1115.0	53	SEG69	-2060.0	-3105.0
14	COM26	-2060.0	1010.0	54	NC		
15	COM25	-2060.0	905.0	55	NC		
16	COM24	-2060.0	800.0	56	NC		
17	COM23	-2060.0	695.0	57	NC		
18	COM22	-2060.0	590.0	58	NC		
19	COM21	-2060.0	485.0	59	NC		
20	COM20	-2060.0	380.0	60	SEG68	-1915.0	-3105.0
21	COM19	-2060.0	275.0	61	SEG67	-1805.0	-3105.0
22	COM18	-2060.0	170.0	62	SEG66	-1695.0	-3105.0
23	COM17	-2060.0	65.0	63	SEG65	-1585.0	-3105.0
24	COM16	-2060.0	-40.0	64	SEG64	-1475.0	-3105.0
25	SEG97	-2060.0	-145.0	65	SEG63	-1365.0	-3105.0
26	SEG96	-2060.0	-250.0	66	SEG62	-1260.0	-3105.0
27	SEG95	-2060.0	-355.0	67	SEG61	-1155.0	-3105.0
28	SEG94	-2060.0	-460.0	68	SEG60	-1050.0	-3105.0
29	SEG93	-2060.0	-565.0	69	SEG59	-945.0	-3105.0
30	SEG92	-2060.0	-670.0	70	SEG58	-840.0	-3105.0
31	SEG91	-2060.0	-775.0	71	SEG57	-735.0	-3105.0
32	SEG90	-2060.0	-880.0	72	SEG56	-630.0	-3105.0
33	SEG89	-2060.0	-985.0	73	SEG55	-525.0	-3105.0
34	SEG88	-2060.0	-1090.0	74	SEG54	-420.0	-3105.0
35	SEG87	-2060.0	-1195.0	75	SEG53	-315.0	-3105.0
36	SEG86	-2060.0	-1300.0	76	SEG52	-210.0	-3105.0
37	SEG85	-2060.0	-1405.0	77	SEG51	-105.0	-3105.0
38	SEG84	-2060.0	-1510.0	78	SEG50	0.0	-3105.0
39	SEG83	-2060.0	-1615.0	79	SEG49	105.0	-3105.0
40	SEG82	-2060.0	-1720.0	80	SEG48	210.0	-3105.0

Pin NO.	Symbol	X	Y	Pin NO.	Symbol	X	Y
81	SEG47	315.0	-3105.0	121	SEG13	2060.0	-1195.0
82	SEG46	420.0	-3105.0	122	SEG12	2060.0	-1090.0
83	SEG45	525.0	-3105.0	123	SEG11	2060.0	-985.0
84	SEG44	630.0	-3105.0	124	SEG10	2060.0	-880.0
85	SEG43	735.0	-3105.0	125	SEG9	2060.0	-775.0
86	SEG42	840.0	-3105.0	126	SEG8	2060.0	-670.0
87	SEG41	945.0	-3105.0	127	SEG7	2060.0	-565.0
88	SEG40	1050.0	-3105.0	128	SEG6	2060.0	-460.0
89	SEG39	1155.0	-3105.0	129	SEG5	2060.0	-355.0
90	SEG38	1260.0	-3105.0	130	SEG4	2060.0	-250.0
91	SEG37	1365.0	-3105.0	131	SEG3	2060.0	-145.0
92	SEG36	1475.0	-3105.0	132	SEG2	2060.0	-40.0
93	SEG35	1585.0	-3105.0	133	SEG1	2060.0	65.0
94	SEG34	1695.0	-3105.0	134	SEG0	2060.0	170.0
95	SEG33	1805.0	-3105.0	135	COM0	2060.0	275.0
96	SEG32	1915.0	-3105.0	136	COM1	2060.0	380.0
97	NC			137	COM2	2060.0	485.0
98	NC			138	COM3	2060.0	590.0
99	NC			139	COM4	2060.0	695.0
100	NC			140	COM5	2060.0	800.0
101	NC			141	COM6	2060.0	905.0
102	NC			142	COM7	2060.0	1010.0
103	SEG31	2060.0	-3105.0	143	COM8	2060.0	1115.0
104	SEG30	2060.0	-2995.0	144	COM9	2060.0	1220.0
105	SEG29	2060.0	-2885.0	145	COM10	2060.0	1325.0
106	SEG28	2060.0	-2775.0	146	COM11	2060.0	1430.0
107	SEG27	2060.0	-2665.0	147	COM12	2060.0	1535.0
108	SEG26	2060.0	-2560.0	148	COM13	2060.0	1640.0
109	SEG25	2060.0	-2455.0	149	COM14	2060.0	1745.0
110	SEG24	2060.0	-2350.0	150	COM15	2060.0	1850.0
111	SEG23	2060.0	-2245.0	151	PA.0	2060.0	1962.5
112	SEG22	2060.0	-2140.0	152	PA.1	2060.0	2082.5
113	SEG21	2060.0	-2035.0	153	PA.2	2060.0	2202.5
114	SEG20	2060.0	-1930.0	154	PA.3	2060.0	2322.5
115	SEG19	2060.0	-1825.0	155	PA.4	2060.0	2442.5
116	SEG18	2060.0	-1720.0	156	PA.5	2060.0	2562.5
117	SEG17	2060.0	-1615.0	157	PA.6	2060.0	2682.5
118	SEG16	2060.0	-1510.0	158	NC		
119	SEG15	2060.0	-1405.0	159	NC		
120	SEG14	2060.0	-1300.0	160	NC		

Pin NO.	Symbol	X	Y
161	NC		
162	NC		
163	NC		
164	NC		
165	NC		
166	NC		
167	NC		
168	NC		
169	NC		
170	PA.7	2050.9	3105.0
171	CLKO	1930.9	3105.0
172	PB.0	1810.8	3105.0
173	PB.1	1690.9	3105.0
174	PB.2	1570.8	3105.0
175	PB.3	1450.9	3105.0
176	PB.4	1330.9	3105.0
177	PB.5	1210.8	3105.0
178	PB.6	1090.8	3105.0
179	PB.7	970.9	3105.0
180	RESET_KEY	850.9	3105.0
181	SYSTEM RESET	730.9	3105.0
182	VDD	610.9	3105.0
183	LVDIN	440.5	3105.0
184	(reserved)	308.5	3105.0
185	(reserved)	188.5	3105.0

Pin NO.	Symbol	X	Y
186	(reserved)	68.5	3105.0
187	(reserved)	-51.5	3105.0
188	(reserved)	-171.5	3105.0
189	PLLC	-974.7	3105.0
190	GND	-1094.7	3105.0
191	OSCI	-1234.7	3105.0
192	OSCO	-1545.6	3105.0
193	TEST	-1665.6	3105.0
194	NC		
195	NC		
196	NC		
197	NC		
198	NC		
199	NC		
200	NC		
201	NC		
202	NC		
203	NC		
204	NC		
205	NC		
206	NC		
207	VCA	-2060.0	2736.3
208	VX	-2060.0	2626.3

Note: Pad 184 ~ Pad 188 is for factory test only. Please do NOT bonding these pads on application circuit.

Chip size : 4390 * 6480 um

For PCB layout, IC substrate must be connected to VSS.