High Efficiency Linear Power Supply with Accurate Power Surveillance and Software Monitoring

Features

- Highly accurate 5 V, 100 mA guaranteed output
- Low dropout voltage, typically 380 mV at 100 mA
- Low quiescent current, typically 155 μA
- Standby mode, maximum current 340 μA (with 100 μA load on OUTPUT)
- Unregulated DC input can withstand -20 V reverse battery and +60 V power transients
- Fully operational for unregulated DC input voltage up to 26 V and regulated output voltage down to 3.0 V
- Reset output guaranteed for regulated output voltage down to 1.2 V
- No reverse output current
- Very low temperature coefficient for the regulated output
- Current limiting
- Comparator for voltage monitoring, voltage reference 1.17V
- ±2.2% voltage reference accuracy at +25°C
- ±4.2% voltage reference accuracy from -40 to +85°C
- Programmable reset voltage monitoring
- Programmable power on reset (POR) delay
- Watchdog with programmable time windows guarantees a minimum time and a maximum time between software clearing of the watchdog
- Time base accuracy ±10%
- System enable output offers added security
- TTL/CMOS compatible
- -40 to +85°C temperature range
- DIP8 and SO8 packages

Description

The A6130 offers a high level of integration by combining voltage regulation, voltage monitoring and software monitoring in an 8 lead package. The voltage regulator has a low dropout voltage (typ. 380 mV at 100 mA) and a low quiescent current (155 μA). The quiescent current increases only slightly in dropout prolonging battery life. Built-in protection includes a positive transient absorber for up to 60 V (load dump) and the ability to survive an unregulated input voltage of -20 V (reverse battery). The input may be connected to ground or a reverse voltage without reverse current flow from the output to the input. A comparator monitors the voltage applied at the V_{IN} input comparing it with an internal 1.17 V reference. The power-on reset function is initialized after V_{IN} reaches 1.17 V and takes the reset output inactive after T_{POR} depending of external resistance. The reset output goes active low when the V_{IN} voltage is less than 1.17 V. The $\overline{RES}$ and $\overline{EN}$ outputs are guaranteed to be in a correct state for a regulated output voltage as low as 1.2 V. The watchdog function monitors software cycle time and execution. If software clears the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. The system enable output prevents critical control functions being activated until software has successfully cleared the watchdog three times. Such a security could be used to prevent motor controls being energized on repeated resets of a faulty system.

Applications

- Industrial electronics
- Cellular telephones
- Security systems
- Battery powered products
- High efficiency linear power supplies
- Automotive electronics

Typical Operating Configuration

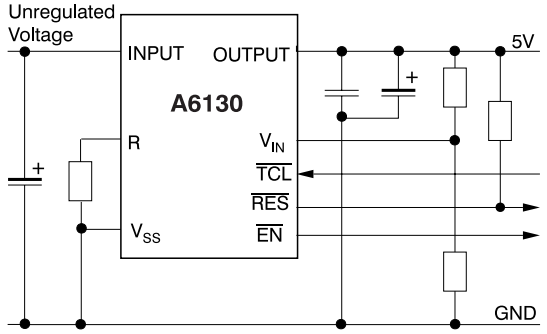


Fig. 1

Pin Assignment

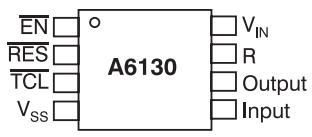


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Continuous voltage at INPUT to V_{SS}	V_{INPUT}	-0.3 to +30 V
Transients on INPUT for t< 100 ms and duty cycle 1%	V_{TRANS}	up to +60 V
Reverse supply voltage on INPUT	V_{REV}	-20 V
Max. voltage at any signal pin	V_{MAX}	OUTPUT+0.3V
Min. voltage at any signal pin	V_{MIN}	V_{SS}-0.3V
Storage temperature	T_{STO}	-65 to +150°C
Electrostatic discharge max. To MIL-STD-883C method 3015	V_{Smax}	1000V
Max. soldering conditions	T_{Smax}	250°C x 10 s

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. At any time, all inputs must be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating junction temperature[1]	T_J	-40	+85	°C
INPUT voltage [2]	V_{INPUT}	2.3	26	V
OUTPUT voltage [2] [3]	V_{OUTPUT}	1.2		V
$\overline{RES}$ & $\overline{EN}$ guaranteed [4]	V_{OUTPUT}	1.2		V
OUTPUT current [5]	I_{OUTPUT}		100	mA
Comparator input voltage	V_{IN}	0	V_{OUTPUT}	V
RC-oscillator programming	R	10	1000	kΩ
Thermal resistance from junction to ambient [6]				
- DIP8	$R_{th(j-a)}$		105	°C/W
- SO8	$R_{th(j-a)}$		160	°C/W

Table 2

[1] The maximum operating temperature is confirmed by sampling at initial device qualification. In production, all devices are tested at +85°C.

[2] Full operation guaranteed. To achieve the load regulation specified in Table 3 a 22 μF capacitor or greater is required on the INPUT, see Fig. 8. The 22 μF must have an effective resistance $\leq$ 5 Ω and a resonant frequency above 500 kHz.

[3] A 10 μF load capacitor and a 100 nF decoupling capacitor are required on the regulator OUTPUT for stability. The 10 μF must have an effective series resistance of $\leq$ 5 Ω and a resonant frequency above 500 kHz.

[4] $\overline{RES}$ must be pulled up externally to V_{OUTPUT} even if it is unused. (Note: $\overline{RES}$ and $\overline{EN}$ are used as inputs by EM test.)

[5] The OUTPUT current will not apply for all possible combinations of input voltage and output current. Combinations that would require the A6130 to work above the maximum junction temperature (+85°C) must be avoided.

[6] The thermal resistance specified assumes the package is soldered to a PCB.

Electrical Characteristics

V_{INPUT} = 6.0 V, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply current in standby mode	I_{SS}	R_{EXT} = don't care, TCL = V_{OUTPUT}, V_{IN} = 0 V, I_L = 100 µA			340	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, O/Ps 1 MΩ to V_{OUTPUT}, I_L = 100 µA		155	400	µA
Supply current [1]	I_{SS}	R_{EXT} = 100 kΩ, I/Ps at V_{OUTPUT}, V_{INPUT} = 8.0 V, O/Ps 1MΩ to V_{OUTPUT}, I_L = 100 mA		1.7	4.2	mA
Output voltage	V_{OUTPUT}	I_L = 100 µA	4.88		5.12	V
Output voltage	V_{OUTPUT}	100 µA ≤ I_L ≤ 100 mA, -40°C ≤ T_J ≤ +85°C	4.85		5.15	V
Output voltage temperature coefficient [2]	$V_{th(coeff)}$			50	180	ppm/°C
Line regulation [3]	V_{LINE}	6 V ≤ V_{INPUT} ≤ 26 V, I_L = 1 mA, T_J = +85°C		0.2	0.5	%
Load regulation [3]	V_L	100 µA ≤ I_L ≤ 100 mA		0.2	0.6	%
Dropout voltage[4]	$V_{DROPOUT}$	I_L = 100 µA		40	170	mV
Dropout voltage[4]	$V_{DROPOUT}$	I_L = 100 µA		380		mV
Dropout voltage[4]	$V_{DROPOUT}$	I_L = 100 mA, -40°C ≤ T_J ≤ +85°C			650	mV
Dropout supply current	I_{SS}	V_{INPUT} = 4.5 V, I_L = 100 µA, R_{EXT} = 100 kΩ, O/Ps 1 MΩ to V_{OUTPUT}, I/Ps at V_{OUTPUT}		1.2	1.6	mA
Thermal regulation [5]	V_{thr}	T_J = +25°C, I_L = 50 mA, V_{INPUT} = 26 V, T = 10 ms		0.05	0.25	%/W
Current limit	I_{Lmax}	OUTPUT tied to V_{SS}		450		mA
OUTPUT noise, 10 Hz to 100kHz	V_{NOISE}			200		µV rms

3.0 ≤ V_{OUTPUT} ≤ 5.5 V, I_L = 100 µA. C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = -40 to +85°C, unless otherwise specified

$\overline{RES}$ and $\overline{EN}$						
Output Low Voltage	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 20 mA		0.4		V
	V_{OL}	V_{OUTPUT} = 4.5 V, I_{OL} = 8 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 2.0 V, I_{OL} = 4 mA		0.2	0.4	V
	V_{OL}	V_{OUTPUT} = 1.2 V, I_{OL} = 0.5 mA		0.06	0.2	V
$\overline{EN}$						
Output High Voltage	V_{OH}	V_{OUTPUT} = 4.5 V, I_{OH} = -1 mA	3.5	4.1		V
	V_{OH}	V_{OUTPUT} = 2.0 V, I_{OH} = -100 µA	1.8	1.9		V
	V_{OH}	V_{OUTPUT} = 1.2 V, I_{OH} = -30 µA	1.0	1.1		V
$\overline{TCL}$ and V_{IN}						
$\overline{TCL}$ Input Low Level	V_{IL}		V_{SS}		0.8	V
$\overline{TCL}$ Input High Level	V_{IH}		2.0		V_{OUTPUT}	V
Leakage current $\overline{TCL}$ input	I_{LI}	V_{SS} ≤ V_{TCL} ≤ V_{OUTPUT}		0.05	1	µA
V_{IN} input resistance	R_{VIN}			100		MΩ
Comparator reference [6][7]	V_{REF}	T_J = +25°C	1.148	1.170	1.200	V
	V_{REF}	20°C ≤ T_J ≤ +70°C	1.123		1.218	V
	V_{REF}		1.123		1.222	V
Comparator hysteresis [7]	V_{HY}			2		mV

Table 3

[1] If INPUT is connected to V_{SS}, no reverse current will flow from the OUTPUT to the INPUT, however the supply current specified will be sank by the OUTPUT to supply the A6130.

[2] The OUTPUT voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

[3] Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in OUTPUT voltage due to heating effects are covered in the specification for thermal regulation.

[4] The dropout voltage is defined as the INPUT to OUTPUT differential, measured with the input voltage equal to 5.0 V.

[5] Thermal regulation is defined as the change in OUTPUT voltage at a time T after a change in power dissipation is applied, excluding load or line regulation effects.

[6] The comparator and the voltage regulator have separate voltage references (see Block Diagram Fig. 7).

[7] The comparator reference is the power-down reset threshold. The power-on reset threshold equals the comparator reference voltage plus the comparator hysteresis (see Fig. 4).

Timing Characteristics

V_{INPUT} = 6.0 V, I_L = 100 µA, C_L = 10 µF + 100 nF, C_{INPUT} = 22 µF, T_J = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays:						
$\overline{TCL}$ to Output Pins	T_{DIDO}			250	500	ns
V_{IN} sensitivity	T_{SEN}		1	5	20	µs
Logic Transition Times on all Output Pins	T_{TR}	Load 10 kΩ, 50 pF		30	100	ns
Power-on Reset delay	T_{POR}	R_{EXT} = 118 kΩ, ± 1%	90	100	110	ms
Watchdog Time	T_{WD}	R_{EXT} = 118 kΩ, ± 1%	90	100	110	ms
Open Window Percentage	OWP			±0.2 T_{WD}		
Closed Window Time	T_{CW}			0.8 T_{WD}		
	T_{CW}	R_{EXT} = 118 kΩ, ± 1%	72	80	88	ms
Open Window Time	T_{OW}			0.4 T_{WD}		
	T_{OW}	R_{EXT} = 118 kΩ, ± 1%	36	40	44	ms
Watchdog Reset Pulse	T_{WDR}			T_{WD} / 40		
	T_{WDR}	R_{EXT} = 118 kΩ, ± 1%		2.5		ms
T_{CL} Input Pulse Width	T_{TCL}		150			ns

Table 4

Timing Waveforms

Watchdog Timeout Period

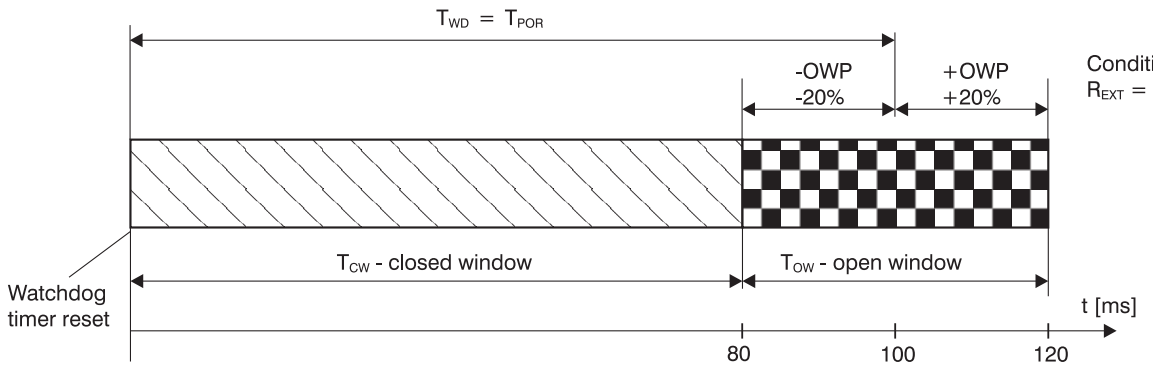
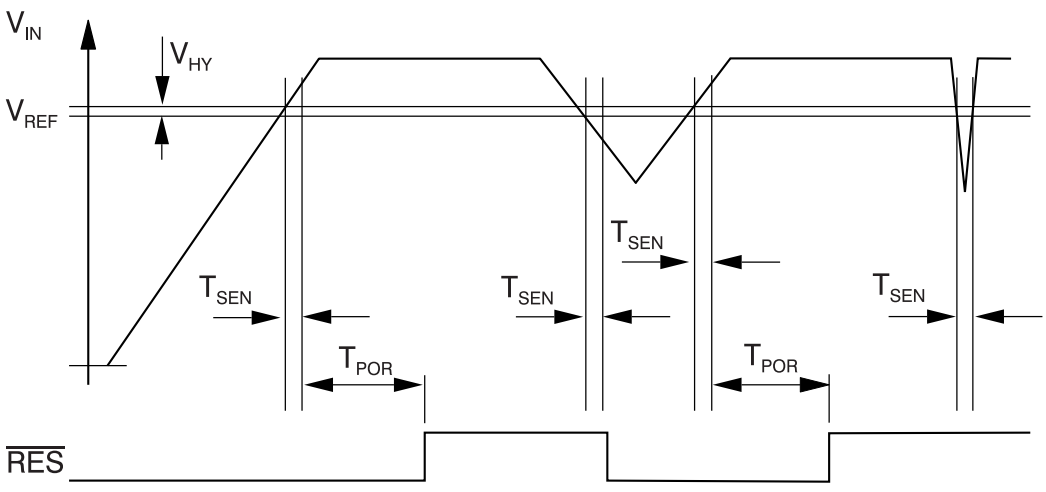


Fig. 3

Voltage Monitoring



Conditions:
V_{OUTPUT} ≥ 3 V
no timeout

Fig. 4

Timer Reaction

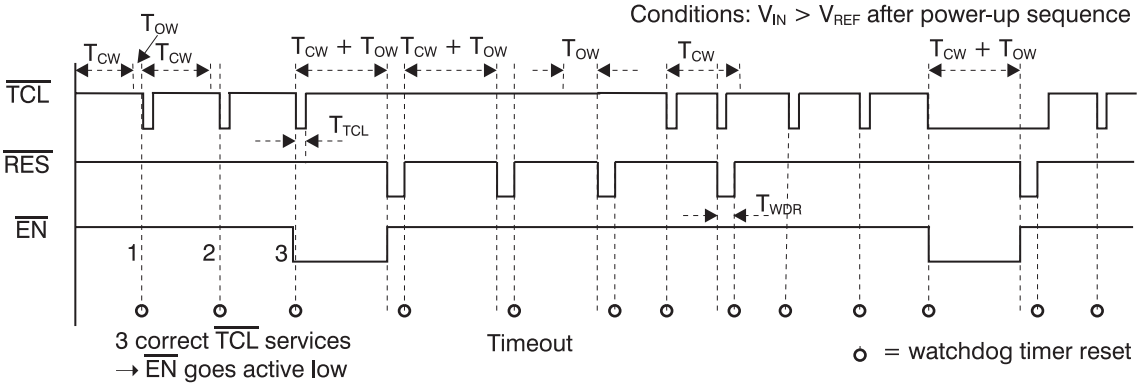


Fig. 5

Combined Voltage and Timer Reaction

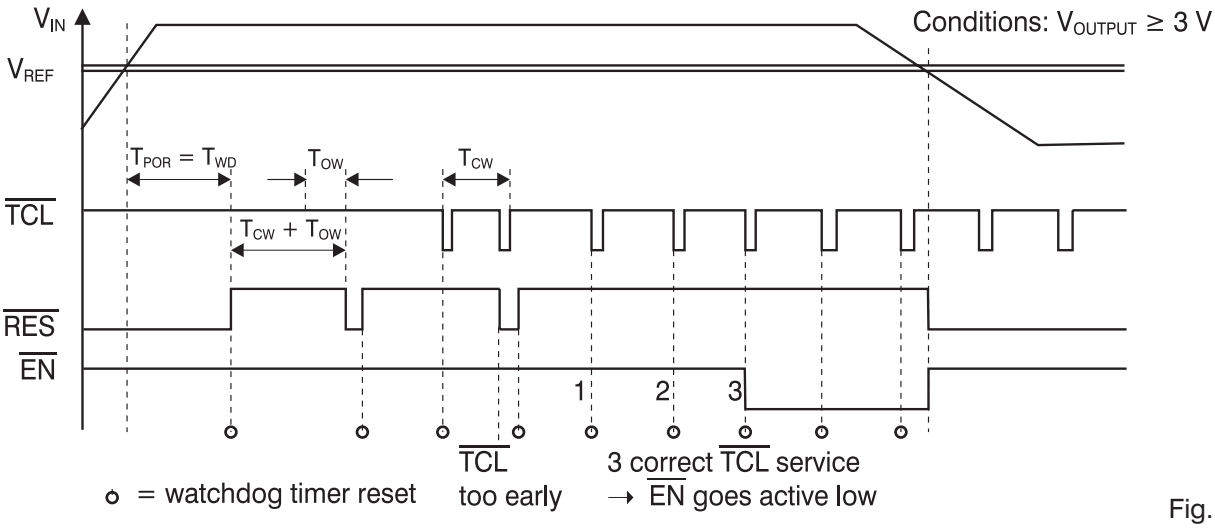


Fig. 6

Block Diagram

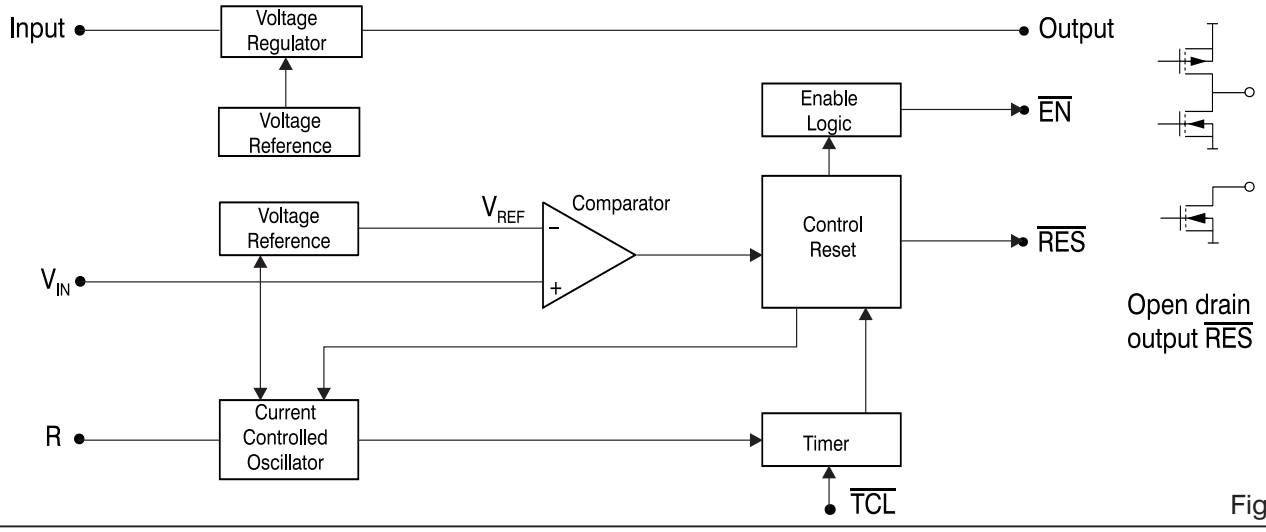


Fig. 7

Pin Description

Pin	Name	Function
1	$\overline{EN}$	Push-pull active low enable output
2	$\overline{RES}$	Open drain active low reset output. $\overline{RES}$ must be pulled up to V_{OUTPUT} even if unused
3	$\overline{TCL}$	Watchdog timer clear input signal
4	V_{SS}	GND terminal
5	INPUT	Voltage regulator input
6	OUTPUT	Voltage regulator output
7	R	R_{EXT} input for RC oscillator tuning
8	V_{IN}	Voltage comparator input

Table 5

Functional Description

Voltage Regulator

The A6130 has a 5 V ± 2%, 100 mA, low dropout voltage regulator. The low supply current (typ. 155 μA) makes the A6130 particularly suited to automotive systems then remain energized 24 hours a day. The input voltage range is 2.3 V to 26 V for operation and the input protection includes both reverse battery (20 V below ground) and load dump (positive transients up to 60 V). There is no reverse current flow from the OUTPUT to the INPUT when the INPUT equals V_{SS}. This feature is important for systems which need to implement (with capacitance) a minimum power supply hold-up time in the event of power failure. To achieve good load regulation a 22 μF capacitor (or greater) is needed on the INPUT (see Fig. 8). Tantalum or aluminium electrolytics are adequate for the 22 μF capacitor; film types will work but are relatively expensive. Many aluminium electrolytics have electrolytes that freeze at about -30°C, so tantalums are recommended for operation below -25°C. The important parameters of the 22 μF capacitor are an effective series re sistance of ≤ 5 Ω and a resonant frequency above 500 kHz.

A 10 μF capacitor (or greater) and a 100 nF capacitor are required on the OUTPUT to prevent oscillations due to instability. The specification of the 10 μF capacitor is as per the 22 μF capacitor on the INPUT (see previous paragraph).

The A6130 will remain stable and in regulation with no external load and the dropout voltage is typically constant as the input voltage fall to below its minimum level (see Table 2). These features are especially important in CMOS RAM keep-alive applications.

Care must be taken not to exceed the maximum junction temperature (+85°C). The power dissipation within the A6130 is given by the formula:

$$P_{TOTAL} = (V_{INPUT} - V_{OUTPUT}) \cdot I_{OUTPUT} + (V_{INPUT}) \cdot I_{SS}$$

The maximum continuous power dissipation at a given temperature can be calculated using the formula:

$$P_{MAX} = (85°C - T_A) / R_{th(j-a)}$$

where $R_{th(j-a)}$ is the thermal resistance from the junction to the ambient and is specified in Table 2. Note the $R_{th(j-a)}$ given in Table 2 assumes that the package is soldered to a PCB. The above formula for maximum power dissipation assumes a constant load (ie. ≥ 100 s). The transient thermal resistance for a single pulse is much lower than the continuous value. For example the A6130 in DIP8 package will have an effective thermal resistance from the junction to the ambient of about 10°C/W for a single 100 ms pulse.

V_{IN} Monitoring

The power-on reset and the power-down reset are generated as a response to the external voltage level applied on the V_{IN} input. The V_{DD} voltage at which reset is asserted or released is determined by the external voltage divider between V_{DD} and V_{SS}, as shown on Fig. 8. A part of V_{DD} is compared to the internal voltage reference. To determine the values of the divider, the leakage current at V_{IN} must be taken into account, as well as the current consumption of the divider itself. Low resistor values will need more current, but high resistor values will make the reset threshold less accurate at high temperature, due to a possible leakage current at the V_{IN} input. The sum of the two resistors should stay below 300 kΩ. The formula is:

$$V_{RESET} = V_{REF} * (1 + R_1/R_2).$$

Example: choosing R_1 = 100 kΩ and R_2 = 36 kΩ will result in a V_{DD} reset threshold of 4.42 V (typ.).

At power-up the reset output ($\overline{RES}$) is held low (see Fig. 4). After INPUT reaches 3.36 V (and so OUTPUT reaches at least 3 V) and V_{IN} becomes greater than V_{REF}, the $\overline{RES}$ output is held low for an additional power-on-reset (POR) delay which is equal to the watchdog time T_{WD} (typically 100 ms with an external resistor of 118 kΩ connected at R pin). The POR delay prevents repeated toggling of $\overline{RES}$ even if V_{IN} and the INPUT voltage drops out and recovers. The POR delay allows the microprocessor's crystal oscillator time to start and stabilize and ensures correct recognition of the reset signal to the microprocessor.

The $\overline{RES}$ output goes active low generating the power-down reset whenever V_{IN} falls below V_{REF}. The sensitivity or reaction time of the internal comparator to the voltage level on V_{IN} is typically 5 μs.

Timer Programming

The on-chip oscillator with an external resistor R_{EXT} connected between the R pin and V_{SS} (see Fig. 8) allows the user to adjust the power-on reset (POR) delay, watchdog time T_{WD} and with this also the closed and open time windows as well as the watchdog reset pulse width (T_{WD} / 40).

With R_{EXT} = 118 kΩ typical values are:

- Power-on reset delay: T_{POR} is 100 ms
- Watchdog time: T_{WD} is 100 ms
- Closed window: T_{CW} is 80 ms
- Open window: T_{OW} is 40 ms
- Watchdog reset: T_{WDR} is 2.5 ms

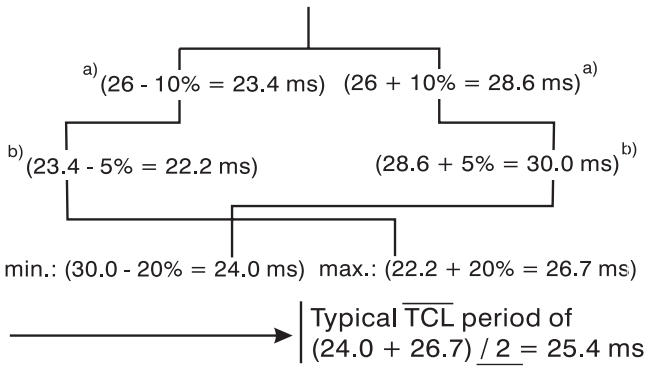
Note: the current consumption increases as the frequency increases.

Watchdog Timeout Period Description

The watchdog timeout period is divided into two parts, a "closed" window and an "open" window (see Fig. 3) and is defined by two parameters, T_{WD} and the Open Window Percentage (OWP). The closed window starts just after

the watchdog timer resets and is defined by $T_{CW} = T_{WD}$ - OWP(T_{WD}).The open window starts after the closed time window finishes and lasts till T_{WD} + OWP(T_{WD}). The open window time is defined by $T_{OW} = 2$ x OWP(T_{WD}).
For example if $T_{WD} = 100$ ms (actual value) and OWP = ± 20% this means the closed window lasts during first the 80 ms (T_{CW} = 80 ms = 100 ms - 0.2 (100 ms)) and the open window the next 40 ms ($T_{OW} = 2 \times 0.2$ (100 ms) = 40 ms). The watchdog can be serviced between 80 ms and 120 ms after the timer reset. However as the time base is ± 10% accurate, software must use the following calculation for servicing signal $\overline{TCL}$ during the open window:
Related to curves (Fig. 10 to Fig. 20), especially Fig. 19 and Fig. 20, the relation between T_{WD} and R_{EXT} could easily be defined. Let us take an example describing the variations due to production and temperature:

1. Choice, $T_{WD} = 26$ ms.
2. Related to Fig. 20, the coefficient (T_{WD} to R_{EXT}) is 1.125 where R_{EXT} is in kΩ and T_{WD} in ms.
3. R_{EXT} (typ.) = 26 x 1.125 = 29.3 kΩ.
4. 26 ms at +25 °C



The ratio between T_{WD} = 26 ms and the ($\overline{TCL}$ period) = 25.4 ms is 0.975.
Then the relation over the production and the full temperature range is $\overline{TCL}$ period = 0.975 x T_{WD} or

$$\overline{TCL}\text{ period} = \frac{0.975 \times R_{EXT}}{1.125}$$, as typical value.

a) While PRODUCTION value unknown for the customer when $R_{EXT} \neq 118$ kΩ.
b) While operating TEMPERATURE range -40°C ≤ T_J ≤ +85°C.

5. If you fixed a $\overline{TCL}$ period = 26 ms

$$\Rightarrow R_{EXT} = \frac{26 \times 1.125}{0.975} = 30\ k\Omega.$$

If during your production the T_{WD} time can be measured at T_J = +25°C and the µC can adjust the $\overline{TCL}$ period, then the $\overline{TCL}$ period range will be much larger for the full operating temperature.

Timer Clearing and $\overline{RES}$ Action

The watchdog circuit monitors the activity of the processor. If the user's software does not send a pulse to the $\overline{TCL}$ input within the programmed open window timeout period a short watchdog $\overline{RES}$ pulse is generated which is equal to T_{WD} / 40 = 2.5 ms typically (see Fig. 5).
With the open window constraint new security is added to conventional watchdogs by monitoring both software cycle time and execution. Should software clear the watchdog too quickly (incorrect cycle time) or too slowly (incorrect execution) it will cause the system to be reset. If software is stuck in a loop which includes the routine to clear the watchdog then a conventional watchdog would not make a system reset even though software is malfunctioning; the A6130 would make a system reset because the watchdog would be cleared too quickly.
If no $\overline{TCL}$ signal is applied before the closed and open windows expire, $\overline{RES}$ will start to generate square waves of period ($T_{CW} + T_{OW} + T_{WDR}$). The watchdog will remain in this state until the next $\overline{TCL}$ falling edge appears during an open window, or until a fresh power-up sequence. The system enable output, $\overline{EN}$, can be used to prevent critical control functions being activated in the event of the system going into this failure mode (see section "Enable - $\overline{EN}$ Output"). The $\overline{RES}$ output must be pulled up to V_{OUTPUT} even if the output is not used by the system (see Fig. 8).

Combined Voltage and Timer Action

The combination of voltage and timer actions is illustrated by the sequence of events shown in Fig. 6. On power-up, when the voltage at V_{IN} reaches V_{REF}, the power-on-reset, POR, delay is initialized and holds $\overline{RES}$ active for the time of the POR delay. A $\overline{TCL}$ pulse will have no effect until this power-on-reset delay is completed. When the risk exists that $\overline{TCL}$ temporarily floats, e.g. during T_{POR}, a pull-up to V_{DD} is required on that pin. After the POR delay has elapsed, $\overline{RES}$ goes inactive and the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, $\overline{RES}$ goes active low for a short time T_{WDR} after each closed and open window period. A $\overline{TCL}$ pulse coming during the open window clears the watchdog timer. When the $\overline{TCL}$ pulse occurs too early (during the closed window), $\overline{RES}$ goes active and a new timeout sequence starts. A voltage drop below the V_{REF} level for longer than typically 5 µs overrides the timer and immediately forces $\overline{RES}$ active and $\overline{EN}$ inactive. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Enable - $\overline{EN}$ Output

The system enable output, $\overline{EN}$, is inactive always when $\overline{RES}$ is active and remains inactive after a $\overline{RES}$ pulse until the watchdog is serviced correctly 3 consecutive times (ie. the $\overline{TCL}$ pulse must come in the open window). After three consecutive services of the watchdog with $\overline{TCL}$ during the open window, the $\overline{EN}$ goes active low. A malfunctioning system would be repeatedly reset by the watchdog. In a conventional system critical motor controls could be energized each time reset goes inactive (time allowed for the system to restart) and in this way the electrical motors driven by the system could function out of control. The A6130 prevents the above failure mode by using the $\overline{EN}$ output to disable the motor controls until software has successfully cleared the watchdog three times (ie. the system has correctly restarted after a reset condition).

Typical Application

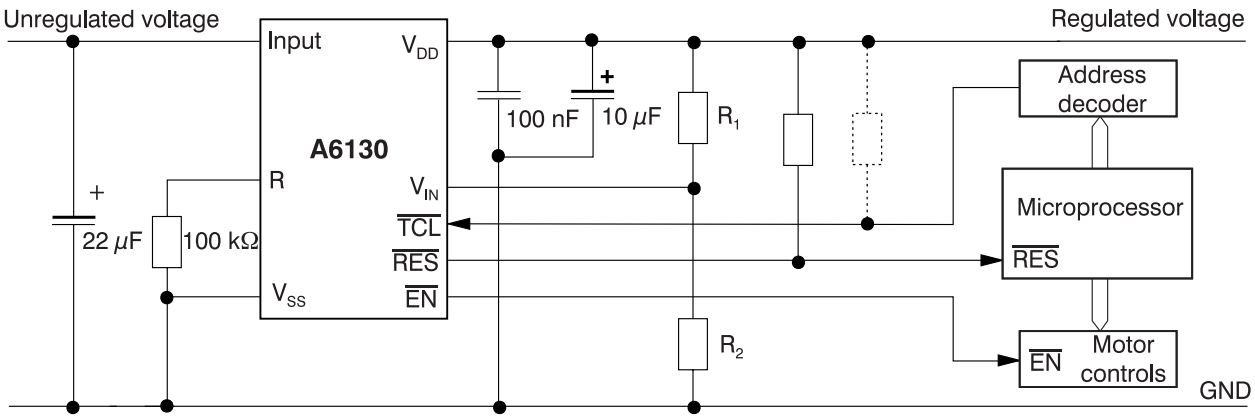


Fig. 8

OUTPUT Current versus INPUT Voltage

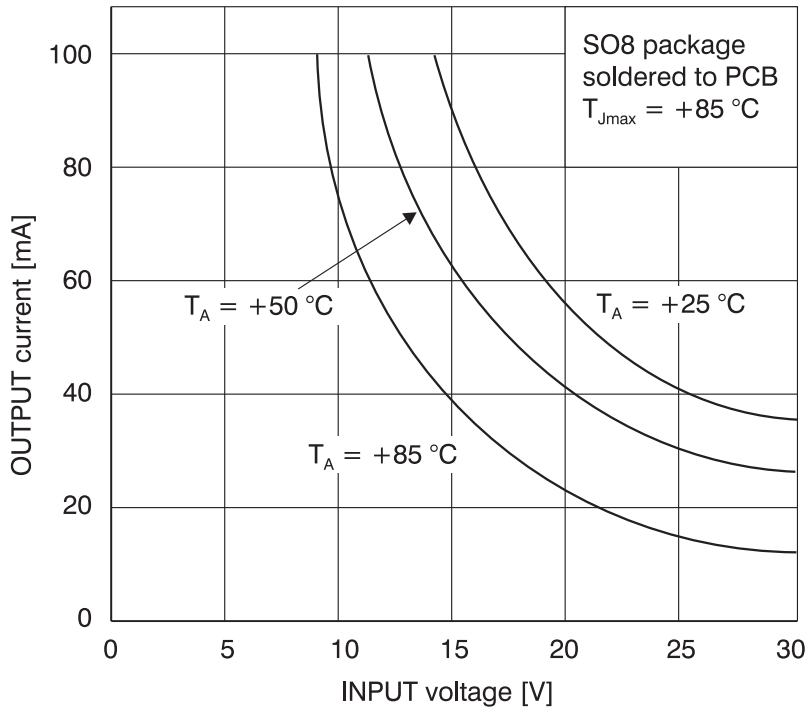


Fig. 9

T_{WD} versus Temperature at 5 V

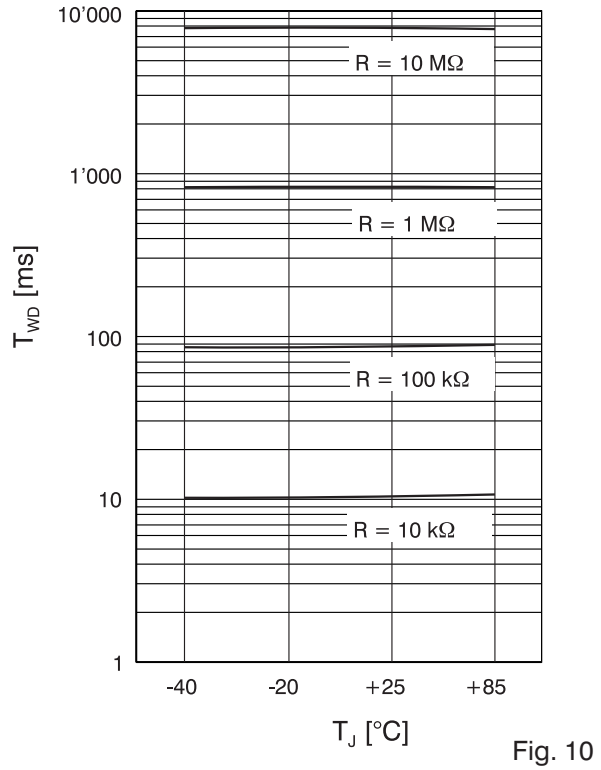


Fig. 10

T_{WD} versus R at 5 V

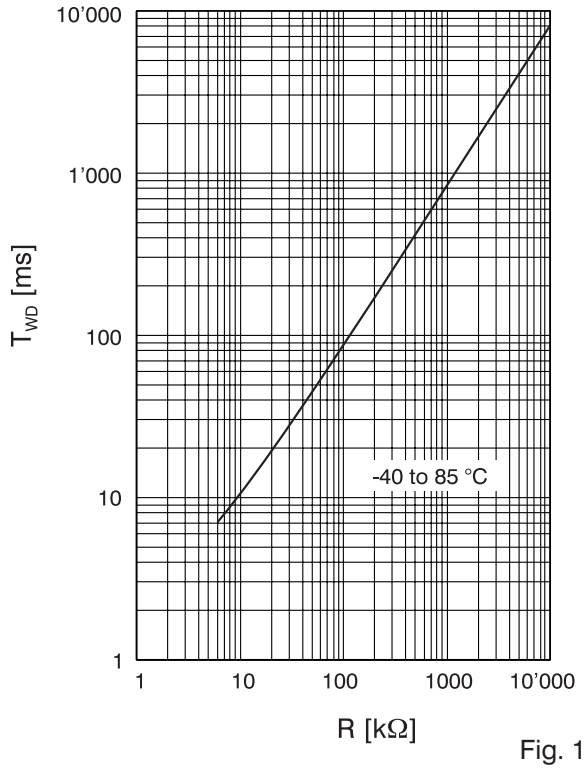


Fig. 11

T_{WD} versus V_{OUTPUT} at T_J = +25°C

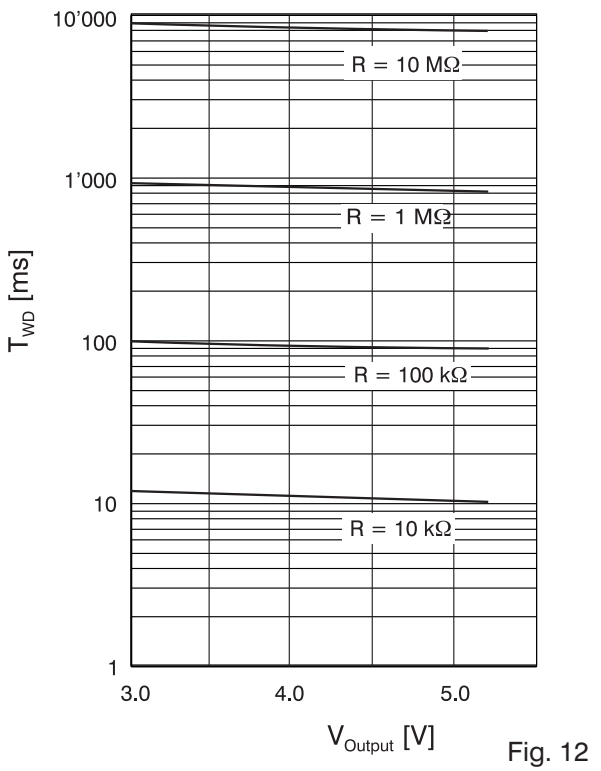


Fig. 12

T_{WD} versus R at T_J = +25°C

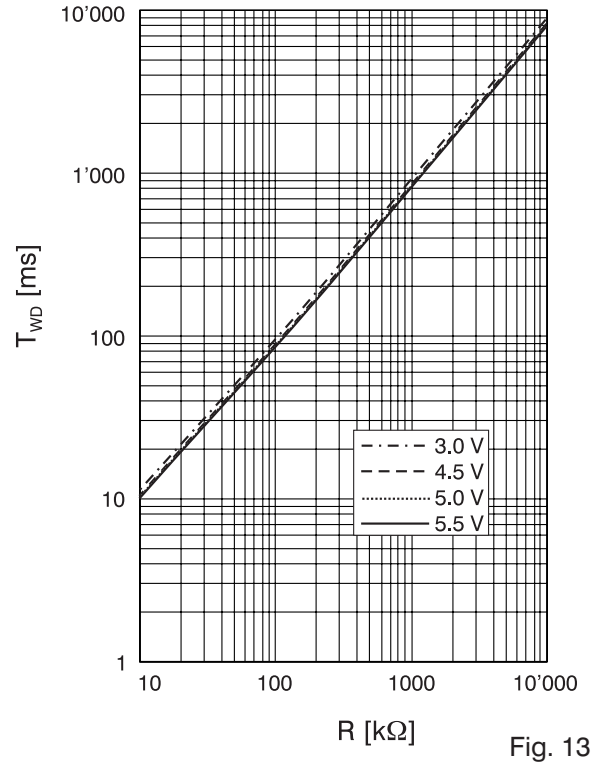
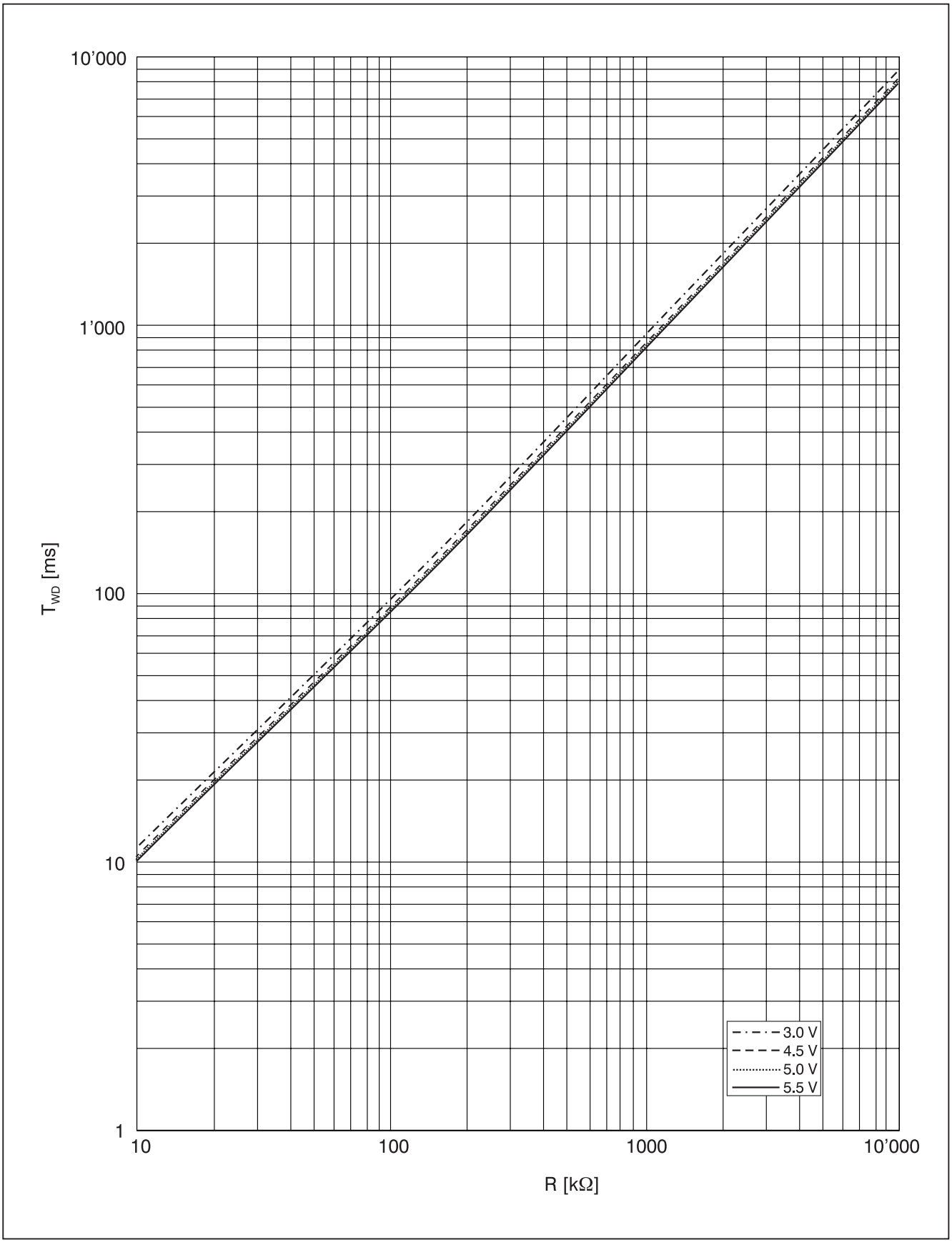


Fig. 13


10'000
1'000
100
10
1
T_{WD} [ms]
10
100
1000
10'000
R [kΩ]
3.0 V
4.5 V
5.0 V
5.5 V

T_{WD} versus V_{DD} at T_J = +85°C

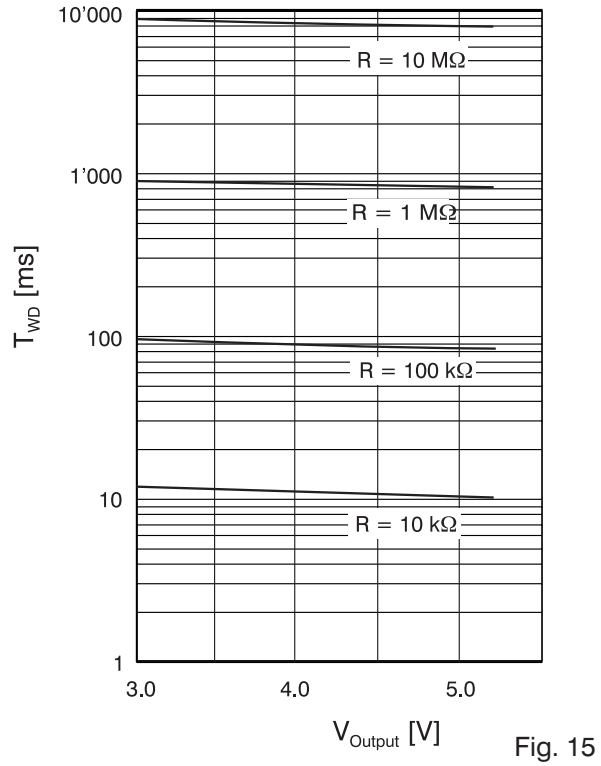


Fig. 15

T_{WD} versus R at T_J = +85°C

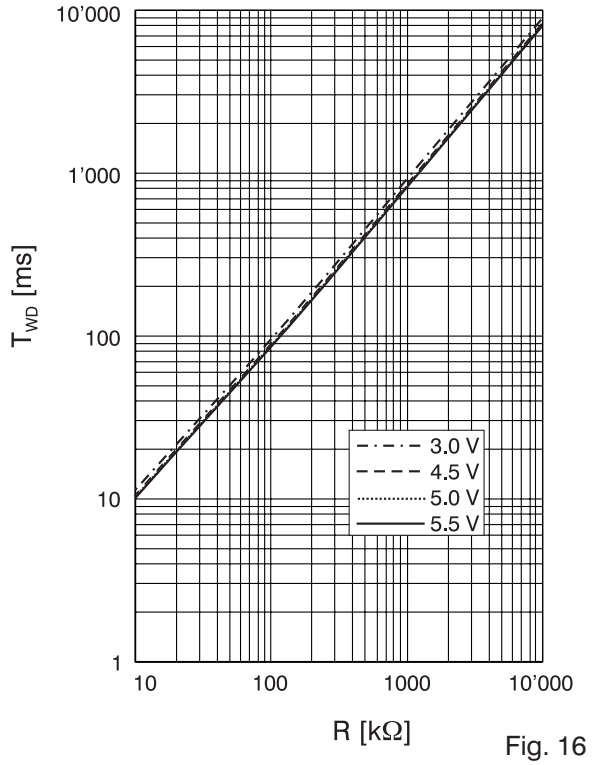


Fig. 16

T_{WD} versus V_{OUTPUT} at T_J = -40°C

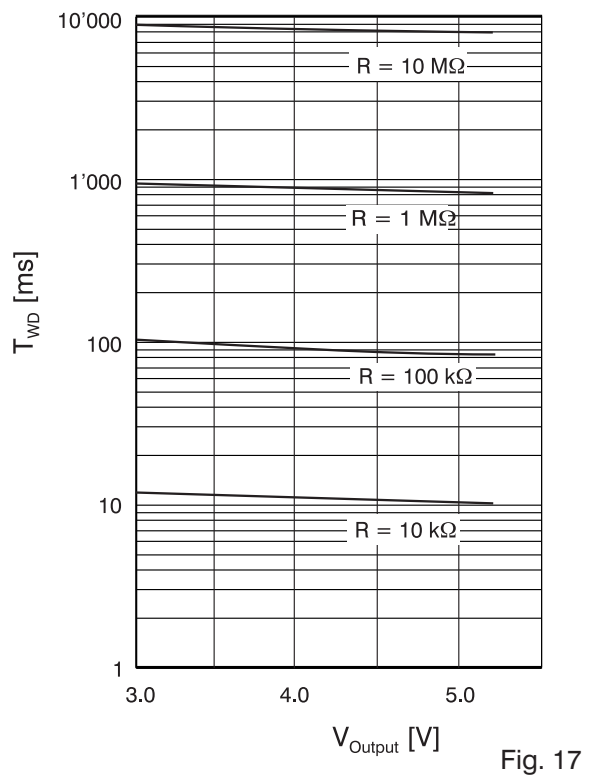


Fig. 17

T_{WD} versus R at T_J = -40°C

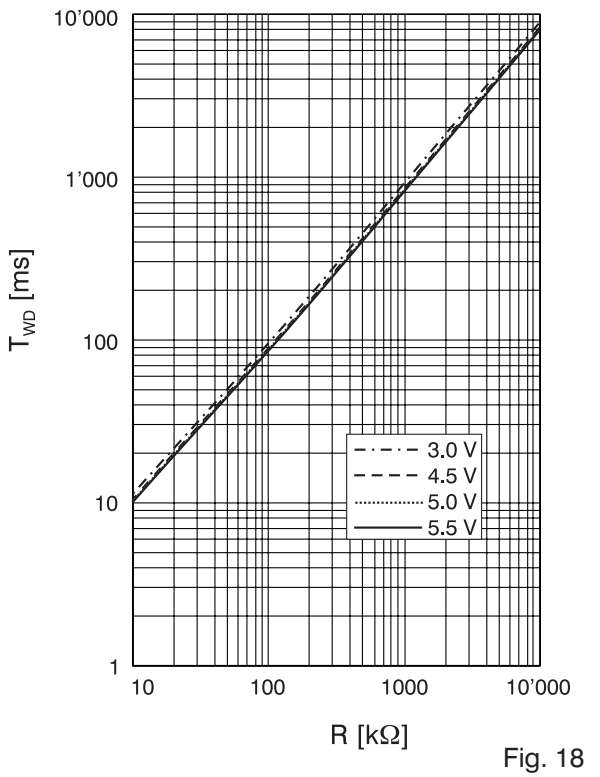


Fig. 18

T_{WD} Coefficient versus R_{EXT} at T_J = +25°C

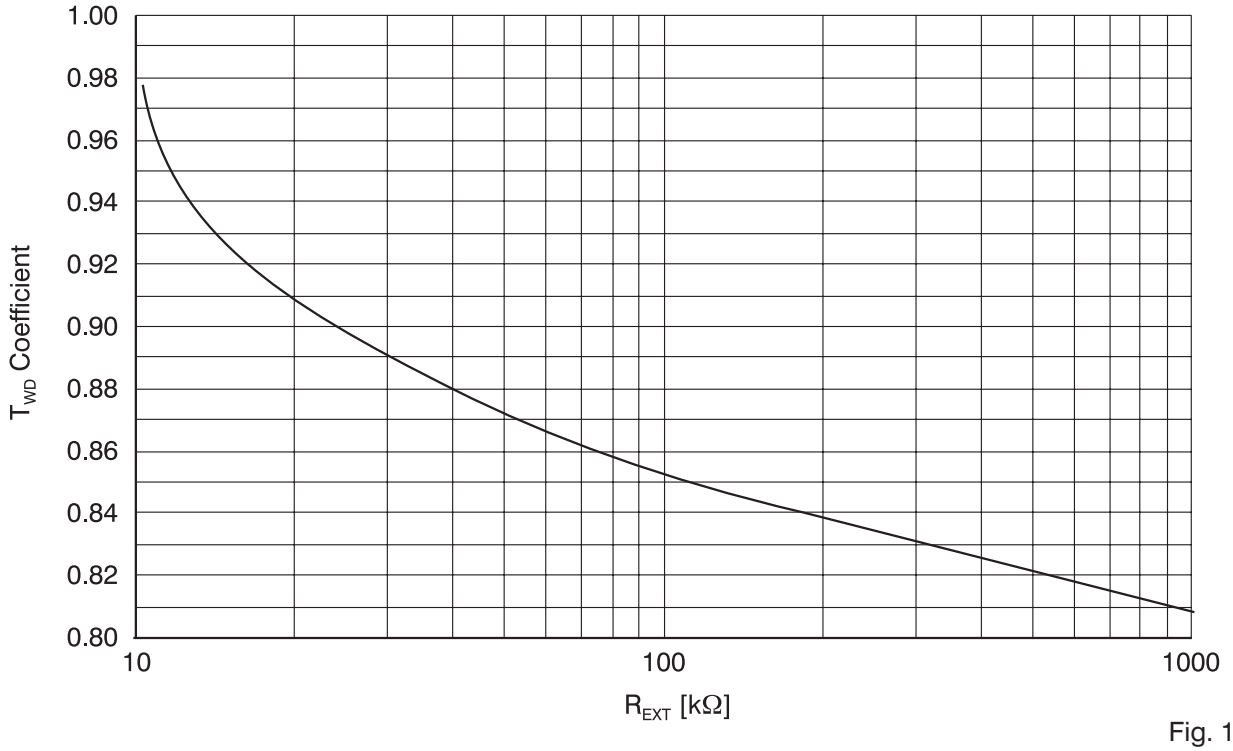


Fig. 19

R_{EXT} Coefficient versus T_{WD} at T_J = +25°C

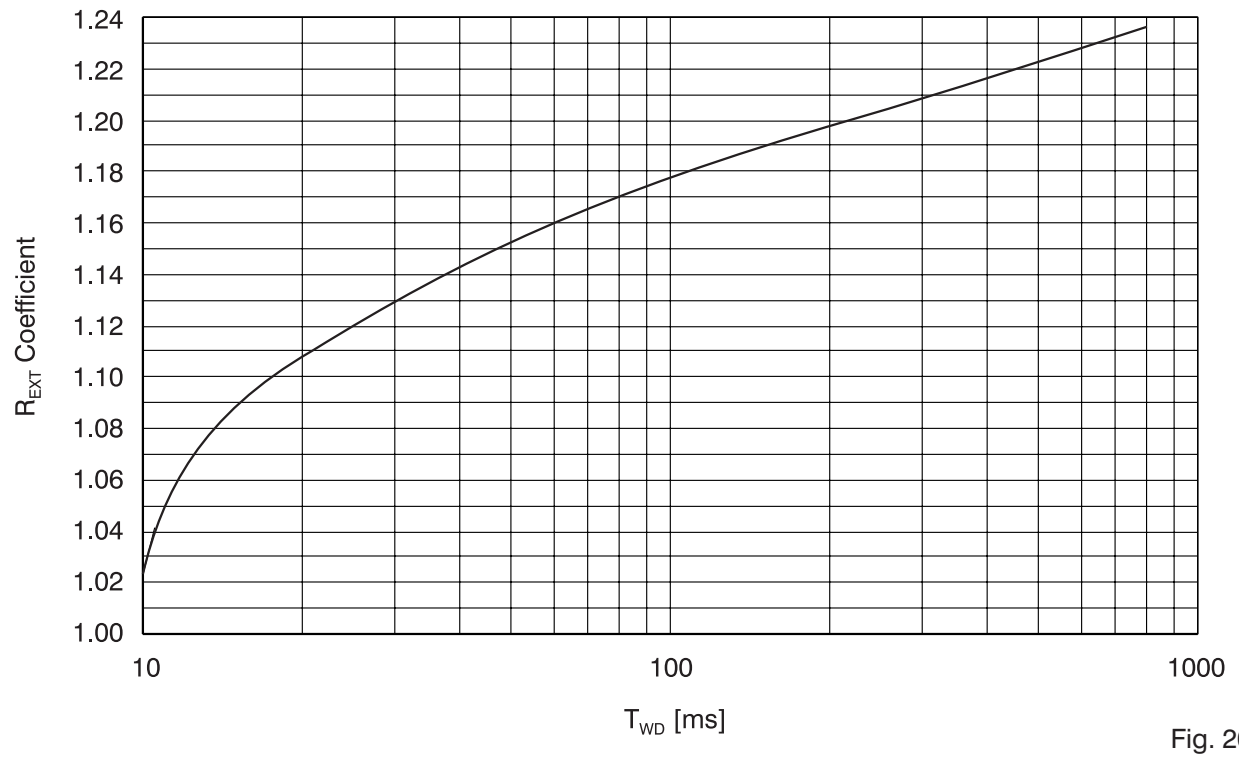
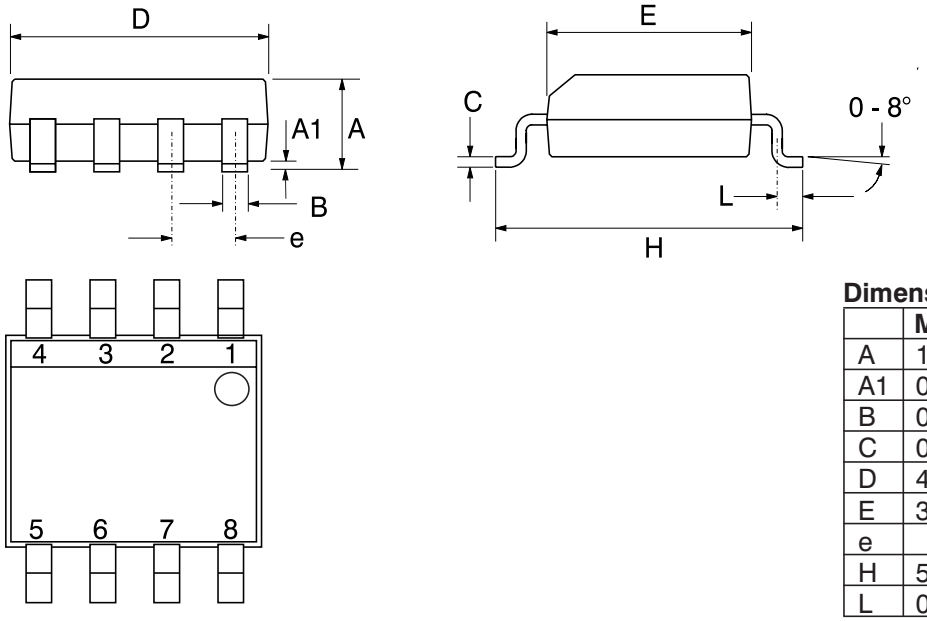


Fig. 20

Package and Ordering Information

Dimensions of 8-pin SOIC Package

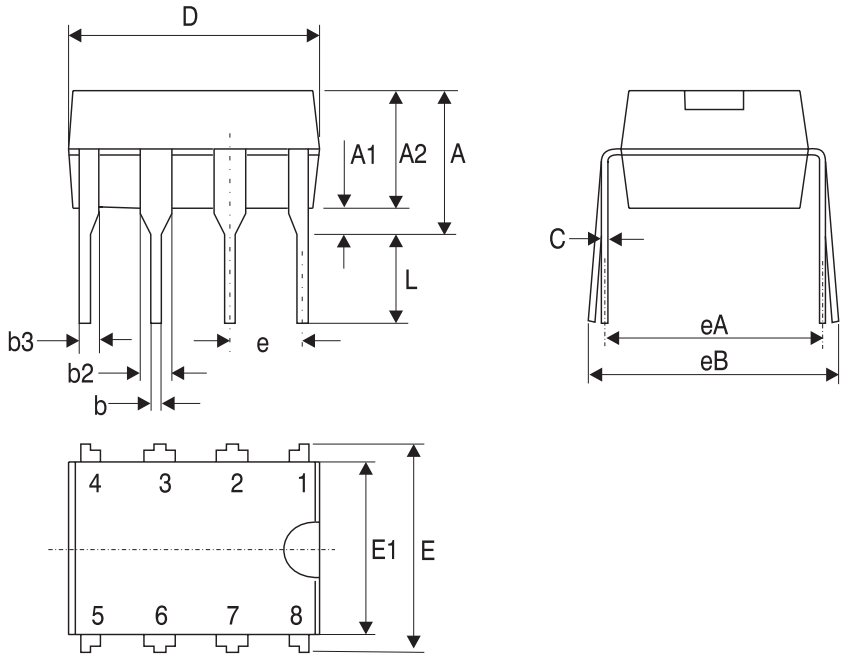


Dimensions in mm

	Min.	Nom.	Max
A	1.35	1.63	1.75
A1	0.10	0.15	0.25
B	0.33	0.41	0.51
C	0.19	0.20	0.25
D	4.80	4.93	5.00
E	3.80	3.94	4.00
e		1.27	
H	5.80	5.99	6.20
L	0.40	0.64	1.27

Fig. 21

Dimensions of 8-pin plastic DIP Package



Dimensions in mm

	Min.	Nom.	Max
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.35	0.45	0.56
b2	1.14	1.52	1.78
B3	0.76	0.99	1.14
C	0.20	0.25	0.35
D	9.01	9.27	10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81

Fig. 22

Ordering Information

When ordering please specify complete part number.

Part Number	Package	Delivery Form	Package Marking (first line)
A6130DL8A	8-pin plastic DIP	Stick	A6130
A6130SO8A	8-pin SOIC	Stick	6130A
A6130SO8B	8-pin SOIC	Tape & Reel	6130A

E. & O.E. Printed in Switzerland, Th

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