PRELIMINARY

May 2000

S1L60000 SERIES HIGH DENSITY GATE ARRAY

DESCRIPTION

The EEA S1L60000 Series is a family of ultra high-speed VLSI CMOS gate arrays utilizing a 0.25µm "sea-of-gates" architecture.

- Ultra-high-speed, high density and low power consumption
- Low voltage operation: 2.5V and 2.0V
- Number of raw gates: 2,519,604 gates

FEATURES

- Process — 0.25µm 3/4 layer metalization CMOS process
- Integration — A maximum of 2,519,604 gates (2 input NAND gate equivalent)
- Operating Speed
  Internal gates: 107ps (2.5V Typ), 140 ps (2.0V Typ)
  (2-input pair NAND, F/O = 1, Typical wire load)
  Input buffer: 260 ps (3.3V Typ), Built-in level shifter used.
  270 ps (2.5V Typ), 360 ps (2.0 Typ)
  (F/O = 2, Typical wire load)
  Output buffer: 1.5ns (3.3V Typ) Built-in level shifter used.
  1.6ns (2.5V Typ), 2.3ns (2.0V Typ) (C_L=15 pF)
- I/F Levels — CMOS/LVTTL compatible
- Input Modes — CMOS, LVTTL, CMOS Schmitt, LVTTL Schmitt, PCI-3V
  Built-in pull-up and pull-down resistor can be usable.
  (2 types for each resistor value)
- Output Modes — Normal, 3-state, bi-directional, PCI-3V
- Output Drive — I_{OL} = 0.1, 1, 3, 6, 12, 24 mA selectable
  (built-in level shifter is used at 3.3V)
  I_{OL} = 0.1, 1,3,6,9,18mA selectable (at 2.5V)
  I_{OL} = 0.05,0.3,1,1,3,6mA selectable (at 2.0V)
- RAM — Asynchronous 1-port, asynchronous 2-port
- Dual Power — Operation supported by using level-shifter circuit
  Internal logic: Operation supported by low voltage.
  I/O Buffer: Built-in interfaces of both high and low voltages possible.

Master Structure

The S1L60000 Series comprises 10 types of masters, from which the customer is able to select the master most suitable.

Master	Total BC (Raw Gates)	Number of Pads	Number of Columns (X)	Number of Rows (Y)	Cell Utilization Ratio (U)*1	
					3-layer metal	4-layer metal
S1L60093	99220	112	605	164	80	90
S1L60173	171720	148	795	216	80	90
S1L60283	284394	188	1023	278	70	85
S1L60403	400290	224	1213	330	70	85
S1L60593	595362	272	1481	402	70	85
S1L60833	831572	284	1747	476	65	80
S1L61233	1234820	344	2129	580	65	80
S1L61583	1587754	388	2413	658	65	80
S1L61903	1902960	424	2643	720	60	75
S1L62513	2519604	488	3043	828	60	75

NOTE: *1: This is the value when there are no cells, such as RAM cells. The cell use efficiency is dependent not only on the scope of the circuits, but also on the number of signals, the number of branches per signal, etc.; thus, use the values in this table only as an estimate

ELECTRICAL CHARACTERISTICS AND SPECIFICATIONS

Absolute Maximum Ratings (For single Power Supplies):

(V_{SS} = 0V)

Item	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	-0.3 to 3.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.5*1	V
Output Voltage	V_O	-0.3 to V_{DD} + 0.5*1	V
Output Current/Pin	I_{OUT}	± 30	mA
Storage Temperature	T_{STG}	-65 to 150	°C

*1: Possible to use from –0.3V to 4.0V of N channel open drain bi-directional buffers and input buffer.

Absolute Maximum Ratings (For Dual Power Supplies):

(V_{SS} = 0V)

Item	Symbol	Limits	Unit
Power Supply Voltage	HV_{DD} *3 LV_{DD} *3	-0.3 to 4.0 -0.3 t0 3.0	V V
Input Voltage	HV_I LV_I	-0.3 to HV_{DD} + 0.5 *1 -0.3 toLV^{DD} + 0.5 *1	V V
Output Voltage	HV_O LV_O	-0.3 to HV_{DD} + 0.5 *1 -0.3 to LV_{DD} + 0.5 *1	V V
Output Current/Pin	I_{OUT}	± 30 (+/- 50 *2)	mA
Storage Temperature	T_{STG}	-65 to 150	°C

*1: Possible to use from –0.3V to 4.0V of N channel open drain bi-directional buffers and input buffer.
*2. Possible to use 24mA of output buffer.
*3. $HV_{DD} > LV_{DD}$.

Recommended Operating Conditions (For Single Power Supplies: V_{DD}= 2.5V)

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	2.30	2.50	2.70	V
Input Voltage	V_I	V_{SS}	--	V_{DD} *1	V
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	t_{ri}	--	--	50	ns
Normal Input for Falling Edge Input	t_{fi}	--	--	50	ns
Schmitt Input for Rising Edge Input	t_{ri}	--	--	5	ms
Schmitt Input for Falling Edge Input	t_{fi}	--	--	5	ms

*1: Possible to use 3.6V of N channel open drain bi-directional buffers and input buffers
*2: The ambient temperature range is recommended for Tj = 0 to 85 °C.
*3: The ambient temperature range is recommended for Tj = -40 to 125 °C.

Recommended Operating Conditions (For Single Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	1.80	2.00	2.20	V
Input Voltage	V_I	V_{SS}	--	V_{DD} *1	V
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	t_{ri}	--	--	100	ns
Normal Input for Falling Edge Input	t_{fi}	--	--	100	ns
Schmitt Input for Rising Edge Input	t_{ri}	--	--	10	ms
Schmitt Input for Falling Edge Input	t_{fi}	--	--	10	ms

*1: Possible to use 3.6V of N channel open drain bi-directional buffers and input buffers
*2: The ambient temperature range is recommended for Tj = 0 to 85 °C.
*3: The ambient temperature range is recommended for Tj = -40 to 125 °C.

Recommended Operating Conditions (For Dual Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	2.30	2.50	2.70	V
Input Voltage	HV_I	V_{SS}	--	HV_{DD} *1	V
	LV_I	V_{SS}	--	LV_{DD} *1	
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	H_{tri}	--	--	50	ns
Normal Input for Falling Edge Input	H_{tfi}	--	--	50	ns
Schmitt Input for Rising Edge Input	H_{tri}	--	--	5	ms
Schmitt Input for Falling Edge Input	H_{tfi}	--	--	5	ms

*1: Possible to use 3.6V of N channel open drain bi-directional buffers and input buffers
*2: The ambient temperature range is recommended for Tj = 0 to 85 °C
*3: The ambient temperature range is recommended to Tj = -40 to 125 °C.

Recommended Operating Conditions (For Dual Power Supplies):

Item	Symbol	Min	Typ	Max	Unit
Power Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power Supply Voltage (Low Voltage)	LV_{DD}	1.80	2.00	2.20	V
Input Voltage	HV_I	V_{SS}	--	HV_{DD} *1	V
	LV_I	V_{SS}	--	LV_{DD} *1	
Ambient Temperature	T_a	0 -40	25 25	70 *2 85 *3	°C
Normal Input for Rising Edge Input	H_{tri}	--	--	50	ns
	L_{tri}	--	--	100	
Normal Input for Falling Edge Input	H_{tfi}	--	--	50	ns
	L_{tfi}	--	--	100	
Schmitt Input for Rising Edge Input	H_{tri}	--	--	5	ms
	L_{tri}	--	--	10	
Schmitt Input for Falling Edge Input	H_{tfi}	--	--	5	ms
	L_{tfi}	--	--	10	

*1: Possible to use 3.6V of N channel open drain bi-directional buffers and input buffers
*2: The ambient temperature range is recommended for Tj = 0 to 85 °C
*3: The ambient temperature range is recommended to Tj = -40 to 125 °C.

Electrical Characteristics of the S1L60000 Series:

(HV_{DD} = 3.3V in common, V_{SS} = OV, Ta = -40 to 85°C)

Item	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	--		-5	--	5	µA
Off State Leakage Current	I_{OZ}	--		-5	--	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M), -3mA (Type 1), -6mA (Type 2), -12mA (Type 3), -24mA (Type 4) HV_{DD} = Min		HV_{DD} -0.4	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M), 3mA (Type 1), 6mA (Type 2), 12mA (Type 3), 24mA (Type 4) HV_{DD}= Min		--	--	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, HV_{DD} = Max		2.2	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, HV_{DD} = Min		--	--	0.8	V
Possitive Trigger Voltage	V_{T1+}	CMOS Schmitt		1.4	--	2.7	V
Negative Trigger Voltage	V_{T1-}	CMOS Schmitt		0.6	--	1.8	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.3	--	--	V
High Level Input Voltage	V_{IH2}	LVTTL Level, HV_{DD} = Max		2.0	--	--	V
Low Level Input Voltage	V_{IL2}	LVTTL Level, HV_{DD} = Min		--	--	0.8	V
Positive Trigger Voltage	V_{T2+}	LVTTL Schmitt		1.1	--	2.4	V
Negative Trigger Voltage	V_{T2-}	LVTTL Schmitt		0.6	--	1.8	V
Hysteresis Voltage	V_{H2}	LVTTL Schmitt		0.1	--	--	V
High Level Input Voltage	V_{IH3}	PCI Level, HV_{DD} + Max		1.8	--	--	V
Low Level Input Voltage	V_{IL3}	PCI Level, HV_{DD} = Min		--	--	0.9	V
High Level Output Current	I_{OH3}	PCI Response, V_{OH} = 0.90V, HV_{DD} = Min V_{OH} = 2.52V, HV_{DD} = Max		 -36 --	 -- --	 -- -115	 mA mA
Low Level Output Current	I_{OL3}	PCI Response V_{OH} = 1.80V, HV_{DD} = Min V_{OL} = .065V, HV_{DD} = Max		 48 --	 -- --	 -- 137	 mA mA
Pull-up Resistance	R_{UP}	V_I = 0V	Type 1	30	60	(120) 144	KΩ
			Type 2	60	120	(240) 288	
Pull-down Resistance	R_{PD}	V_I =HV_{DD}	Type 1	30	60	(120) 144	KΩ
			Type 2	60	120	(240) 288	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, V_{IN} = 2.0V, HV_{DD} = Min		--	--	-20	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, V_{IN} = 0.8V, HV_{DD} = Min		--	--	17	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response, V_{IN} = 0.8V, HV_{DD} = Max		-350	--	--	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, V_{IN} = 2.0V, HV_{DD} = Max		210	--	--	µA
Input Terminal Capacitance	C_I	f = 1Mhz, V_{DD} = 0V		--	--	8	pF
Output Terminal Capacitance	C_O	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1Mhz, V_{DD} = 0V		--	--	10	pF

Electrical Characteristics of the S1L60000 Series:

(V_{DD} = 2.0V ± 0.2V, V_{SS} = 0V, T_a = -40 to 85°C)

Item	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	--		-5	--	5	µA
Off State Leakage Current	I_{OZ}	--		-5	--	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.1mA (Type S), -1mA (Type M), -3mA (Type 1), -6mA (Type 2), -9mA (Type 3), -18mA (Type 4) V_{DD} = Min		V_{DD} -0.4	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.1mA (Type S), 1mA (Type M), 3mA (Type 1), 6mA (Type 2), 9mA (Type 3), 18mA (Type 4) V_{DD} = Min		--	--	0.4	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max		1.7	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min		--	--	0.7	V
High Level Input Voltage	V_{T1+}	CMOS Schmitt		0.8	--	1.9	V
Low Level Input Voltage	V_{T1-}	CMOS Schmitt		0.5	--	1.3	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0	--	--	V
Pull-up Resistance	R_{UP}	V_I = 0V	Type 1	20	50	(100) 120	KΩ
			Type 2	40	100	(200) 240	
Pull-down Resistance	R_{PD}	V_I = V_{DD}	Type 1	20	50	(100) 120	KΩ
			Type 2	40	100	(200) 240	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, V_{IN} = 1.7V, V_{DD} = Min		--	--	-5	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, V_{IN} = 0.7V, V_{DD} = Min		--	--	5	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response, V_{IN} = 0.3V, V_{DD} = Max		-280	--	--	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, V_{IN} = 1.6V, V_{DD} = Max		170	--	--	µA
Input Terminal Capacitance	C_I	f = 1Mhz, V_{DD} = 0V		--	--	8	pF
Output Terminal Capacitance	C_O	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1Mhz, V_{DD} = 0V		--	--	10	pF

* The values parenthesized means in case of Ta = 0 to 70°C

Electrical Characteristics of the S1L60000 Series:

(V_{DD} = 2.0V ± 0.2V, V_{SS} = 0V, T_a = -40 to 85°C)

Item	Symbol	Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	--		-5	--	5	µA
Off State Leakage Current	I_{OZ}	--		-5	--	5	µA
High Level Output Voltage	V_{OH}	I_{OH} = -0.05mA (Type S), -0.3mA (Type M), -1mA (Type 1), -2mA (Type 2), -3mA (Type 3), -6mA (Type 4) V_{DD} = Min		V_{DD} -0.2	--	--	V
Low Level Output Voltage	V_{OL}	I_{OL} = 0.05mA (Type S), 0.3mA (Type M), 1mA (Type 1), 2mA (Type 2), 3A (Type 3), 6mA (Type 4) V_{DD} = Min		--	--	0.2	V
High Level Input Voltage	V_{IH1}	CMOS Level, V_{DD} = Max		1.6	--	--	V
Low Level Input Voltage	V_{IL1}	CMOS Level, V_{DD} = Min		--	--	0.3	V
Positive Trigger Voltage	V_{T1+}	CMOS Schmitt		0.4	--	1.6	V
Negative Trigger Voltage	V_{T1-}	CMOS Schmitt		0.3	--	1.4	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0	--	--	V
Pull-up Resistance	R_{UP}	V_I = 0V	Type 1	30	70	200	KΩ
			Type 2	60	140	400	
Pull-down Resistance	R_{PD}	V_I = V_{DD}	Type 1	30	70	200	KΩ
			Type 2	60	140	400	
High Level Maintenance Current	I_{BHH}	Bus Hold Response, V_{IN} = 1.7V, V_{DD} = Min		--	--	-2	µA
Low Level Maintenance Current	I_{BHL}	Bus Hold Response, V_{IN} = 0.7V, V_{DD} = Min		--	--	2	µA
High Level Reversal Current	I_{BHHO}	Bus Hold Response, V_{IN} = 0.3V, V_{DD} = Max		-100	--	--	µA
Low Level Reversal Current	I_{BHLO}	Bus Hold Response, V_{IN} = 1.6V, V_{DD} = Max		100	--	--	µA
Input Terminal Capacitance	C_I	f = 1Mhz, V_{DD} = 0V		--	--	8	pF
Output Terminal Capacitance	C_O	f = 1Mhz, V_{DD} = 0V		--	--	10	pF
Input/Output Terminal Capacitance	C_{IO}	f = 1Mhz, V_{DD} = 0V		--	--	10	pF

* The values parenthesized means in case of Ta = 0 to 70°C

Quiescent Current (For Single Power Supplies)

(Tj = 85°C)

Master	2.5V ±0.2V I_{DDS} Max	2.0V ±0.2V I_{DDS} Max	Unit
S1L60093 / 60173 / 60283	120	90	µA
S1L60403 / 60593 / 60833	330	270	µA
S1L61233 / 61583	630	510	µA
S1L61903 / 62513	1000	800	µA

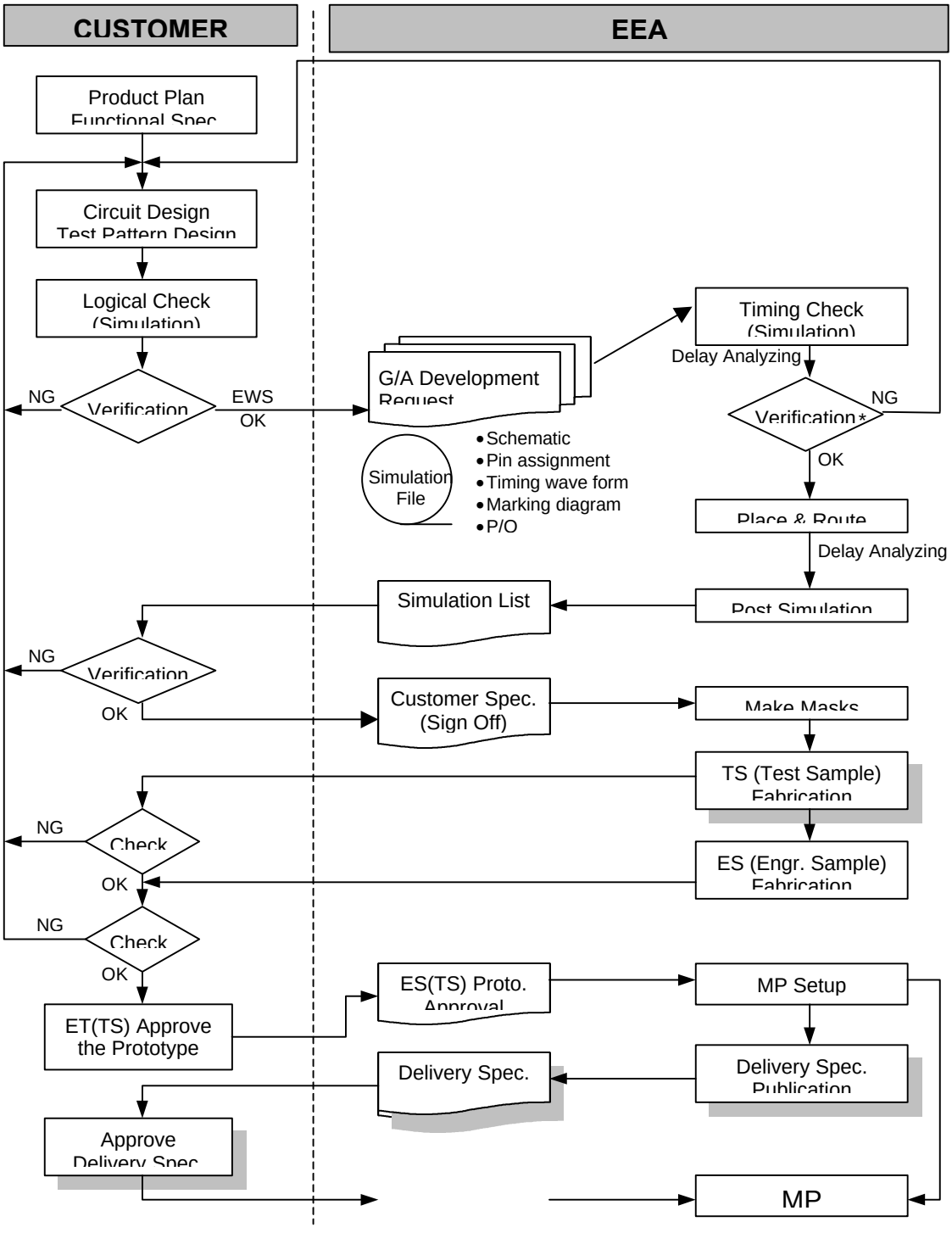
Quiescent Current (For Dual Power Supplies)

(Tj = 85°C)

Master	3.3V ±0.3V HI_{DDS} Max	2.5V ± 0.2V LI_{DDS} Max	3.3V ±0.3V HI_{DDS} Max	2.0V ±0.2V LI_{DDS} Max	Unit
S1L60093 / 60173 / 60283	21	120	21	90	µA
S1L60403 / 60593 / 60833	35	330	35	270	µA
S1L61233 / 61583	48	630	48	510	µA
S1L61903 / 62513	60	1000	60	800	µA

GATE ARRAY DEVELOPMENT FLOW

May 2000



NOTE: ( ) is based on customer's requirement.

EEA CUSTOMER ENGINEERING

To help customers implement their design of EEA ASIC's, we offer training at our design centers and at customer sites when required.

When a design is started, an EEA engineer is assigned to the project and will remain with the project through its completion. EEA engineers will work with the customer on design, software and other technical issues. When the design files are transferred to EEA, the assigned engineer will verify the design's integrity and prepare it for place and route. The EEA Customer Engineering Group provides all technical customer-support services including:

- Pre-Sale Technical Support
- Customer Training
- Design Assistance
- Custom Cell Development
- Place and Route
- Scan Insertion and ATPG
- Netlist Conversion and Synthesis
- Software Documentation
- Simulation Support
- Turnkey Design
- Design Verification
- Static Timing Analysis
- JTAG Insertion
- Test Vector Conversion

EDA/CAE SUPPORT

- Schematic Capture
  - Viewlogic (Synopsys): Viewdraw
  - EEA: Auklet (ECS)
- Synthesis
  - Synopsys: DesignCompiler
  - Exemplar Logic: Leonardo
- Simulation
  - Cadence: Verilog-XL
  - Synopsys: VSS (VHDL)
  - Avant!: Polaris (Purespeed)
  - Viewlogic (Synopsys): Viewsim
  - Modeltech: V-System (VHDL)
- DFT
  - Synopsys: TestCompiler+
  - Viewlogic (Synopsys): TestGen (Sunrise)
- Place & Route
  - Cadence: GateEnsemble
  - Avant!: Aquarius-GA (Apollo)
- Delay Calculation (Post-Route)
  - EEA: Peacock (EXDT)

EDA/CAE SUPPORT (continued)

- Static Timing
  - Synopsys: PrimeTime (DesignTime)
  - Viewlogic (Synopsys): Motive

- Layout Verification
  - Cadence: Dracula/LVS

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ASIC DATA SHEET

S1L60000 Series

NOTICE

For additional information about EEA ASIC products and services, or to discuss a solution tailored to your specific requirements, call your local EEA sales office or contact the factory.

Corporate Headquarters
Northwest Regional
Sales Office & Design Center
150 River Oaks Parkway
San Jose, CA 95134
Phone: (408)922-0200
Fax: (408)922-0238

Northeast Regional
Sales Office
301 Edgewater Place, Suite 120,
Wakefield, MA 01880
Phone: (617)246-3600
Fax: (617)246-5443

Southeast Regional
Sales Office
4300 Six Forks Road, Suite 430,
Raleigh, NC 27609
Phone: (919)781-7667
Fax: (919)781-6778

Central Regional
Sales Office
1450 E. American Lane, #1550
Schaumburg, IL 60173
Phone: (847)517-7667
Fax: (847)517-7601

http://www.eea.epson.com