EPSON

SED1670

Dot Matrix High Duty LCD Driver

- 100 Output
- 1/64 to 1/300 in display duty
- CMOS High Voltage Resistant Process

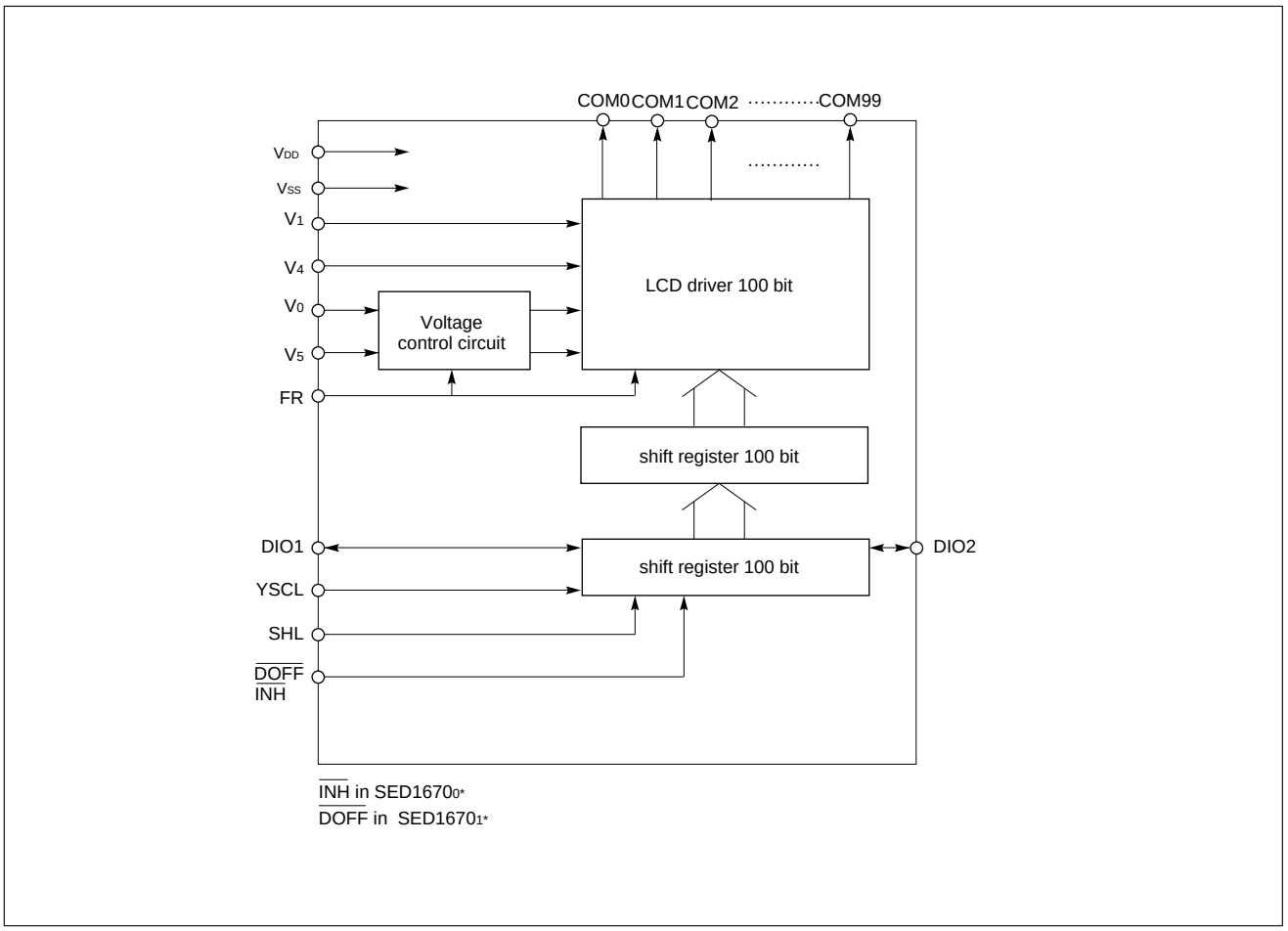
■ OVERVIEW

The SED1670 is a 100 output low-power resistance common (row) driver which is suitable for driving a very high capacity dotmatrix LCD panels upto a duty ratio of 1/300. It is intended to be used in conjunction with the SED1640D or SED1606D as a pair.
Since the SED1670 is so designed to drive LCDs over a wide range of voltages, and also the maximum potential V0 of its LCD drive bias voltages is isolated from V_{DD} to allow the LCD driving bias voltages to be externally generated optionally with a high accuracy, it can cope with a wide range of LCD panels.
Owing to its pad layout which can minimize its PC boards mounting space in addition to its selectable bidirectional driver output sequence and as many as 100 LCD output segments of high pressure resistance and low output impedance, it is possible to obtain the highest driver working efficiency for the 1/200 duty panel.
And the SED1670 can display 65 x 132 panel when used as a common driver of RAM buit-in driver, SED1531.

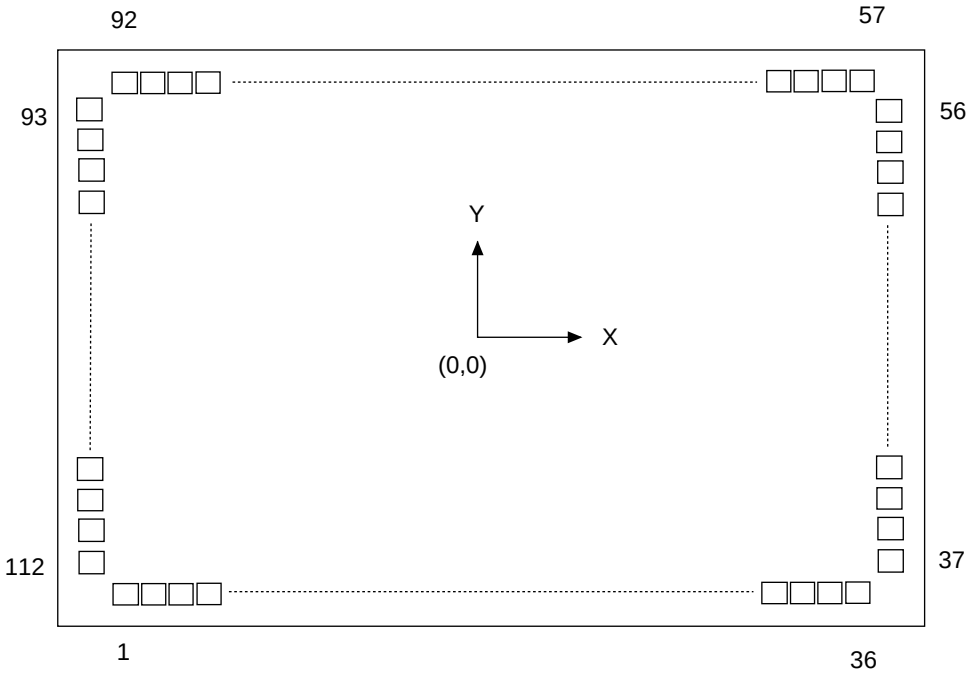
■ FEATURES

- Number of LCD drive output segments: 100
- Common output ON resistance: 700Ω (Typ.)
- Display duty ratio: 1/64 to 1/300 (Reference)
- Display capacity: Possible to display 640 x 480 dots when used in combination with SED 1640D or SED1606D.
- Selectable pin output shift direction
- No-bias display OFF function (*1*)
- Instantaneous display blanking enabled by inhibit function (*0*)
- Adjustable offset bias of LCD power to V_{DD} level
- Wide range of LCD drive voltages: –7 V to –28 V (Absolute maximum rated voltage: –30 V)
- Logic system power supply: –2.7 V to –5.5 V
- Chip packaging
  SED1670D$_{0A}$ (Al-pad die form)
  SED1670D$_{1A}$
  SED1670D$_{0B}$ (Au bump die form)
  SED1670D$_{1B}$
  SED1670T$_{0A}$ (TCP die form) * Under Planning
  SED1670T$_{1A}$ * Under Planning
- No radial rays countermeasure taken in designing

■ BLOCK DIAGRAM



• PAD LAYOUT AND COORDINATES



Chip size ..... 5.49mm x 3.03mm

1) Au bump specification reference values
   Bump specific : High Quarity Au bump
   Bump size : 100µm x 113µm
   Bump height : 17µm - 28µm

2) Al Pad specification reference values
   Pad Opening : 100µm x 100µm

PAD		Actual dimensions	
NO.	NAME	X	Y
1	COM5	-2187	-1357
2	6	-2058	↓
3	7	-1929	
4	8	-1799	
5	9	-1670	
6	10	-1541	
7	11	-1412	
8	12	-1283	
9	13	-1153	
10	14	-1024	
11	15	-895	
12	16	-766	
13	17	-637	
14	18	-507	
15	19	-378	
16	20	-249	
17	21	-120	
18	22	10	
19	23	139	
20	24	268	
21	25	397	
22	26	526	
23	27	656	
24	28	785	
25	29	914	
26	30	1043	
27	31	1172	
28	32	1302	
29	33	1431	
30	34	1560	
31	35	1689	
32	36	1818	
33	37	1948	
34	38	2077	
35	39	2206	
36	40	2335	-1357
37	41	2584	-1231
38	42	2584	-1094
39	43	2584	-969
40	44	2584	-840

PAD		Actual dimensions	
NO.	NAME	X	Y
41	COM45	2584	-711
42	46	↓	-581
43	47		-452
44	48		-323
45	49		-194
46	50		-65
47	51		65
48	52		194
49	53		323
50	54		452
51	55		581
52	56		711
53	57		840
54	58		969
55	59		1098
56	60	2584	1231
57	61	2298	1357
58	62	2168	↓
59	63	2039	
60	64	1910	
61	65	1781	
62	66	1652	
63	67	1522	
64	68	1393	
65	69	1264	
66	70	1135	
67	71	1006	
68	72	876	
69	73	747	
70	74	618	
71	75	489	
72	76	360	
73	77	230	
74	78	101	
75	79	-28	
76	80	-157	
77	81	-286	
78	82	-416	
79	83	-545	↓
80	84	-674	1357

PAD		Actual dimensions	
NO.	NAME	X	Y
81	COM85	-803	1357
82	86	-932	↓
83	87	-1062	
84	88	-1191	
85	89	-1320	
89	90	-1449	
87	91	-1578	
88	92	-1708	
89	93	-1837	
90	94	-1966	
91	95	-2095	
92	96	-2224	1357
93	97	-2473	1334
94	98	↓	1201
95	99		1071
96	DIO2		941
97	$\overline{\text{DOFF}}$		715
(97)	($\overline{\text{INH}}$)		
98	FR		585
99	YSCL		455
100	SHL		325
101	V_{DD}		185
102	V_{SS}		46
103	V_0		-112
104	V_1		-252
105	V_4		-391
106	V_5		-531
107	DIO1		-671
108	COM0		-810
109	1		-941
110	2		-1071
111	3	↓	-1201
112	4	-2473	-1334

PAD No. 97: $\overline{\text{INH}}$ for SED1670*0*
$\overline{\text{DOFF}}$ for SED1670*1*

• ABSOLUTE MAXIMUM RATINGS

V_{DD}=0V

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–7.0 to +0.3	V
Supply voltage (2)	V_5	–30.0 to +0.3	V
Supply voltage (3)	V_0, V_1, V_4	V_5–0.3 to +0.3	V
Input voltageV_I		V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Output current (1)	I_O	20	mA
Output current (2)	I_{OCOM}	20	mA
Operating temperature	Topr	–40 to + 85	°C
Storing temperature 1	Tstg	–65 to +150	°C

Notes: 1. The voltage of V_0, V_1 and V_4 must always satisfy the condition of $V_{DD} \geqq V_0 \geqq V_1 \geqq V_4 \geqq V_5$.
2. Floating of the logic system power during while the LCD drive system power is applied, or exceeding V_{SS} = –2.6 V or more can cause permanent damage to the LSI. Functional operation under these conditions is not implied.
Care should be taken to the power supply sequence especially in the system power ON or OFF.

• ELECTRICAL CHARACTERISTICS

● DC characteristics

(Unless otherwise specified, V_{DD} = V_0 = 0V, V_{SS} = –5.0V±10%, Ta = –40 to 85°C.)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
Supply voltage (1)	V_{SS}	–	–5.5	–5.0	–2.7	V	V_{SS}
Recommended operating voltage	V_5	–	–28.0	–	–7.0	V	V_5
Operation enable voltage	V_5	Functional operation	–	–	–7.0	V	V_5
Supply voltage (2)	V_0	Recommended value	–2.5	–	0	V	V_0
Supply voltage (3)	V_1	Recommended value	2/9·V_5	–	V_{DD}	V	V_1
Supply voltage (4)	V_4	Recommended value	V_5	–	7/9·V_5	V	V_4
"H" input voltage (1)	V_{IH}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	DIO1, DIO2, YSCL, SHL, FR
"L" input voltage (1)	V_{IL}		V_{SS}	–	0.8V_{SS}	V	
"H" input voltage (2)	V_{IHT}	V_{SS}=–2.7V to –5.5V	0.2V_{SS}	–	0	V	$\overline{DOFF}$, $\overline{INH}$
"L" input voltage (2)	V_{ILT}		V_{SS}	–	0.85V_{SS}	V	
"H" output voltage	V_{OH}	I_{OH}=–0.3mA I_{OH}=–0.2mA (V_{SS}=–2.7 to –4.5V)	–0.4	–	0	V	DIO1, DIO2
"L" output voltage	V_{OL}	I_{OL}=+0.3mA I_{OL}=+0.2mA (V_{SS}=–2.7 to –4.5V)	V_{SS}	–	V_{SS}+0.4	V	
Input leakage current Input/output leakage current	I_{LI}	V_{SS} ≤ V_{IN} ≤ 0V	–	–	2.0	µA	YSCL, SHL, $\overline{DOFF}$, $\overline{INH}$, FR
Static current	$I_{LI/O}$	V_{SS} ≤ V_{IN} ≤ 0V	–	–	5.0	µA	DIO1, DIO2
	I_{DDS}	V_5=–7.0 to –28.0V V_{IH}=V_{DD}, V_{IL}=V_{SS}	–	–	25	µA	V_{DD}
Output resistance	R_{COM}	ΔVON =0.5V, V_5= –20.0V, When the V_1, V_4, V_0 or V_5 level is output	–	0.70	1.40	KΩ	COM0~COM99
Average operating current consumption (1)	I_{SS1}	V_{SS}=–5.0V, V_{IH}=VDD, V_{IL}=V_{SS}, f_{YSCL}=12KHz, Frame frequency=60Hz, Input data; "H" at no load every 1/200 duty	–	7	15	µA	V_{SS}
		Other conditions are the same as V_{SS} = –3.0 V	–	5	10		
Average operating current consumption (2)	I_{SS2}	V_{SS}=–5.0, V,=–2.0V, V_4=–18.0V, V_5=–20.0V Other conditions are the same as in the item of ISS1.	–	7	15	µA	V_5
Input pin capacitance	C_I	Ta=25°C	–	–	8	pF	YSCL, SHL, $\overline{DOFF}$, $\overline{INH}$, FR
Input/output pin capacitance	$C_{I/O}$		–	–	15	pF	DIO1, DIO2

• DIFFERENT POINTS FROM REPLACEMENT PRODUCT

	SED1670*0*	SED1631**
Function	Bidirectional shift register $\overline{INH}$ 100 output segments	Bidirectional shift register $\overline{INH}$ 100 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

	SED1670*1*	SED1635**
Function	Bidirectional shift register $\overline{DOFF}$ 100 output segments	Bidirectional shift register $\overline{DOFF}$ 100 output segments
Output Tr configuration	Fig. 1	Fig. 2
PAD layout	Identical to the equivalent product	–
PAD coordinates	Different from the equivalent product	–

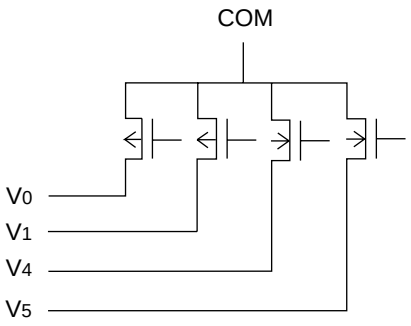
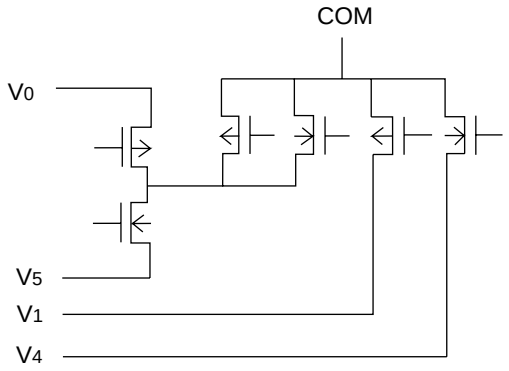


Fig. 1



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SEIKO EPSON CORPORATION
ELECTRONIC DEVICE MARKETING DEPARTMENT

IC Marketing & Engineering Group
421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5816 FAX: 0425-87-5624

International Marketing Department I (Europe, U.S.A.)
421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5812 FAX: 0425-87-5564

International Marketing Department II (Asia)
421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5814 FAX: 0425-87-5110

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