ESS Technology, Inc.

ES2898/ES2828
V.90/V.92 PCI DSP Modem Solution
Product Brief

DESCRIPTION

The ESS Technology ES2898/ES2828 *Tele*Drive® chipset is a highly integrated solution that brings advanced modem functionality to notebooks, desktops, and add-in-cards. The ES2898/ES2828 chipset provides an efficient V.90/V.92 56 kbps data/fax solution and adds both a Telephone Answering Machine (TAM) feature and a full-duplex speakerphone feature.

The data pump algorithms run on the ES2898 DSP, along with the echo cancellation required for implementing a full-duplex speakerphone feature. The host CPU is utilized to run the modem controller functions, including the standard AT command set, V.42***bis*** and V.44 data compression features, Classes 1 and 2 fax, and ITU-T V.80 sync access to support H.324 video conferencing applications. The ES2898 DSP offers an integrated PCI bus interface.

The ES2828 is the companion Analog-Front-End (AFE) chip to the ES2898. It integrates a low-pass, continuous-time anti-aliasing filter, a 16-bit resolution ADC, a 16-bit DAC, a low-pass output-reconstruction filter, and a CHI bus interface to interface to the ES2898. The ES2828 includes two signal processing channels that operate synchronously so that data reception at the ADC channel and data transmission from the DAC channel occur during the same time interval. The ES2828 incorporates an AC-Link to interface to core logic chipsets to provide a standalone MC'97 host-based V.90/V.92 modem solution.

The ES2898 DSP is available in an industry-standard 100-pin Low-profile Quad Flat Pack (LQFP) package. The ES2828 is available in an industry-standard 48-pin LQFP package.

MODEM FEATURES

- Data mode capabilities:
  - V.90/V.92 56 kbps.
  - V.34 33.6 kbps and fallbacks.
  - Standard AT command set.
  - V.42 (LAPM) and MNP error correction.
  - V.42***bis***/MNP 5 and V.44 data compression.
  - 3.3V power supply, 5V input tolerant.
- Fax mode capabilities:
  - ITU-T V.17, V.21 ch2, V.27ter, and V.29.
  - Group 3 (TIA/EIA 578 Class 1 and Class 2).
- Telephony capabilities:
  - Telephone answering machine.
  - Full duplex speakerphone.
  - Caller ID.
  - Modem on hold.
- Sigma-delta modulation Codec.
- Programmable downsampling frequency for modem and voice applications.
- ACPI power management.
- TIES escape sequence.
- V.80 (H.324 software stack compatible).
- Microsoft Windows™ 98/SE/ME/2000/XP:
  - UNIMODEM V.
  - TAPI.
- Microsoft Windows NT 4.0

SYSTEM BLOCK DIAGRAM

Figure 1 Shows the ES2898/ES2828 system block diagram.

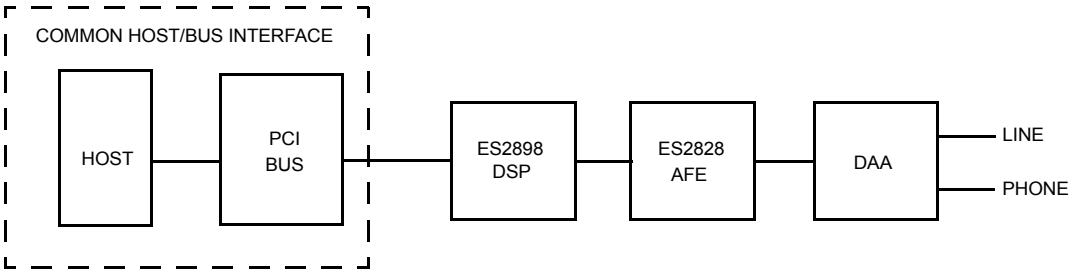

Figure 1 ES2898/ES2828 System Block Diagram

PINOUT

Figure 2 shows the ES2898 and ES2828 pinout diagrams.

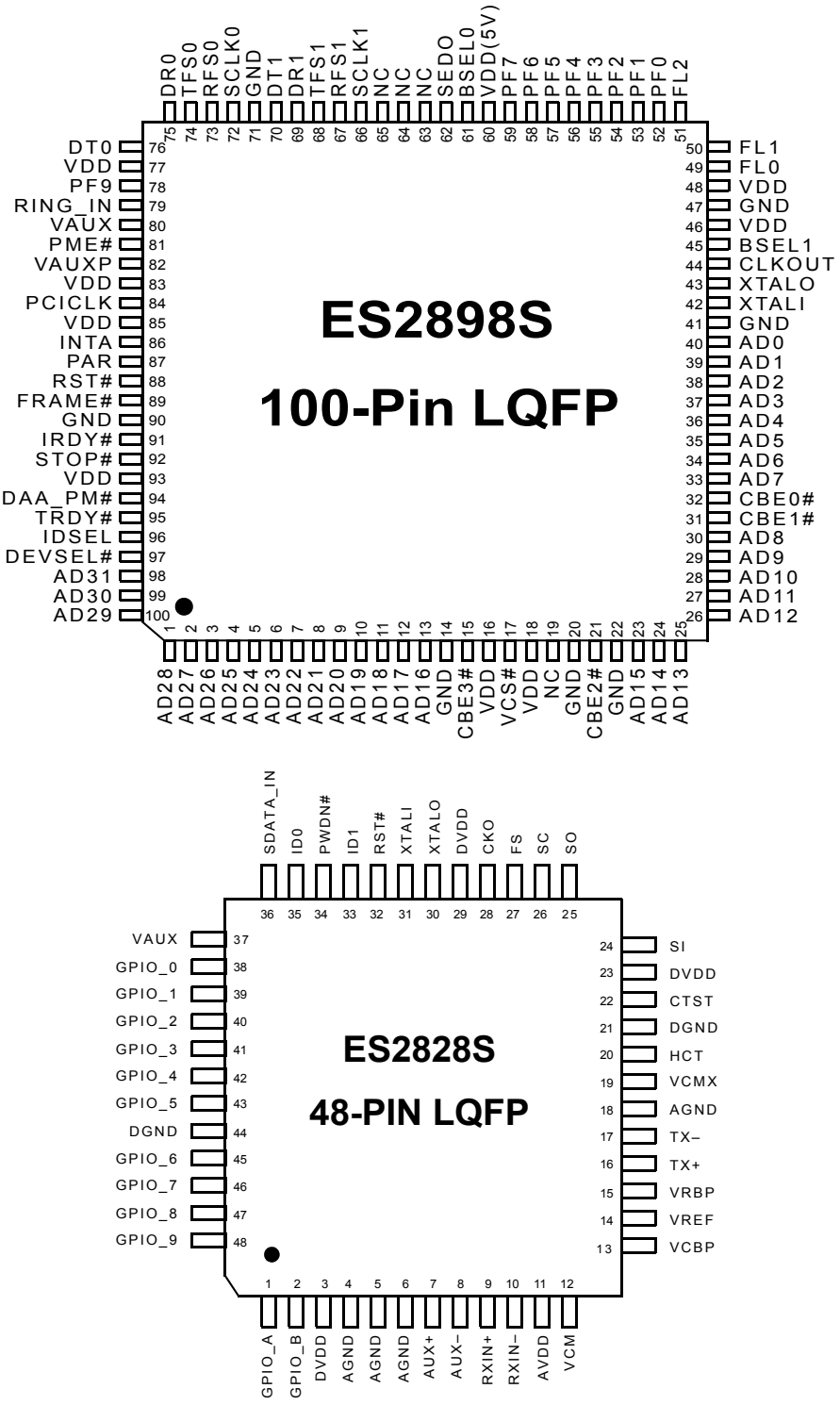

Figure 2 ES2898 and ES2828 Pinout Diagrams

PIN DESCRIPTIONS

Table 1 lists the ES2898 pin descriptions. Table 2 lists the ES2828 pin descriptions.

Table 1 ES2898 Pin Descriptions

Names	Pin Numbers	I/O	Definitions
AD[16:31]	1:13, 98, 99, 100	I	When the ES2898 interfaces to a PCI bus, these pins function as AD[16:31]. The PCI bus implements a 32-bit multiplexed address and data bus.
GND	14, 20, 22, 41, 47, 71, 90	G	Ground.
C/BE[3:0]#	15, 21, 31, 32	I	Bus command/byte enable. These pins are multiplexed. During the address phase of a bus transaction, these pins define the bus command. During the data phase, these pins are used as byte enables.
VDD	16, 18, 46, 48, 77, 83, 85, 93	P	Digital supply voltage, 3.3V.
CS#	17	I	ES2898 chip select when the device is in non-PnP mode which requires an external chip select. When the ES2898 interfaces to a PCI bus, use an internal chip select and tie the CS pin to this VDD pin through a pullup 10 kΩ resistor.
PERR#	19	O	Parity error output.
AD[0:15]	23:30, 33:40	I/O	When the ES2898 interfaces to a PCI bus, these pins function as AD[15:0]. The PCI bus implements a 32-bit multiplexed address and data bus.
XTALI	42	I	ES2898 clock input. This pin can be driven by either a crystal or an oscillator. When using a crystal, XTALO is used as the other crystal pin. When using an oscillator, the output of the oscillator is connected to XTALI. An internal clock doubler doubles the frequency at XTALI.
XTALO	43	O	Works in conjunction with XTALI when a crystal is used. When an oscillator is used, XTALO is left unconnected.
CLKOUT	44	O	Fixed-frequency clock output. The frequency of this pin is the same as the crystal input of the DSP clock. The clock is stopped during D2 and D3 states when the ST_CLKOUT bit is set.
BSEL1 / BSEL0	45, 61	I	Used to determine the operating mode of the ES2898. These pins are sampled at the falling edge of reset and are encoded as follows:.

Configuration	BSEL1 (pin 45)	BSEL0 (pin 61)
ISA PnP mode with internal chip select	0	0
ISA mode with external chip select	0	1
PCI interface	1	0
Generic 16-bit host interface	1	1

FL0	49	O	Used as flag 0 output during normal operation.
FL1	50	O	Used as flag 1 output during normal operation while the bypass circuitry is included. Will be activated during power-down mode.
FL2	51	O	Functions as flag 2 output during normal operation, and can also be used to provide a pass-through reset to the ES2828. To bring the devices out of reset, write a logic zero. FL2 carries the reset signal for the ES2828.
PF[7:0]	52, 53, 54, 55, 56, 57, 58, 59	I/O	General-purpose programmable bidirectional flag. These pins can be used for interfacing with a telephone or other device, performing such functions as phone-off-hook, phone-on-hook, ring, caller ID, etc. PF[0] is specially designed to support the ring function.
VDD(5V)	60	P	Digital supply voltage. If the ES2898 interfaces with a 5V input, tie this pin to 5V. Otherwise, tie this pin to 3.3V.
SEDO	62	I	Serial EEPROM data input.
SECS	63	O	Serial EEPROM chip select.
SEDI	64	O	Serial EEPROM serial data output.
SECLK	65	O	Serial EEPROM clock.
SCLK1	66	I/O	Serial clock 1. This clock can be generated either by the ES2898 or by the ES2828.

Table 1 ES2898 Pin Descriptions (Continued)

Names	Pin Numbers	I/O	Definitions
RFS1	67	I/O	Receive frame for serial port 1. Can be generated either internally or externally. This signal is asserted one clock before data is sent on the DR1 pin.
TFS1	68	I/O	Transmit frame for serial port 1. Can be generated either internally or externally.
DR1	69	I	Data receive pin for serial port 1.
DT1	70	O	Data transmit pin for serial port 1.
SCLK0	72	I/O	Serial clock 0. This clock can be generated either by the ES2898 or by the ES2828.
RFS0	73	I/O	Receive frame for serial port 0. Can be generated either internally or externally. This signal is asserted one clock before data is sent on the DR0 pin.
TFS0	74	I/O	Transmit frame for serial port 0. Can be generated either internally or externally.
DR0	75	I	Data receive pin for serial port 0.
DT0	76	O	Data transmit pin for serial port 0.
PF9	78	I	Tie this pin to ground through a 4.7k Ω resistor.
RING_IN	79	I	Used for ring detect during ***D3$_{cold}$*** state to drive device back to its default power-up state.
V_{AUX}	80	P	Power to device during implementation of the ***D3$_{cold}$*** state required by PCI Power Management Interface specification.
PME#	81	O	PME# output.
VAUXP	82	I	V_{AUX} support detection. V_{AUXP} pin is driven high to indicate that ACPI is supported with ***D3$_{cold}$*** state. No V_{AUX} support when driven low.
PCICLK	84	I	PCI bus clock. Functions as PCI CLK pin and operates at 33 MHz.
INTA#	86	O	Interrupt A. Used to request an interrupt from the PCI bus.
PAR	87	I/O	Parity. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction.
FRAME#	89	I/O	Cycle frame. FRAME# is driven by the current master to indicate the beginning and duration of an access. FRAME# is asserted to indicate the start of a bus transaction. When FRAME# is deasserted, the transaction is in the final data phase or has been completed.
IRDY#	91	I/O	Initiator ready. IRDY# is used in conjuction with TRDY# and indicates the bus master's ability to complete the current data phase of a transaction. During a write transaction, IRDY# indicates that valid data is present on AD[16:31] and AD[0:15]. During a read transaction, IRDY# indicates that master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together.
STOP#	92	I/O	Stop. STOP# indicates the current target is requesting the master to stop the current transaction.
TRDY#	95	O	Target ready. TRDY# is used in conjuction with IRDY# and indicates the bus master's ability to complete the current data phase of a transaction. During a write transaction, TRDY# indicates that valid data is present on AD[16:31] and AD[0:15]. During a read transaction, TRDY# indicates that master is prepared to accept data. Wait cycles are inserted until both TRDY# and IRDY# are asserted together.
IDSEL	96	O	Initialization device select. IDSEL is used as a chip select during configuration read and write transactions.
DEVSEL#	97	O	Device select. When actively driven, DEVSEL# indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
RESET#	88	I	Active-low ES2898 reset input.
DAA_PM#	94	O	DAA power control output.

Table 2 ES2828 Pin Descriptions

Names	Pin Numbers	I/O	Definitions
GPIO_A	1	I	Reserved.
GPIO_B	2	I/O	Reserved.
DVDD	3, 23, 29	P	3.3V digital power.
AGND	4:6, 18	I	Analog ground.
AUX+	7	I	Codec analog auxiliary differential positive input. The DC level is VCM, and the full-scale input is either 0.22 Vp-p ±5% or 1.1 Vp-p±5%, depending on the gain setting.
AUX–	8	I	Codec analog auxiliary differential negative input. The DC level is VCM, and the full-scale input is either 0.22 Vp-p ±5% or 1.1 Vp-p±5%, depending on the gain setting.
RXIN+	9	I	Codec analog differential positive input. The DC level is VCM, and the full-scale input is either 0.22 Vp-p ±5% or 1.1 Vp-p±5%, depending on the gain setting.
RXIN–	10	I	Codec analog differential negative input. The DC level is VCM, and the full-scale input is either 0.22 Vp-p ±5% or 1.1 Vp-p±5%, depending on the gain setting.
AVDD	11	I	Analog 5.0V supply.
VCM	12	O	Common mode voltage bypass 1. Has a range of 2.16V±5%. Bypass to VCBP with 0.1-μF ceramic chip capacitor parallel with 10-μF-tantalum capacitor.
VCBP	13	I	Ground for VCM.
VREF	14	O	Voltage reference bypass. Has a range of 1.2356V±5%. Bypass to VRBP with 0.1-μF ceramic chip capacitor parallel with 10-μF tantalum capacitor.
VRBP	15	I	Ground for VREF.
TX+	16	O	Codec positive analog output. The DC level is VCM, and the full-scale AC output is either 2.8V p-p±5% or 1.4V p-p±5%, depending on the gain setting. The maximum loading is 1k Ω, in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD <–60 db) current is 10 mA rms.
TX–	17	O	Codec negative analog output. The DC level is VCM, and the full-scale AC output is either 2.8V p-p±5% or 1.4V p-p±5%, depending on the gain setting. The maximum loading is 1k Ω, in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD <–60 db) current is 10 mA rms.
VCMX	19	O	Codec common mode reference voltage output. 2.16V±5%, maximum current ±500 μA, maximum capacitive load 20 pF.
HCT	20	I	Codec digital input mode control.
DGND	21, 44	P	Digital ground.
CTST	22	I	Codec sigma delta modulator test port output enable.
SI	24	I	Serial port input (default).
SO	25	O	Serial port output without V_{AUX} support.
SC	26	I/O	Serial port clock output. While input must be TTL-compatible, should be able to handle 3.3V input.
FS	27	O	Serial port frame sync.
CKO	28	O	3.3V clock output.
XTALO	30	O	Crystal oscillator output.
XTALI	31	I	Crystal oscillator input.
RST#	32	I	Reset.
ID1	33	I	Reserved.

Table 2 ES2828 Pin Descriptions (Continued)

Names	Pin Numbers	I/O	Definitions
PWDN#	34	I	Power down.
ID0	35	I	Reserved.
SDATA_IN	36	O	Reserved.
V_{AUX}	37	I	Auxiliary power to device during implementation of ***D3$_{cold}$*** state required by PCI power management interface specification.
GPIO_0	38	I/O	Reserved.
GPIO_1	39	I/O	Reserved.
GPIO_2	40	I/O	Reserved.
GPIO_3	41	I/O	Reserved.
GPIO_4	42	I/O	Reserved.
GPIO_5	43	I/O	Reserved.
GPIO_6	45	I/O	Reserved.
GPIO_7	46	I/O	Reserved.
GPIO_8	47	I/O	Reserved.
GPIO_9	48	I/O	Reserved.

ORDERING INFORMATION

Part Numbers	Descriptions	Packages
ES2898S	DSP Modem	100-pin LQFP
ES2828S	Modem Analog Front-End	48-pin LQFP

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