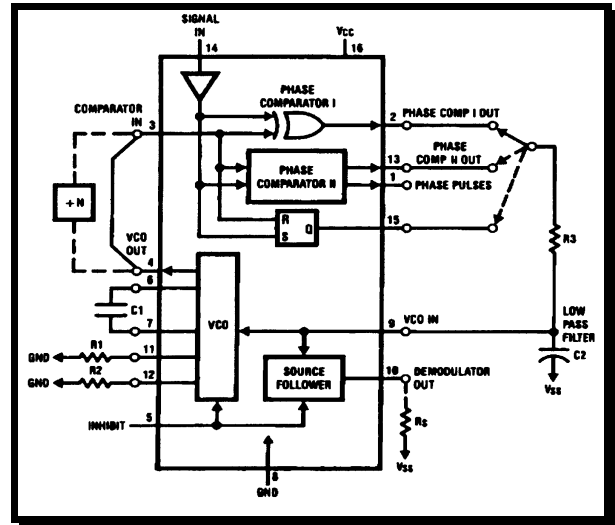
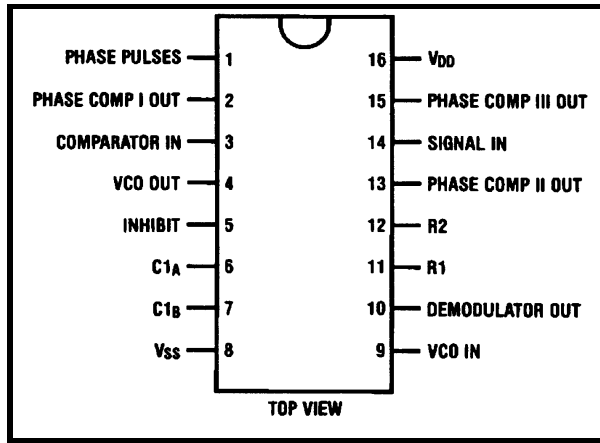


SEi - Radiation Hardened 54HC4046RP

Phase-Locked Loop



Features

- RAD-PAK[®] Technology Hardened Against Natural Space Radiation
- Total Dose Hardness >100 krad (Si)
- Low Power Phase Lock Loop
- Package:
 - 16 Pin RAD-PAK[®] Flat Package
 - 16 Pin RAD-PAK[®] DIP
- Low Dynamic Power Consumption
 - $V_{CC} = 4.5V$
- Maximum VCO Operating Frequency
 - 12 MHz ($V_{CC} = 4.5V$)
- Fast Comparator Response Time ($V_{CC} = 4.5V$)
 - Comparator I: 25 ns
 - Comparator II: 30 ns
 - Comparator III: 25 ns
- Screening per TM 5004
- QCI per TM5005

SEi's 54HC4046RP (RP for RAD-PAK[®]) high speed Phase Lock Loop microcircuit features a 100 kilorad (Si) total dose tolerance. This device uses advanced CMOS technology to obtain high frequency operation. The 54HC4046RP contains a low power linear voltage controlled oscillator (VCO), a source follower, and three phase comparators. The three phase comparators have a common signal input and a common comparator input. The signal input has a self biasing amplifier allowing signals to be either capacitively coupled to the phase comparators with a small signal or directly coupled with standard input logic levels. Any one of the three comparators feeds an external filter network, which in turn feeds the VCO input. This input is a very high impedance CMOS input that also drives the source follower. An inhibit pin is provided to disable the VCO and the source follower, providing a method of putting the IC in a low power state. Capable of surviving space environments, the 54HC4046RP is ideal for many satellite, spacecraft, and space probe missions. The radiation hardened RAD-PAK[®] technology incorporates radiation shielding in the microcircuit package. The 54HC4046RP is available in Class S packaging and screening.

Specifications and design are subject to change without notice.

1



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SEi - Radiation Hardened 54HC4046RP

Phase-Locked Loop

54HC4046RP ABSOLUTE MAXIMUM RATINGS 1/ 2/

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V _{CC}	-0.5	+7.0	V
DC Input Voltage	V _{IN}	-0.5	V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5	V _{CC} +0.5	V
Clamp Diode Current	I _{IK} , I _{OK}		+20	mA
DC Output Current, per pin	I _{OUT}		+25	mA
DC V _{CC} or GND Current, per pin	I _{CC}		±50	mA
Storage Temperature Range	T _{STG}	-65	+150	°C
Power Dissipation	P _D		500	mW

54HC4046RP OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V _{CC}	+2.0	+6.0	V
DC Input or Output Voltage	V _{IN} , V _{OUT}	0	V _{CC}	V
Operating Temperature Range	T _A	-55	+125	°C
Input Rise or Fall Times	t _r , t _f			ns
V _{CC} = 2.0V		0	1000	
V _{CC} = 4.5V		0	500	
V _{CC} = 6.0V		0	400	

Note:

- 1/ Maximum Ratings are those values beyond which damage to the device may occur.
 2/ All voltages are referenced to ground, unless otherwise specified.

54HC4046RP DC ELECTRICAL CHARACTERISTICS¹

PARAMETER	SYMBOL	TYP	MAX	UNIT
Minimum High Level Input Voltage V _{CC} = 2.0V V _{CC} = 4.5V V _{CC} = 6.0V	V _{IH}		1.5 3.15 4.2	V
Maximum Low Level Input Voltage V _{CC} = 2.0V V _{CC} = 4.5V V _{CC} = 6.0V	V _{IL}		0.5 1.35 1.8	V
Minimum High Level Output Voltage V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20µA V _{CC} = 2.0V V _{CC} = 4.5V V _{CC} = 6.0V V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0mA @ V _{CC} = 4.5V I _{OUT} < 5.2mA @ V _{CC} = 6.0V	V _{OH}	2.0 4.5 6.0	1.9 4.4 5.9	V
Maximum Low Level Output Voltage V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20µA V _{CC} = 3.0V V _{CC} = 4.5V V _{CC} = 6.0V V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0mA @ V _{CC} = 4.5V I _{OUT} < 5.2mA @ V _{CC} = 6.0V	V _{OL}		0.1 0.1 0.1 0.4 0.4	V
Input Current V _{IN} = V _{CC} or GND @ V _{CC} = 6.0V Pin 3, 5, 9 Pin 14	I _{IN}		±1.0 100	µA
Maximum Tri-State Output Leakage Current (pin 13) V _{OUT} = V _{CC} or GND @ V _{CC} = 6.0V	I _{OZ}		±10	µA
Maximum Quiescent Supply Current V _{IN} = V _{CC} or GND, I _{OUT} = 0µA, @ V _{CC} = 6.0V V _{IN} = V _{CC} or GND, Pin 14 Open, @ V _{CC} = 6.0V	I _{CC}	30 600	160 3000	µA

Note:

1. For a power supply of 5V ± 10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.



SEi - Radiation Hardened 54HC4046RP

Phase-Locked Loop

54HC4046RP AC ELECTRICAL CHARACTERISTICS 2/

PARAMETER	SYMBOL	TYP 3/	MAX	UNIT
AC Coupled Input Sensitivity, Signal In C(series) = 100 pF, $f_{IN} = 500$ kHz $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$			200 250 350	mV
Maximum Output Rise and Fall Time $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_r, t_f		110 22 19	ns
PHASE COMPARATOR I				
Maximum Propagation Delay $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_{PHL}, t_{PLH}		300 60 51	ns
PHASE COMPARATOR II				
Maximum Tri-State Enable Time $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_{PZL}		340 68 57	ns
Maximum Tri-State Enable Time $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_{PZH}, t_{PHZ}		360 72 61	ns
Maximum Tri-State Disable Time $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_{PLZ}		360 72 61	ns
Maximum Propagation Delay High to Low to Phase Pulses $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_{PHL}, t_{PLH}		380 75 64	ns
PHASE COMPARATOR III				
Maximum Propagation Delay $V_{CC} = 2.0V$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	t_{PHL}, t_{PLH}		300 60 51	ns
Maximum Power Dissipation Capacitance All comparators, $V_{IN} = V_{CC}$ and GND	CPD	130		pF
VOLTAGE CONTROLLED OSCILLATOR (operate @ $V_{CC} = 3.0V$ to $6.0V$)				
Maximum Operating Frequency $C_1 = 50pF, R_1 = 100\Omega, R_2 = \infty$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$ $V_{COin} = V_{CC}, C_1 = 0pF, R_1 = 100\Omega, V_{COin} = V_{CC}$ $V_{CC} = 4.5V$ $V_{CC} = 6.0V$	f_{MAX}		7 11 12 14	MHz
Duty Cycle		50		%
DEMODULATOR OUTPUT				
Offset Voltage ($V_{COin} - V_{dem}$) $R_S = 20k\Omega, V_{CC} = 4.5V$			1.6	V
Offset Variation $R_S = 20k\Omega, V_{CC} = 4.5V$ $V_{COin} = 1.75V$ $V_{COin} = 2.25V$ $V_{COin} = 2.75V$		0.65 0.1 0.75		V

Note:

2/ $V_{CC} = 2.0$ to $6.0V, C_L = 50pF, t_r = t_f = 6ns$ (unless otherwise specified.)
3/ $T_A = 25^\circ C.$



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SEi - Radiation Hardened **54HC4046RP** Phase-Locked Loop

54HC4046RP Package Ordering Guide

Package Style	Case Outline	Description
D	D-16	16 Pin Dual In Line Package
F	F-16A	16 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

54HC4046RP PINOUT

PIN	SIGNAL	DESCRIPTION
1	PHASE PULSES	Phase Comparator Pulse Output
2	PHASE COMP 1 OUT	Phase Comparator 1 Output
3	COMPARATOR IN	Comparator Input
4	VCO OUT	VCO Output
5	INHIBIT	Inhibit Input
6	C1A	Capacitor C1 Connection A
7	C1B	Capacitor C1 Connection B
8	VSS	Ground
9	VCO IN	VCO Input
10	DEMODULATOR OUT	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	PHASE COMP II OUT	Phase Comparator 2 Output
14	SIGNAL IN	Signal Input
15	PHASE COMP III OUT	Phase Comparator 3 Output
	VDD	Positive Supply Voltage



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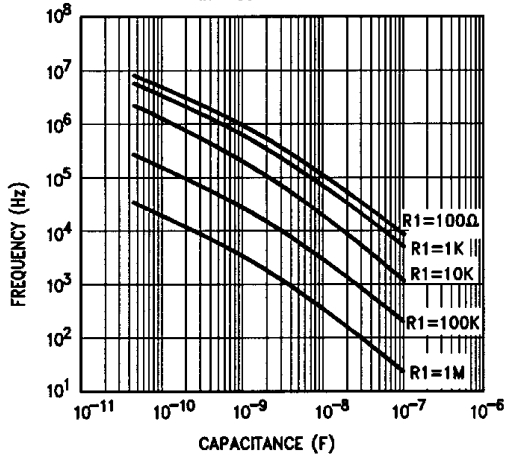
SEi- Radiation Hardened 54HC4046RP

Phase-Locked Loop

Typical Performance Characteristics

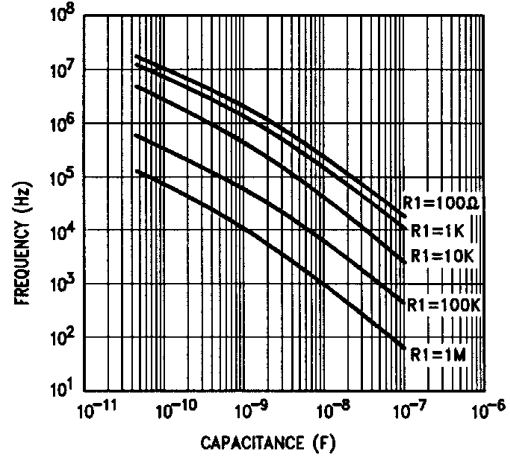
Typical Center Frequency
vs R1, C1 V_{CC} = 4.5V

V_{COIN}=V_{CC}/2 R2=OPEN



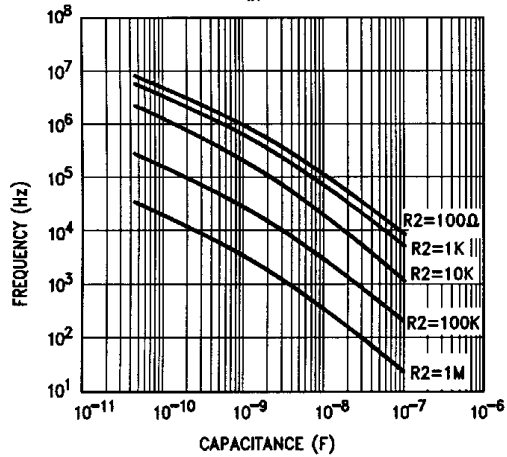
Typical Center Frequency
vs R1, C1 V_{CC} = 6V

V_{COIN}=V_{CC}/2 R2=OPEN



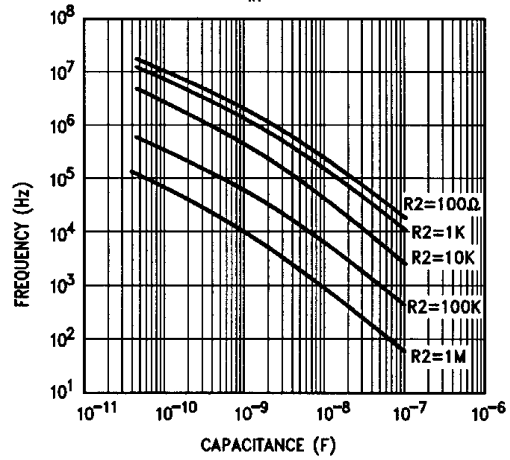
Typical Offset Frequency
vs R2, C1 V_{CC} = 4.5V

T=25°C V_{COIN}=GND R1=OPEN



Typical Offset Frequency
vs R2, C1 V_{CC} = 6V

T=25°C V_{COIN}=GND R1=OPEN



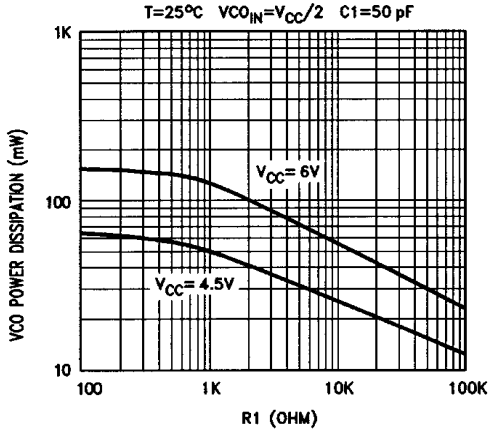
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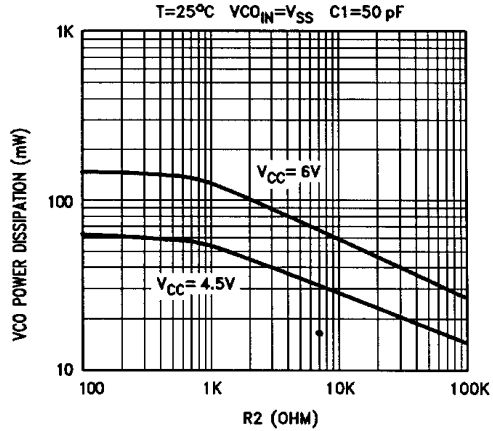
Phase-Locked Loop

Typical Performance Characteristics (Continued)

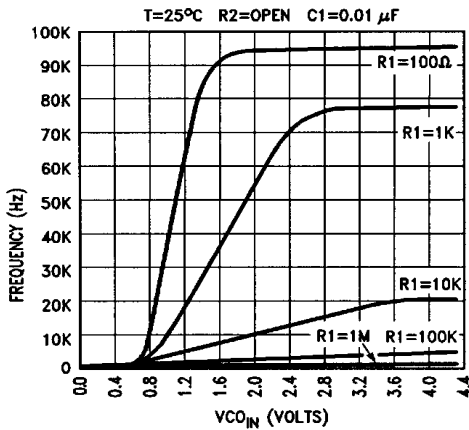
HC4046 Typical VCO Power Dissipation @ Center Frequency vs R1



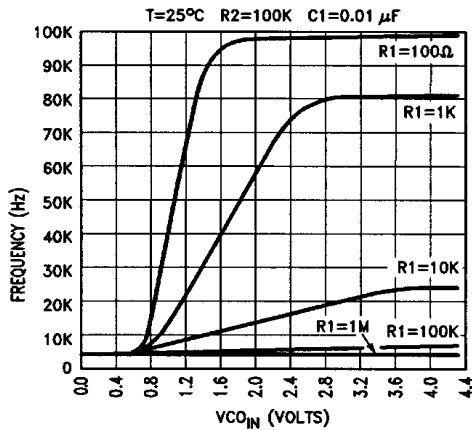
HC4046 Typical VCO Power Dissipation @ f_{min} vs R2



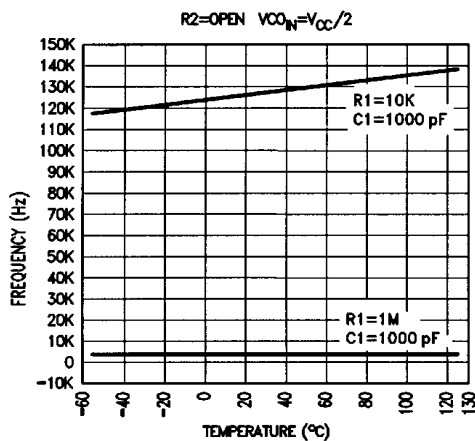
HC4046 VCO_{IN} vs f_{out} V_{CC} = 4.5V



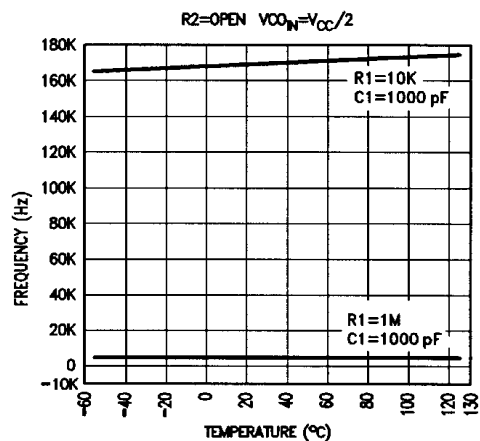
HC4046 VCO_{IN} vs f_{out} V_{CC} = 4.5V



HC4046 VCO_{out} vs Temperature V_{CC} = 4.5V



HC4046 VCO_{out} vs Temperature V_{CC} = 6V



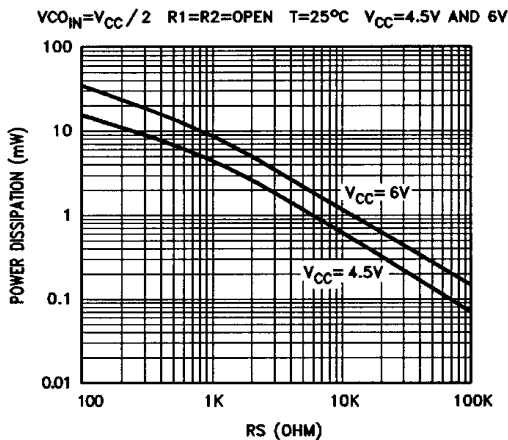
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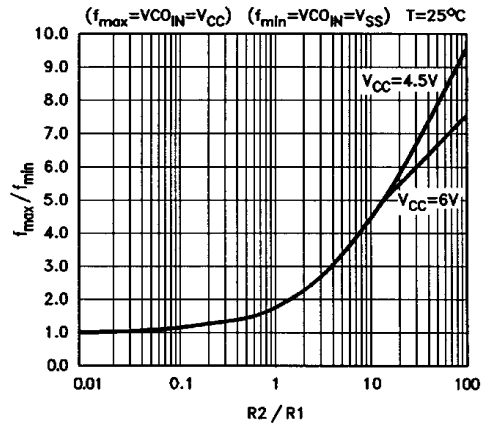
Phase-Locked Loop

Typical Performance Characteristics (Continued)

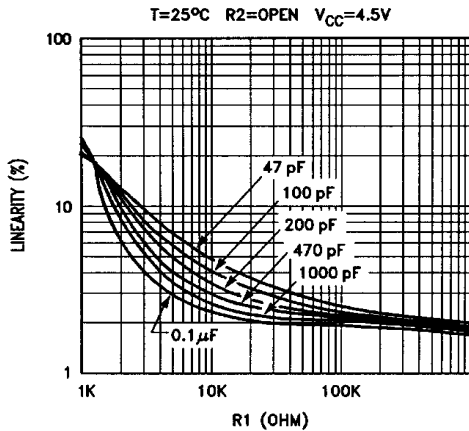
HC4046 Typical Source Follower Power Dissipation vs RS



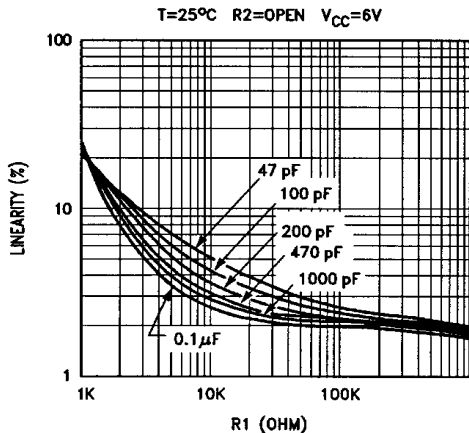
Typical f_{max}/f_{min} vs $R2/R1$
 $V_{CC} = 4.5V$ & $6V$ f_{max}/f_{min}



HC4046 Typical VCO Linearity vs R1 & C1

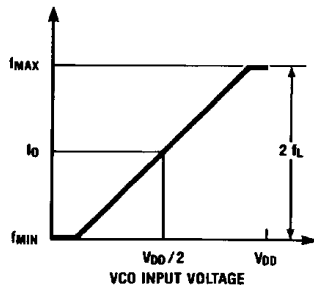


HC4046 Typical VCO Linearity vs R1 & C1

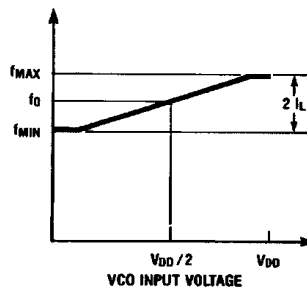


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VCO WITHOUT OFFSET
 $R2 = \infty$



VCO WITH OFFSET



(a)

FIGURE 1

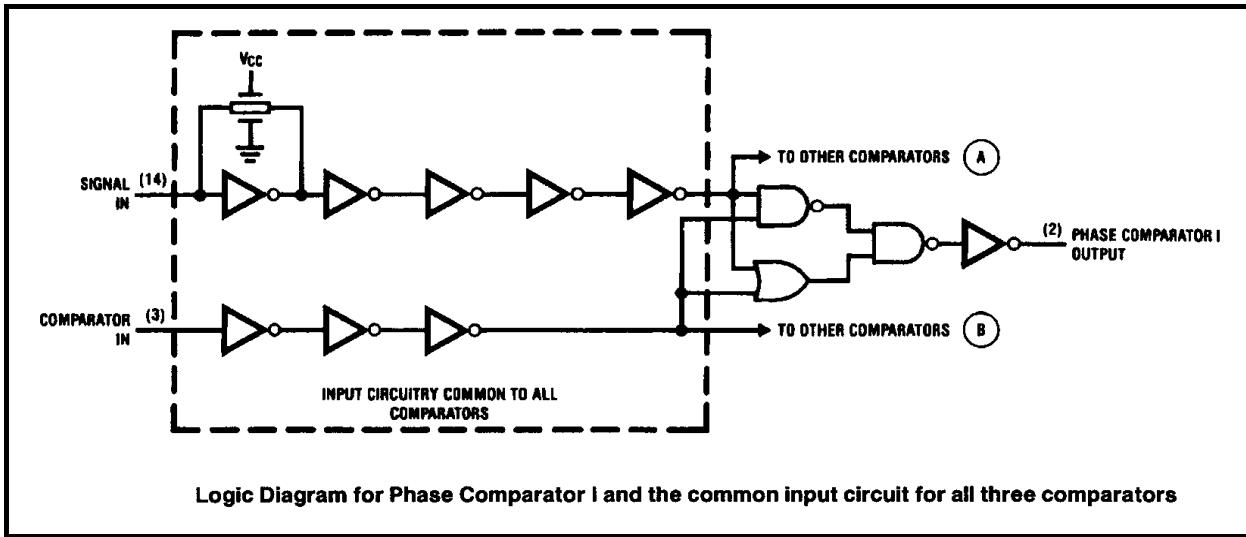
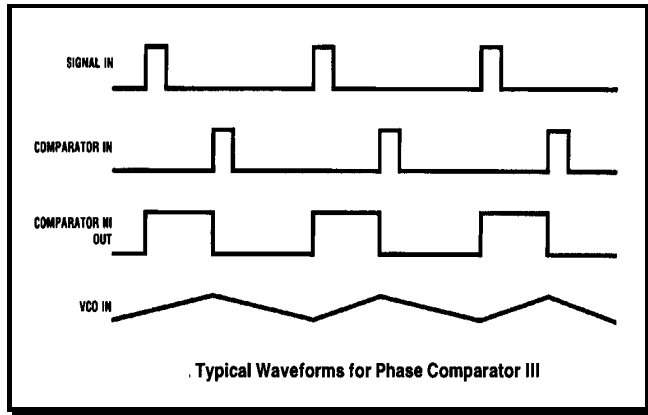
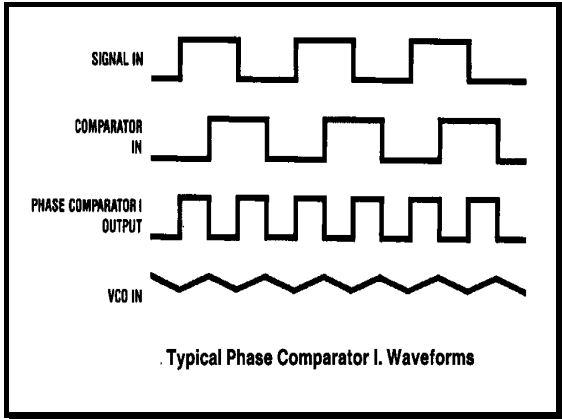
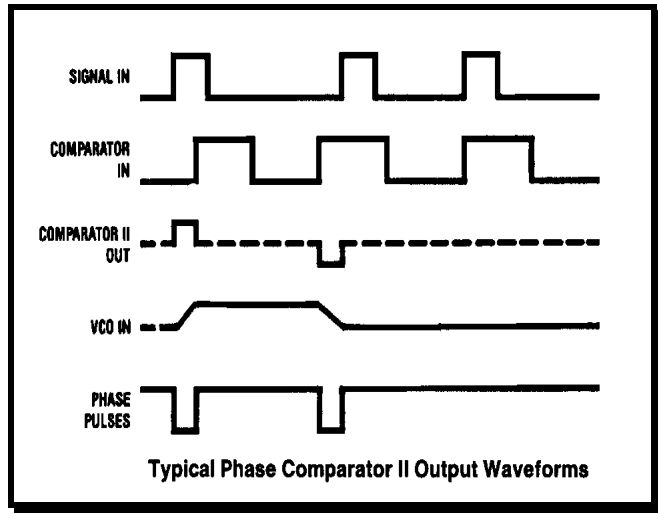
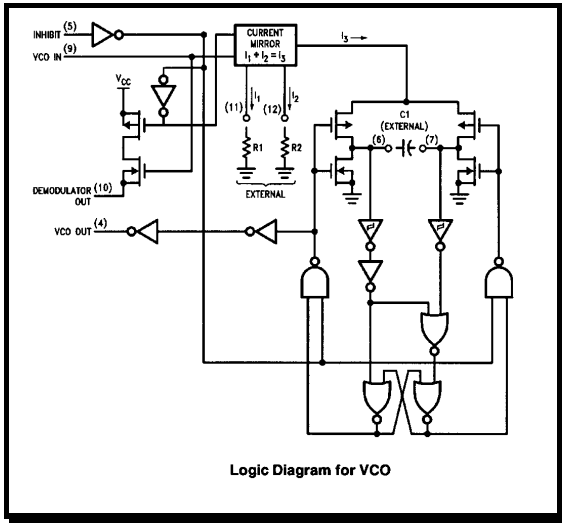


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