

GENERAL DESCRIPTION

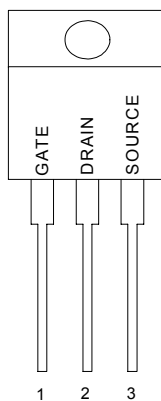
This Power MOSFET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

FEATURES

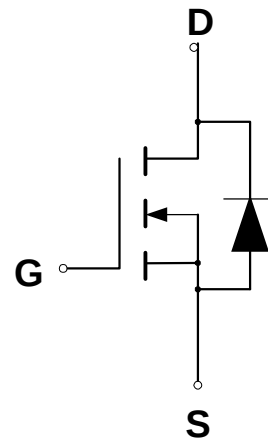
- ◆ Silicon Gate for Fast Switching Speeds
- ◆ Low $R_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- ◆ Rugged – SOA is Power Dissipation Limited
- ◆ Source-to-Drain Characterized for Use With Inductive Loads

PIN CONFIGURATION

TO-220
Front View



SYMBOL



N-Channel MOSFET

ORDERING INFORMATION

Part Number	Package
CMT18N20N220	TO-220

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain to Current – Continuous	I_D	18	A
– Pulsed	I_{DM}	72	
Gate-to-Source Voltage – Continue	V_{GS}	± 20	V
– Non-repetitive	V_{GSM}	± 40	V
Total Power Dissipation	P_D	125	W
Derate above 25°C		1.00	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy – $T_J = 25^\circ\text{C}$ ($V_{DD} = 100\text{V}$, $V_{GS} = 10\text{V}$, $I_L = 18\text{A}$, $L = 1.38\text{mH}$, $R_G = 25\Omega$)	E_{AS}	224	mJ
Thermal Resistance – Junction to Case	θ_{JC}	1.00	°C/W
– Junction to Ambient	θ_{JA}	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

(1) Pulse Width and frequency is limited by $T_J(\text{max})$ and thermal response

ELECTRICAL CHARACTERISTICS

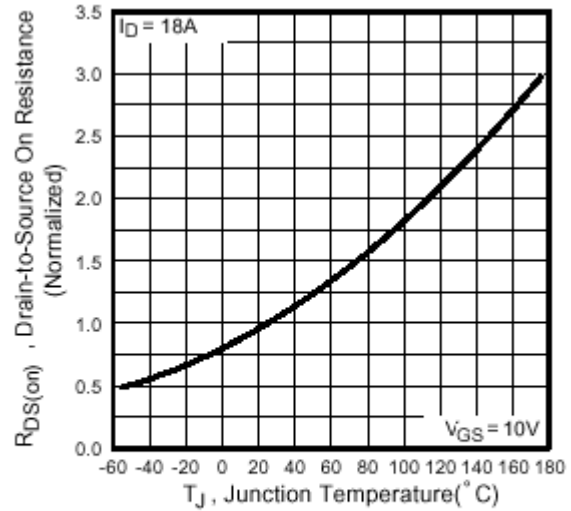
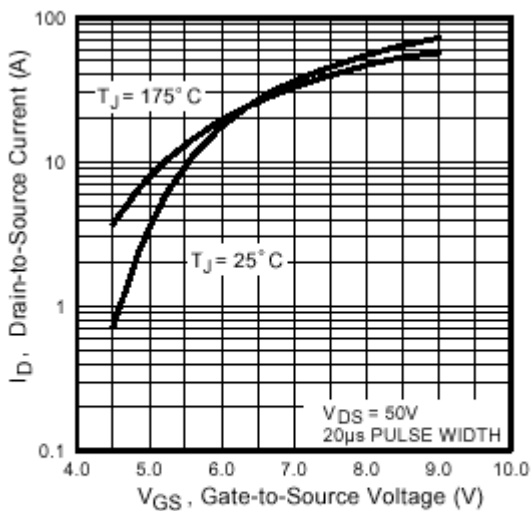
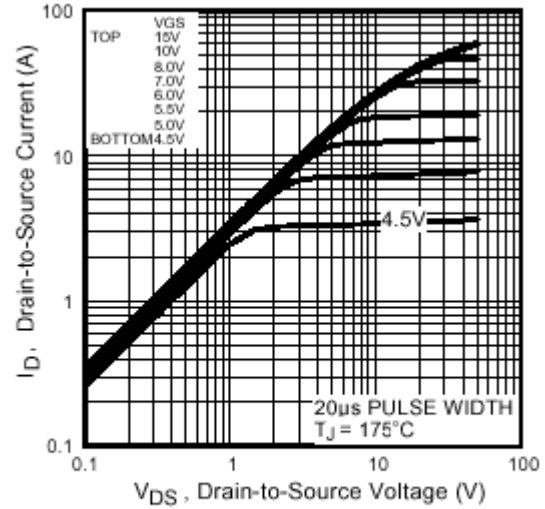
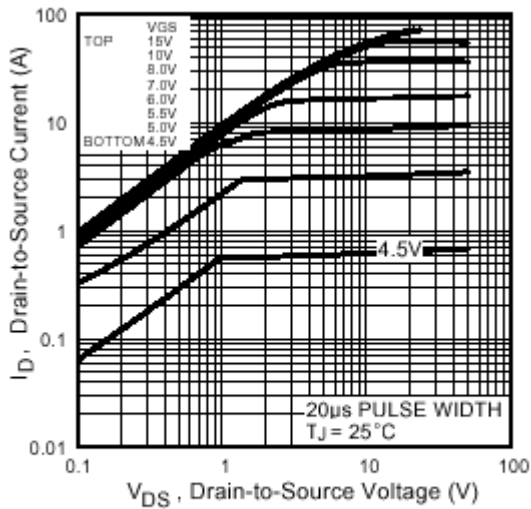
Unless otherwise specified, $T_J = 25^\circ\text{C}$.

		CMT18N20				
Characteristic		Symbol	Min	Typ	Max	Units
Drain-Source Breakdown Voltage (V _{GS} = 0 V, I _D = 250 μA)		V _{(BR)DSS}	200			V
Drain-Source Leakage Current (V _{DS} = Rated V _{DSS} , V _{GS} = 0 V) (V _{DS} = 0.8Rated V _{DSS} , V _{GS} = 0 V, T _J = 125°C)		I _{DSS}			0.025 1.0	mA
Gate-Source Leakage Current-Forward (V _{gsf} = 20 V, V _{DS} = 0 V)		I _{GSSF}			100	nA
Gate-Source Leakage Current-Reverse (V _{gsr} = 20 V, V _{DS} = 0 V)		I _{GSSR}			100	nA
Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μA)		V _{GS(th)}	2.0		4.0	V
Static Drain-Source On-Resistance (V _{GS} = 10 V, I _D = 10A) *		R _{DS(on)}			0.18	Ω
Drain-Source On-Voltage (V _{GS} = 10 V) (I _D = 5.0 A)		V _{DS(on)}			6.0	V
Forward Transconductance (V _{DS} = 50 V, I _D = 10 A) *		g _{FS}	6.8			mhos
Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz)	C _{iss}			1600	pF
Output Capacitance		C _{oss}			750	pF
Reverse Transfer Capacitance		C _{rss}			300	pF
Turn-On Delay Time	(V _{DD} = 30 V, I _D = 10 A, V _{GS} = 10 V, R _G = 4.7Ω) *	t _{d(on)}			30	ns
Rise Time		t _r			60	ns
Turn-Off Delay Time		t _{d(off)}			80	ns
Fall Time		t _f			60	ns
Total Gate Charge	(V _{DS} = 0.8Rated V _{DSS} , I _D = Rated I _D , V _{GS} = 10 V)*	Q _g		36	63	nC
Gate-Source Charge		Q _{gs}		16		nC
Gate-Drain Charge		Q _{gd}		26		nC
Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die)		L _D		4.5		nH
Internal Drain Inductance (Measured from the source lead 0.25" from package to source bond pad)		L _S		7.5		nH
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage(1)	(I _S = Rated I _D , d _{IS} /d _t = 100A/μs)	V _{SD}			1.5	V
Forward Turn-On Time		t _{on}		**		ns
Reverse Recovery Time		t _{rr}		450		ns

* Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$

** Negligible, Dominated by circuit inductance

TYPICAL ELECTRICAL CHARACTERISTICS



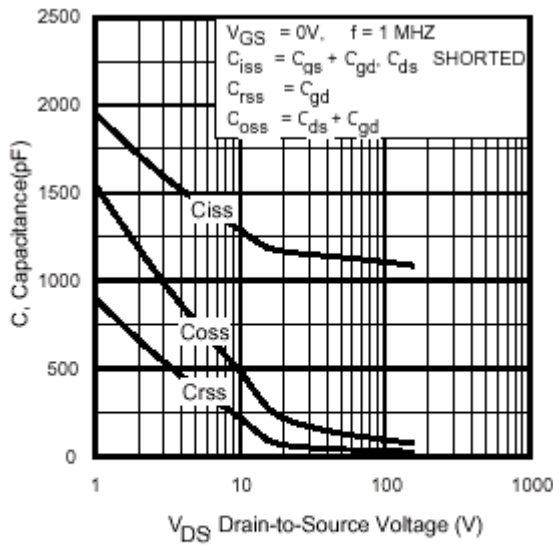


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

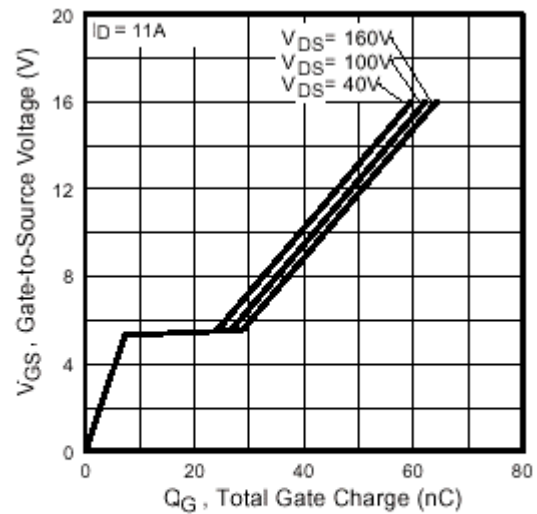


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

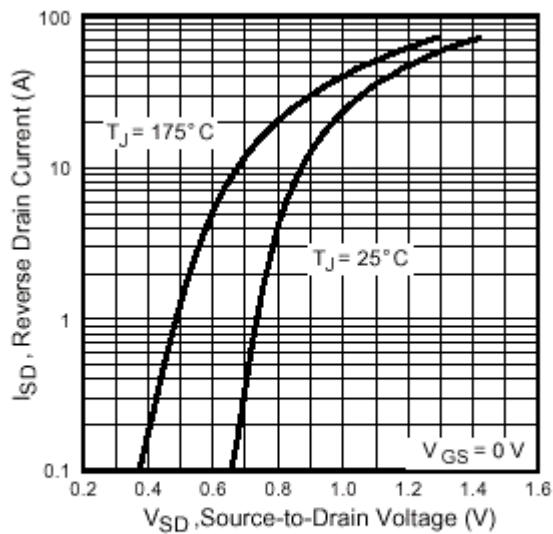


Fig 7. Typical Source-Drain Diode Forward Voltage

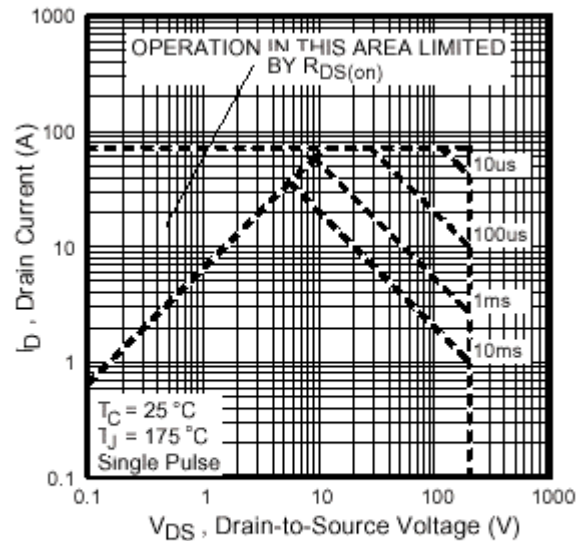


Fig 8. Maximum Safe Operating Area

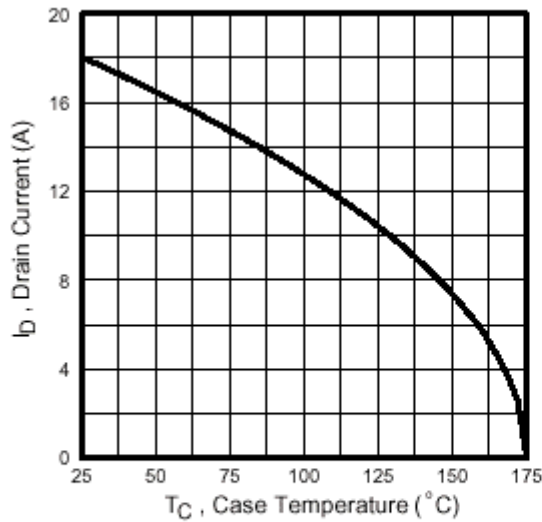


Fig 9. Maximum Drain Current Vs. Case Temperature

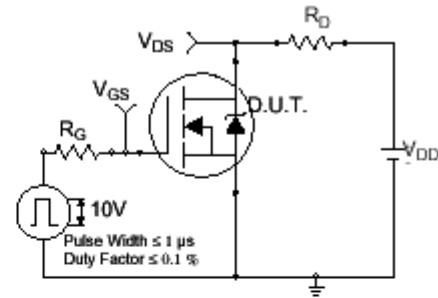


Fig 10a. Switching Time Test Circuit

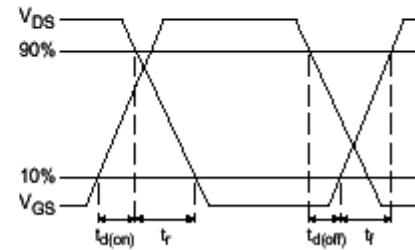


Fig 10b. Switching Time Waveforms

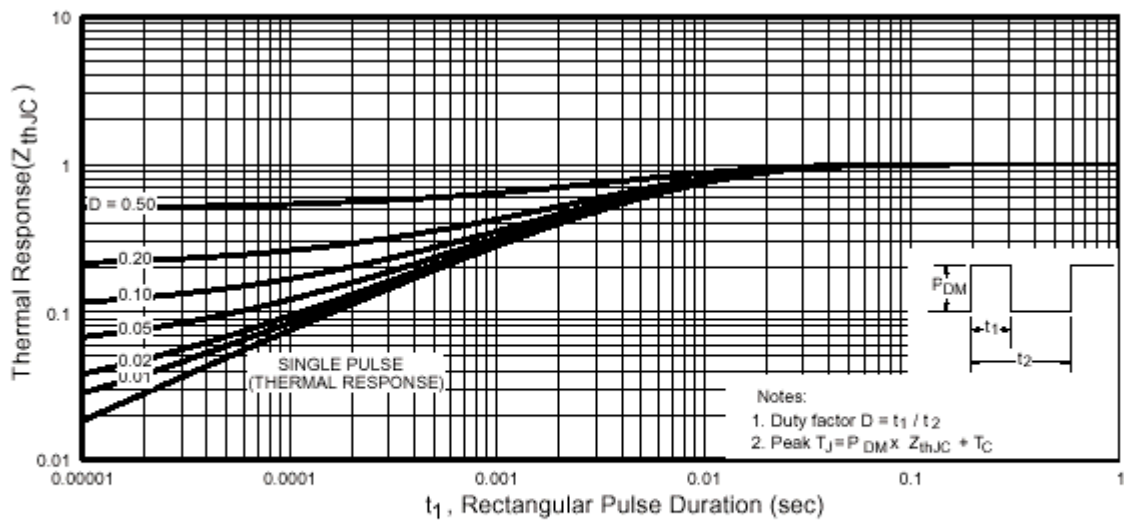
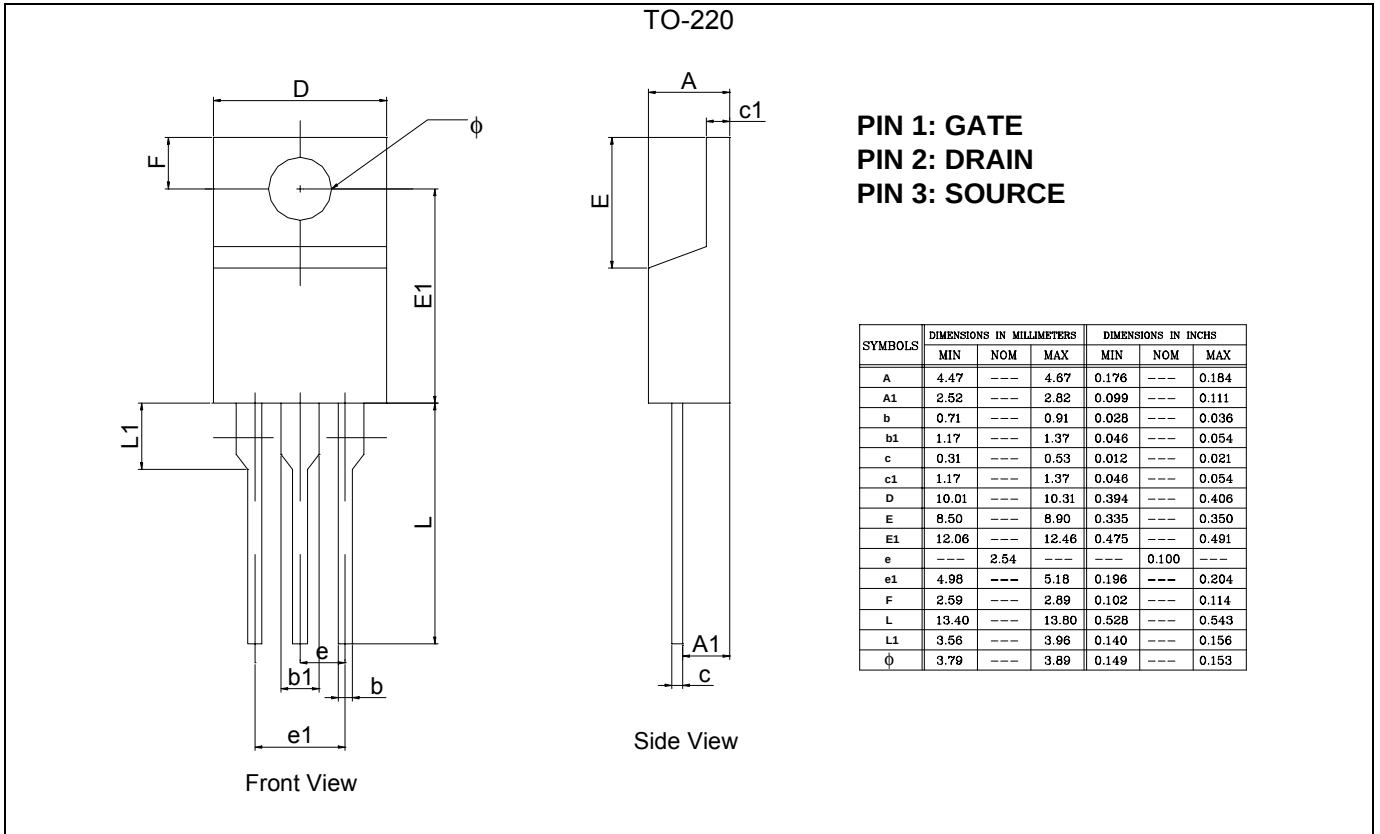


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

PACKAGE DIMENSION



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