STANDARD MICROSYSTEMS CORPORATION

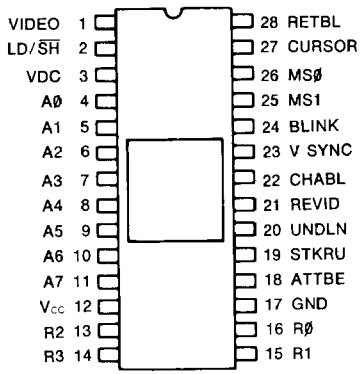
CRT 8002
μPC FAMILY

CRT Video Display Attributes Controller Video Generator VDAC™

FEATURES

- ☐ On chip character generator (mask programmable)
  - 128 Characters (alphanumeric and graphic)
  - 7 x 11 Dot matrix block
- ☐ On chip video shift register
  - Maximum shift register frequency
    - CRT 8002A 20MHz
    - CRT 8002B 15MHz
    - CRT 8002C 10MHz
    - Access time 400ns
- ☐ On chip horizontal and vertical retrace video blanking
- ☐ No descender circuitry required
- ☐ Four modes of operation (intermixable)
  - Internal character generator (ROM)
  - Wide graphics
  - Thin graphics
  - External inputs (fonts/dot graphics)
- ☐ On chip attribute logic—character, field
  - Reverse video
  - Character blank
  - Character blink
  - Underline
  - Strike-thru
- ☐ Four on chip cursor modes
  - Underline
  - Blinking underline
  - Reverse video
  - Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ Subscriptable
- ☐ Expandable character set
  - External fonts
  - Alphanumeric and graphic
  - RAM, ROM, and PROM
- ☐ On chip address buffer
- ☐ On chip attribute buffer
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology—ROM and options
- ☐ Compatible with CRT 5027 VTAC®

PIN CONFIGURATION



SECTION V

General Description

The SMC CRT 8002 Video Display Attributes Controller (VDAC) is an N-channel COPLAMOS® MOS/LSI device which utilizes CLASP® technology. It contains a 7X11X128 character generator ROM, a wide graphics mode, a thin graphics mode, an external input mode, character address/data latch, field and/or character attribute logic, attribute latch, four cursor modes, two programmable blink rates, and a high speed video shift register. The CRT 8002 VDAC™ is a companion chip to SMC's CRT 5027 VTAC. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

The CRT 8002 video output may be connected directly to a CRT monitor video input. The CRT 5027 blanking output can be connected directly to the CRT 8002 retrace blank input to provide both horizontal and vertical retrace blanking of the video output.

Four cursor modes are available on the CRT 8002. They are: underline, blinking underline, reverse video block, and blinking reverse video block. Any one of these can be mask programmed as the cursor function. There is a separate cursor blink rate which can be mask programmed to provide a 15Hz to 1Hz blink rate.

The CRT 8002 attributes include: reverse video, character blank, blink, underline, and strike-thru. The character blink rate is mask programmable from 7.5Hz to 0.5Hz and has a duty cycle of 75/25. The underline and strike-thru are similar but independently controlled functions and can be mask programmed to any number of raster lines at any position in the character block. These attributes are available in all modes.

In the wide graphic mode the CRT 8002 produces a graphic entity the size of the character block. The graphic entity contains 8 parts, each of which is associated with one bit of a graphic byte, thereby providing for 256 unique graphic symbols. Thus, the CRT 8002 can produce either an alphanumeric symbol or a graphic entity depending on the mode selected. The mode can be changed on a per character basis.

The thin graphic mode enables the user to create single line drawings and forms.

The external mode enables the user to extend the on-chip ROM character set and/or the on-chip graphics capabilities by inserting external symbols. These external symbols can come from either RAM, ROM or PROM.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

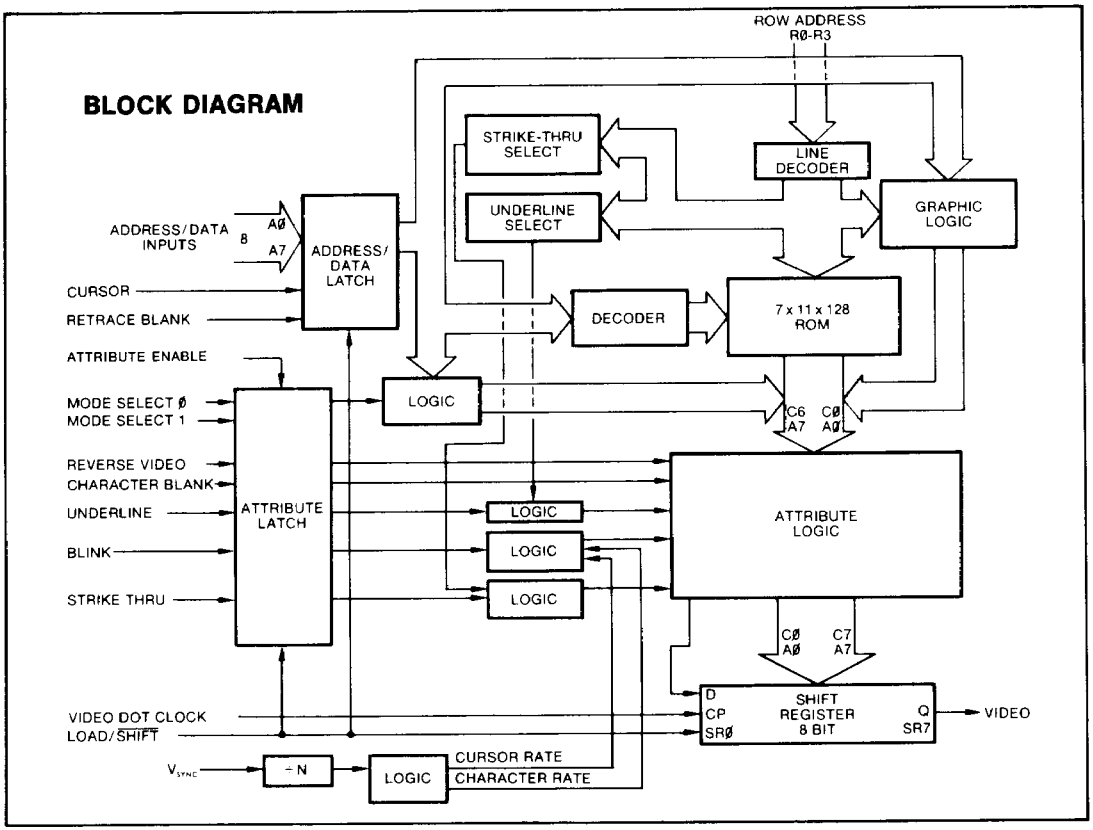
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding VDC
High-level, V_{IH}	2.0			V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}			0.8	V	
High-level, V_{IH}	4.3			V	See Figure 6
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	$I_{OL} = 0.4$ mA, 74LSXX load
High-level, V_{OH}	2.4			V	$I_{OH} = -20\mu A$
INPUT CURRENT					
Leakage, I_L (Except CLOCK)			10	μA	$0 \leq V_{IN} \leq V_{CC}$
Leakage, I_L (CLOCK Only)			50	μA	$0 \leq V_{IN} \leq V_{CC}$
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
LD/$\overline{SH}$		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	
A.C. CHARACTERISTICS					
See Figure 6, 7					

SYMBOL	PARAMETER	CRT 8002A		CRT 8002B		CRT 8002C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW_H	VDC—High Time	15.0		23		40		ns
PW_L	VDC—Low Time	15.0		23		40		ns
t_{CY}	LD/$\overline{SH}$ cycle time	400		533		800		ns
t_r, t_f	Rise, fall time		10		10		10	ns
$t_{SET\text{-}UP}$	Input set-up time	≥0		≥0		≥0		ns
t_{HOLD}	Input hold time	15		15		15		ns
t_{PDI}, t_{PDO}	Output propagation delay	15	50	15	65	15	100	ns
t_1	LD/$\overline{SH}$ set-up time	10		15		20		ns
t_2	LD/$\overline{SH}$ hold time	15		15		15		ns



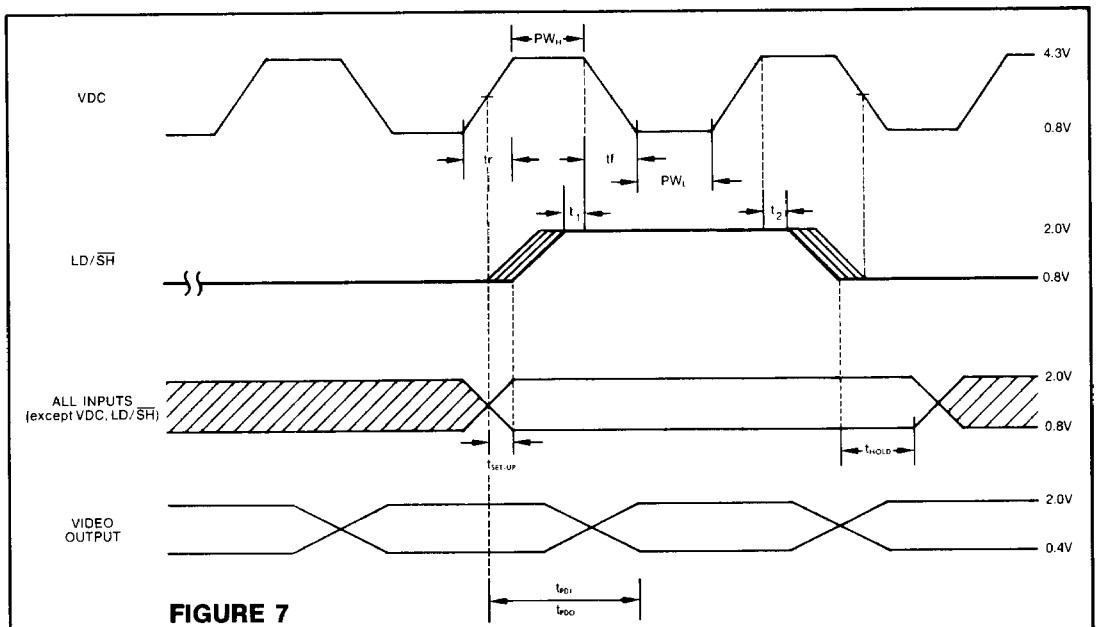


FIGURE 7
AC TIMING DIAGRAM

SECTION V

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
1	VIDEO	Video Output	O	The video output contains the dot stream for the selected row of the alpha-numeric, wide graphic, thin graphic, or external character after processing by the attribute logic, and the retrace blank and cursor inputs. In the alphanumeric mode, the characters are ROM programmed into the 77 dots, (7X11) allocated for each of the 128 characters. See figure 5. The top row (RØ) and rows R12 to R15 are normally all zeros as is column C7. Thus, the character is defined in the box bounded by R1 to R11 and CØ to C6. When a row of the ROM, via the attribute logic, is parallel loaded into the 8-bit shift-register, the first bit serially shifted out is C7 (A zero; or a one in REVID). It is followed by C6, C5, through CØ. The timing of the Load/$\overline{\text{Shift}}$ pulse will determine the number of additional (— —, zero to N) backfill zeros (or ones if in REVID) shifted out. See figure 4. When the next Load/$\overline{\text{Shift}}$ pulse appears the next character's row of the ROM, via the attribute logic, is parallel loaded into the shift register and the cycle repeats.
2	LD/$\overline{\text{SH}}$	Load/$\overline{\text{Shift}}$	I	The 8 bit shift-register parallel-in load or serial-out shift modes are established by the Load/$\overline{\text{Shift}}$ input. When low, this input enables the shift register for serial shifting with each Video Dot Clock pulse. When high, the shift register parallel (broadside) data inputs are enabled and synchronous loading occurs on the next Video Dot Clock pulse. During parallel loading, serial data flow is inhibited. The Address/Data inputs (AØ-A7) are latched on the negative transition of the Load/$\overline{\text{Shift}}$ input. See timing diagram, figure 7.
3	VDC	Video Dot Clock	I	Frequency at which video is shifted.
4-11	AØ-A7	Address/Data	I	In the Alphanumeric Mode the 7 bits on inputs (AØ-A6) are internally decoded to address one of the 128 available characters (A7 = X). In the External Mode, AØ-A7 is used to insert an 8 bit word from a user defined external ROM, PROM or RAM into the on-chip Attribute logic. In the wide Graphic Modes AØ-A7 is used to define one of 256 graphic entities. In the thin Graphic Mode AØ-A2 is used to define the 3 line segments.
12	V_{CC}	Power Supply	PS	+5 volt power supply
13,14,15,16	R2,R3,R1,RØ	Row Address	I	These 4 binary inputs define the row address in the current character block.
17	GND	Ground	GND	Ground
18	ATTBE	Attribute Enable	I	A positive level on this input enables data from the Reverse Video, Character Blank, Underline, Strike-Thru, Blink, Mode Select Ø, and Mode Select 1 inputs to be strobed into the on-chip attribute latch at the negative transition of the Load/$\overline{\text{Shift}}$ pulse. The latch loading is disabled when this input is low. The latched attributes will remain fixed until this input becomes high again. To facilitate attribute latching on a character by character basis, tie ATTBE high. See timing diagram, figure 7.
19	STKRU	Strike-Thru	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of strike-thru is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which strike-thru is to be placed as well as to program the strike-thru to be 1 to N raster lines high. Actually, the strike-thru decoder (mask programmable) logic allows the strike-thru to be any number or arrangement of horizontal lines in the character block. The standard strike-thru will be a double line on rows R5 and R6.
20	UNDLN	Underline	I	When this input is high and RETBL = 0, the parallel inputs to the shift register are forced high (SRØ-SR7), providing a solid line segment throughout the character block. The operation of underline is modified by Reverse Video (see table 1). In addition, an on-chip ROM programmable decoder is available to decode the line count on which underline is to be placed as well as to program the underline to be 1 to N raster lines high. Actually, the underline decoder (mask programmable) logic allows the underline to be any number or arrangement of horizontal lines in the character block. The standard underline will be a single line on R11.
21	REVID	Reverse Video	I	When this input is low and RETBL = 0, data into the Attribute Logic is presented directly to the shift register parallel inputs. When reverse video is high data into the Attribute Logic is inverted and then presented to the shift register parallel inputs. This operation reverses the data and field video. See table 1.
22	CHABL	Character Blank	I	When this input is high, the parallel inputs to the shift register are all set low, providing a blank character line segment. Character blank will override blink. The operation of Character Blank is modified by the Reverse Video input. See table 1.
23	V SYNC	V SYNC	I	This input is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will be twice the character blink rate (75/25 duty cycle). The divisors can be programmed from ÷ 4 to ÷ 30 for the cursor (÷ 8 to ÷ 60 for the character).
24	BLINK	Blink	I	When this input is high and RETBL = 0 and CHABL = 0, the character will blink at the programmed character blink rate. Blinking is accomplished by blanking the character block with the internal Character Blink clock. The standard character blink rate is 1.875 Hz.
25 26	MS1 MSØ	Mode Select 1 Mode Select Ø	I I	These 2 inputs define the four modes of operation of the CRT 8002 as follows: Alphanumeric Mode — In this mode addresses AØ-A6 (A7 = X) are internally decoded to address 1 of the 128 available ROM characters. The addressed character along with the decoded row will define a 7 bit output from the ROM to be loaded into the shift register via the attribute logic. Thin Graphics Mode — In this mode AØ-A2 (A3-A7 = X) will be loaded into the thin graphic logic along with the row addresses. This logic will define the segments of a graphic entity as defined in figure 2. The top of the entity will begin on row 0000 and will end on a mask programmable row.

MS1	MSØ	MODE
1	1	Alphanumeric
1	0	Thin Graphics
0	1	External Mode
0	0	Wide Graphics

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	NAME	INPUT/ OUTPUT	FUNCTION
25 26 (cont.)				External Mode – In this mode the inputs AØ-A7 go directly from the character latch into the shift register via the attribute logic. Thus the user may define external character fonts or graphic entities in an external PROM, ROM or RAM. See figure 3. Wide Graphics Mode –In this mode the inputs AØ-A7 will define a graphic entity as described in figure 1. Each line of the graphic entity is determined by the wide graphic logic in conjunction with the row inputs RØ to R3. In this mode each segment of the entity is defined by one of the bits of the 8 bit word. Therefore, the 8 bits can define any 1 of the 256 possible graphic entities. These entities can butt up against each other to form a contiguous pattern or can be interspaced with alphanumeric characters. Each of the entities occupies the space of 1 character block and thus requires 1 byte of memory. These 4 modes can be intermixed on a per character basis.
27	CURSOR	Cursor	I	When this input is enabled 1 of the 4 pre-programmed cursor modes will be activated. The cursor mode is on-chip mask programmable. The standard cursor will be a blinking (at 3.75Hz) reverse video block. The 4 cursor modes are: Underline—In this mode an underline (1 to N raster lines) at the programmed underline position occurs. Blinking Underline—In this mode the underline blinks at the cursor rate. Reverse Video Block—In this mode the Character Block is set to reverse video. Blinking Reverse Video Block—In this mode the Character Block is set to reverse video at the cursor blink rate. The Character Block will alternate between normal video and reverse video. The cursor functions are listed in table 1.
28	RETBL	Retrace Blank	I	When this input is latched high, the shift register parallel inputs are unconditionally cleared to all zeros and loaded into the shift register on the next Load/Shift pulse. This blanks the video, independent of all attributes, during horizontal and vertical retrace time.

TABLE 1

CURSOR	RETBL	REVID	CHABL	UNDLN*	FUNCTION
X	1	X	X	X	"0" (S.R. All
0	0	0	0	0	D (S.R.) All
0	0	0	0	1	"1" (S.R.)*
					D (S.R.) All others
0	0	0	1	X	"0" (S.R.) All
0	0	1	0	0	D (S.R.) All
0	0	1	0	1	"0" (S.R.)*
					D (S.R.) All others
0	0	1	1	X	"1" (S.R.) All
Underline*	0	0	0	X	"1" (S.R.)*
					D (S.R.) All others
Underline*	0	0	1	X	"1" (S.R.)*
					"0" (S.R.) All others
Underline*	0	1	0	X	"0" (S.R.)*
					D (S.R.) All others
Underline*	0	1	1	X	"0" (S.R.)*
					"1" (S.R.) All others
Blinking** Underline*	0	0	0	X	"1" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	0	1	X	"1" (S.R.)* Blinking
					"0" (S.R.) All others
Blinking** Underline*	0	1	0	X	"0" (S.R.)* Blinking
					D (S.R.) All others
Blinking** Underline*	0	1	1	X	"0" (S.R.)* Blinking
					"1" (S.R.) All others
REVID Block	0	0	0	0	D (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	0	1	X	"1" (S.R.) All
REVID Block	0	0	0	1	"0" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	0	0	D (S.R.) All
REVID Block	0	1	0	1	"1" (S.R.)*
					D (S.R.) All others
REVID Block	0	1	1	X	"0" (S.R.) All
Blink** REVID Block	0	0	0	0	Alternate Normal Video/REVID At Cursor Blink Rate
Blink** REVID Block	0	0	0	1	
Blink** REVID Block	0	0	1	X	
Blink** REVID Block	0	1	0	0	
Blink** REVID Block	0	1	0	1	
Blink** REVID Block	0	1	1	X	

*At Selected Row Decode **At Cursor Blink Rate

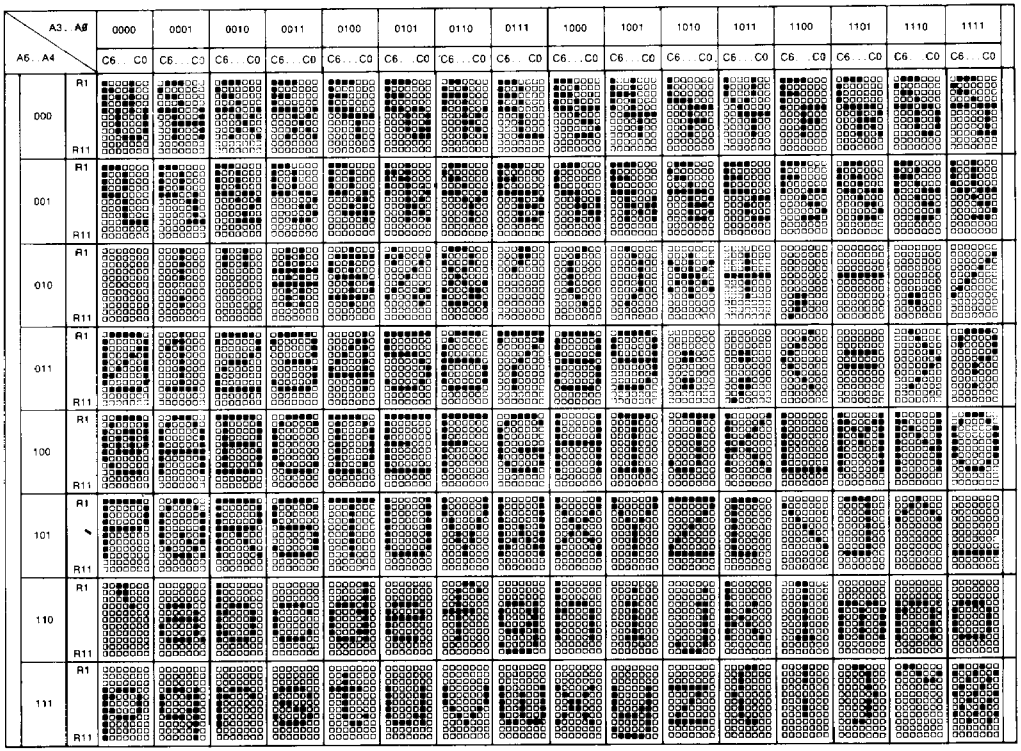
Note: If Character is Blinking at Character Rate, Cursor will change it to Cursor Blink Rate.

FIGURE 5
ROM CHARACTER BLOCK FORMAT

											ROWS	R3	R2	R1	RØ
(ALL ZEROS) →	0	0	0	0	0	0	0	0	—	—	RØ	0	0	0	0
	0	0	0	0	0	0	0	0	—	—	R1	0	0	0	1
	0	0	0	0	0	0	0	0	—	—	R2	0	0	1	0
	0	0	0	0	0	0	0	0	—	—	R3	0	0	1	1
	0	0	0	0	0	0	0	0	—	—	R4	0	1	0	0
	0	0	0	0	0	0	0	0	—	—	R5	0	1	0	1
77 BITS (7 x 11 ROM)	0	0	0	0	0	0	0	0	—	—	R6	0	1	1	0
	0	0	0	0	0	0	0	0	—	—	R7	0	1	1	1
	0	0	0	0	0	0	0	0	—	—	R8	1	0	0	0
	0	0	0	0	0	0	0	0	—	—	R9	1	0	0	1
	0	0	0	0	0	0	0	0	—	—	RIØ	1	0	1	0
	0	0	0	0	0	0	0	0	—	—	R11	1	0	1	1
	0	0	0	0	0	0	0	0	—	—	R12	1	1	0	0
	0	0	0	0	0	0	0	0	—	—	R13	1	1	0	1
(ALL ZEROS)	0	0	0	0	0	0	0	0	—	—	R14	1	1	1	0
	0	0	0	0	0	0	0	0	—	—	R15	1	1	1	1
	*C7	C6	C5	C4	C3	C2	C1	CØ	—	—					

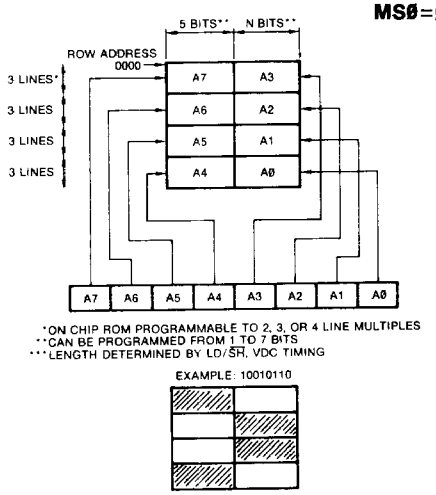
EXTENDED ZEROS (BACK FILL) FOR INTERCHARACTER SPACING (NUMBER CONTROLLED BY LD/SH, VDC TIMING)

*COLUMN 7 IS ALL ZEROS (REVID = 0)
COLUMN 7 IS SHIFTED OUT FIRST



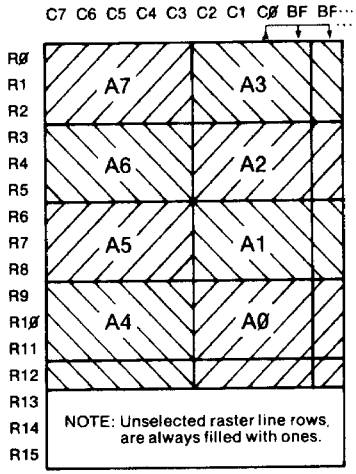
CONSULT FACTORY FOR CUSTOM FONT AND OPTION PROGRAMMING FORMS.

FIGURE 1
WIDE GRAPHICS MODE
MSØ=Ø MS1=Ø



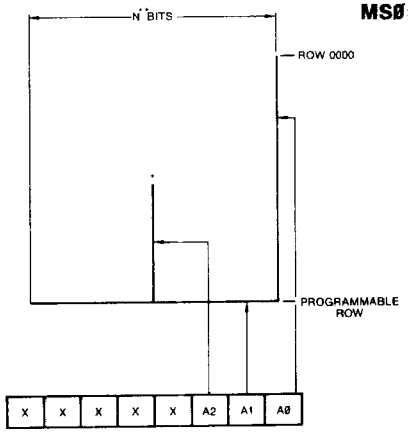
*ON CHIP ROM PROGRAMMABLE TO 2, 3, OR 4 LINE MULTIPLES
**CAN BE PROGRAMMED FROM 1 TO 7 BITS
***LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING

EXAMPLE: 10010110

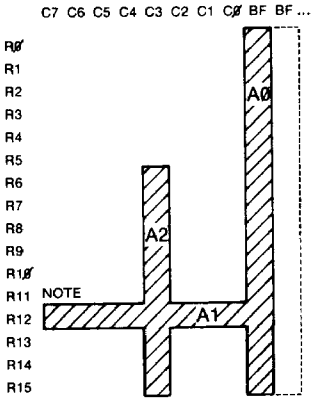


BF = back fill

FIGURE 2
THIN GRAPHICS MODE
MSØ=Ø MS1=1



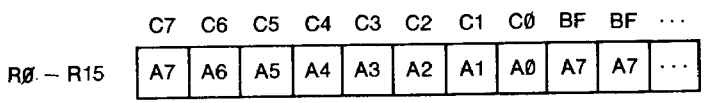
X = DON'T CARE
* THE INSIDE SEGMENT IS MASK PROGRAMMABLE TO ROW 0000
** LENGTH DETERMINED BY LD/$\overline{SR}$, VDC TIMING



NOTE: When A1 = "1", the underline row/rows are deleted.
When A1 = "0", the underline, if selected, will appear.

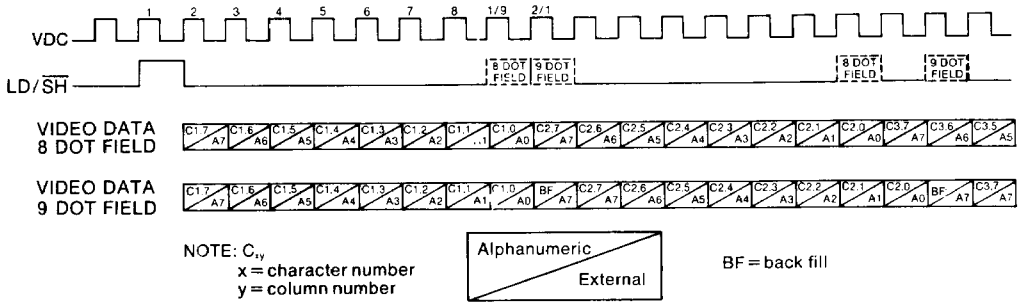
BF = back fill

FIGURE 3
EXTERNAL MODE
MSØ=1 MS1=Ø



BF = back fill

FIGURE 4 TYPICAL VIDEO OUTPUT



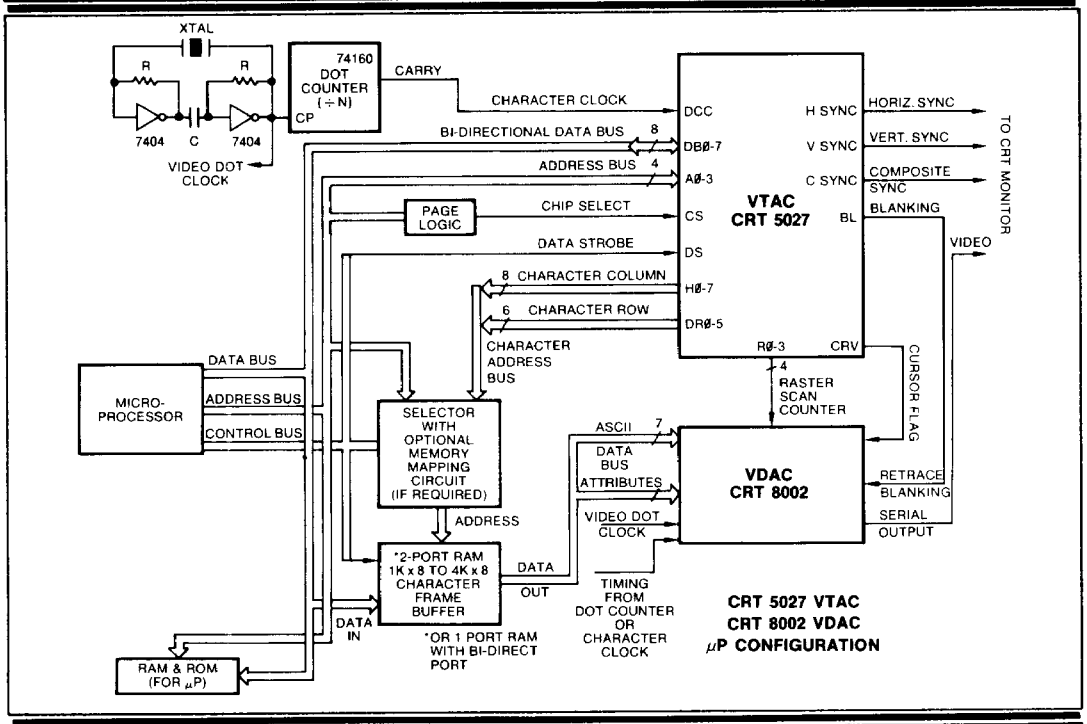
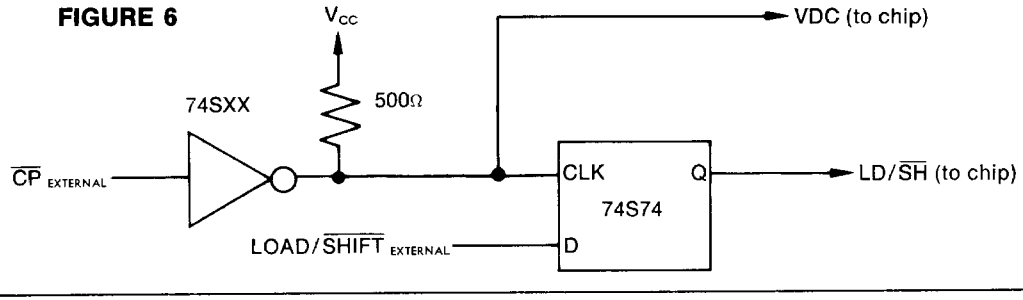
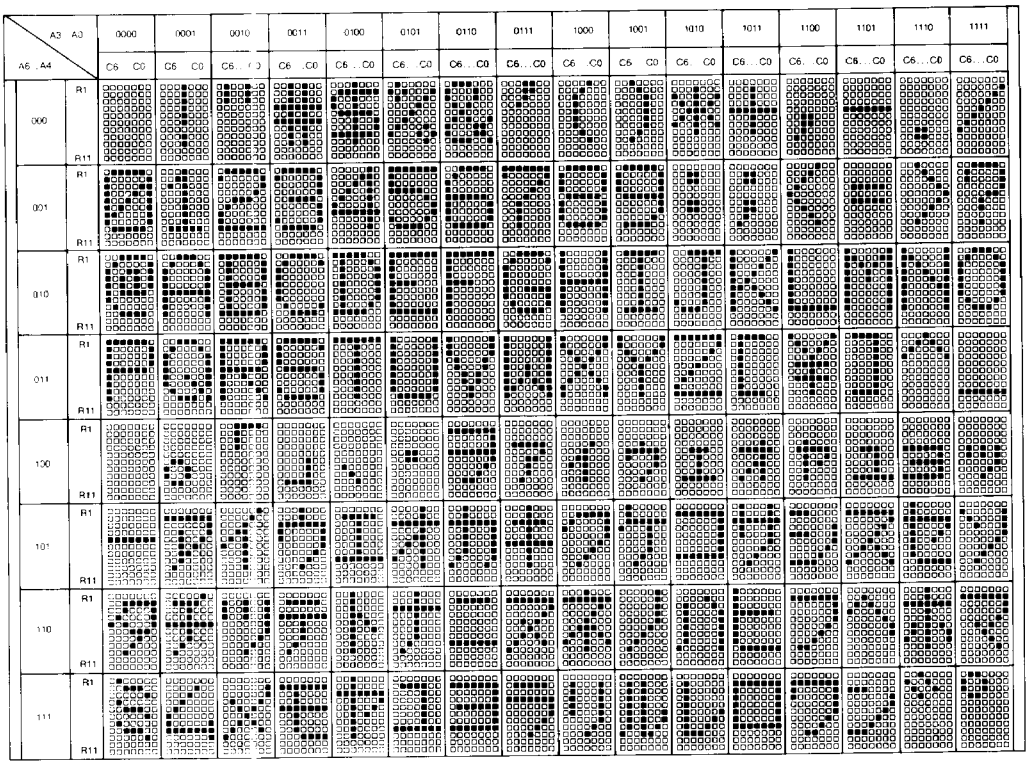


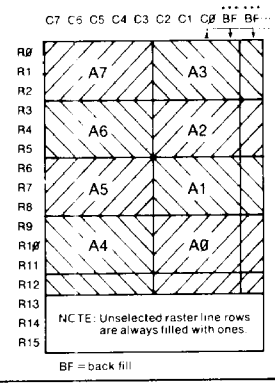
FIGURE 6



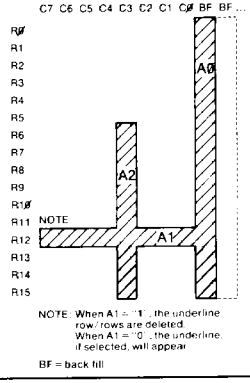
CRT Video Display-Controller Video Generator VDAC™



WIDE GRAPHICS MODE



THIN GRAPHICS MODE



ATTRIBUTES

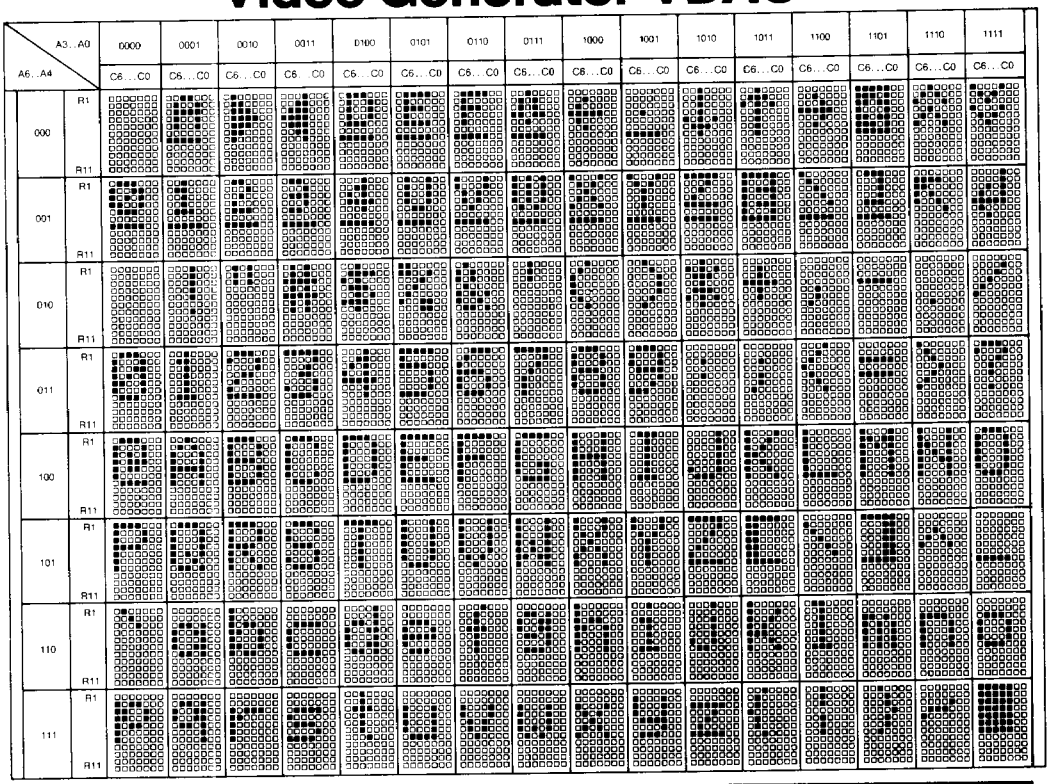
Underline
Underline will be a single horizontal line at row R11

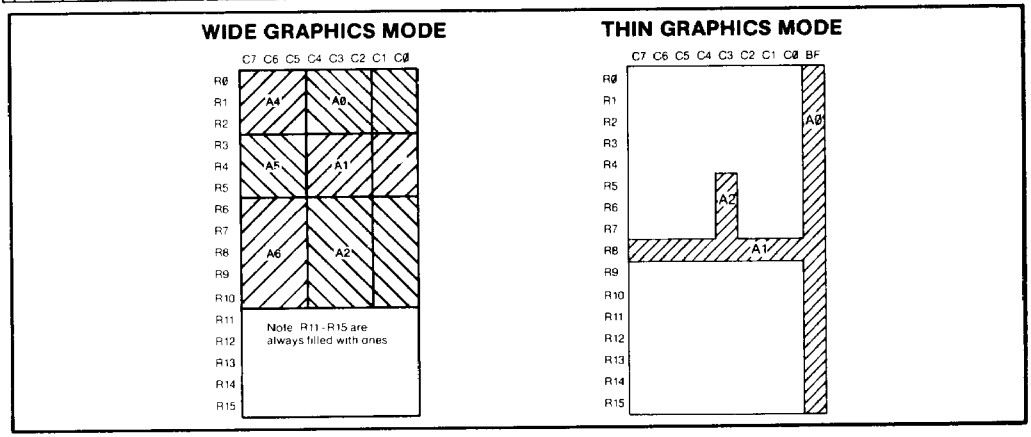
Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate will be 1.875 Hz

Strike-Thru
The strike-thru will be a double line at rows R5 and R6

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

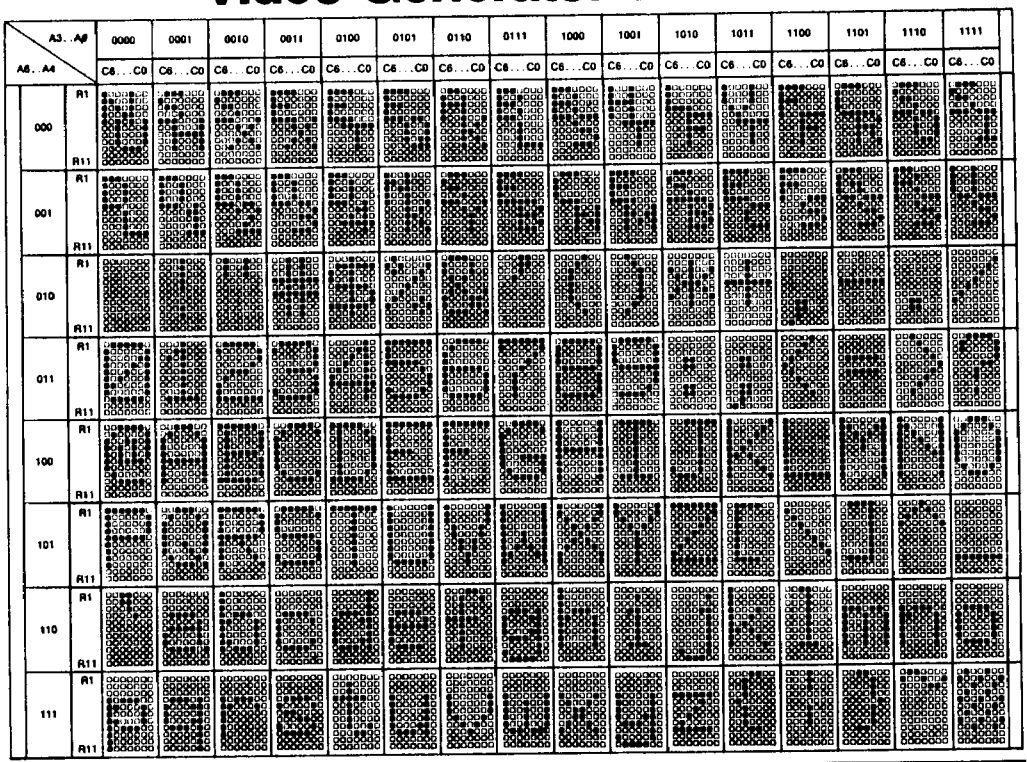
Underline
Underline will be a single horizontal line at R8

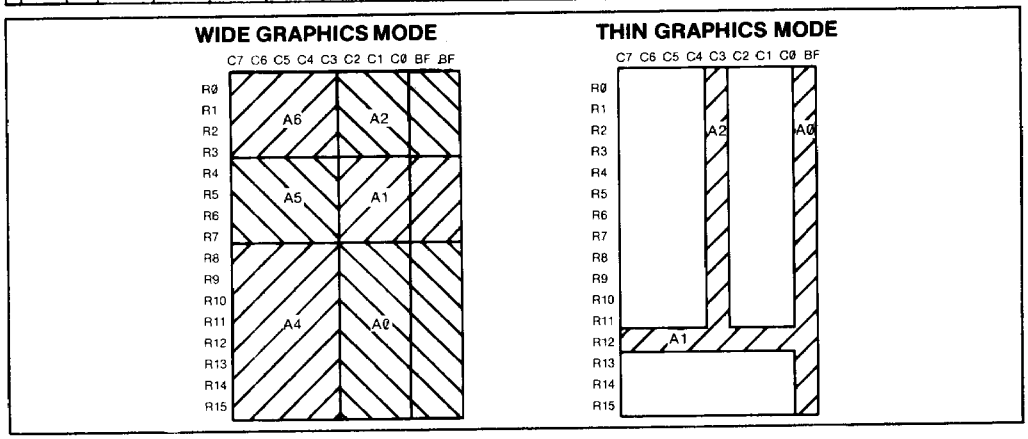
Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a single horizontal line at R4

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a single horizontal line at R12

Cursor
Cursor will be a reverse video block

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a double line at rows R5 and R6

STANDARD MICROSYSTEMS CORPORATION

CRT 8002-011 (ASCII) CODING INFORMATION

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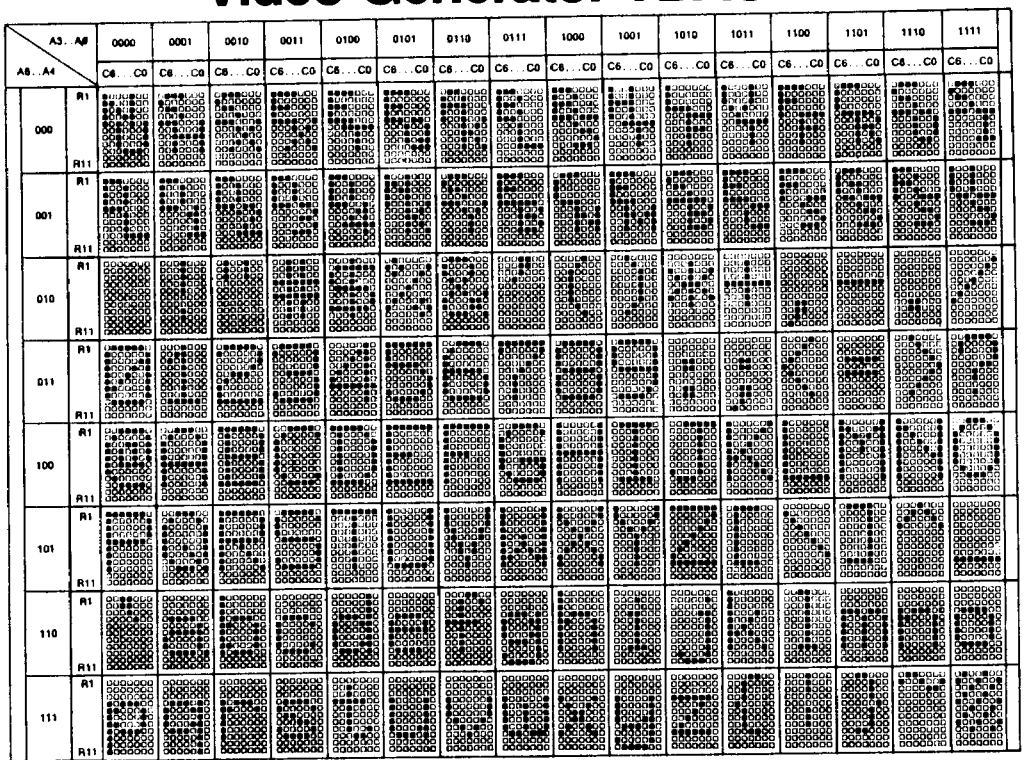
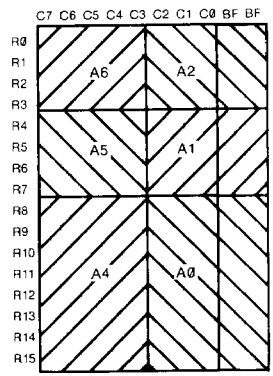
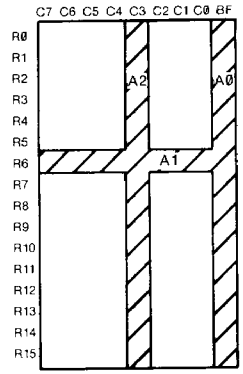


WIDE GRAPHICS MODE



THIN GRAPHICS MODE



ATTRIBUTES

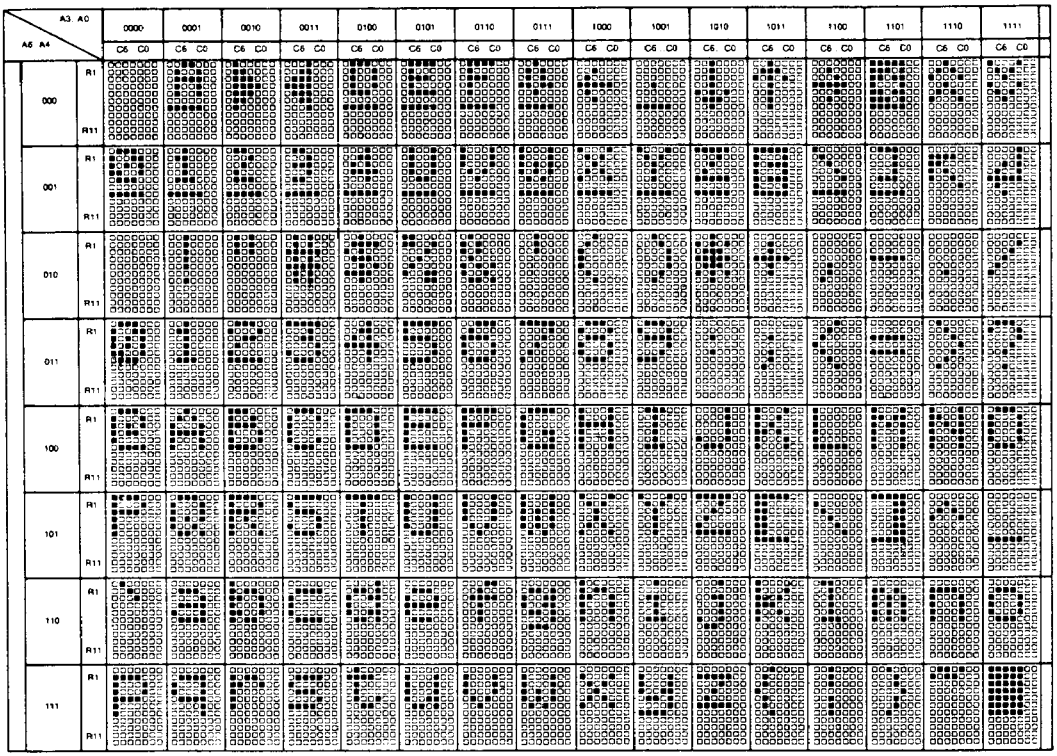
Underline
Underline will be a single horizontal line at R11

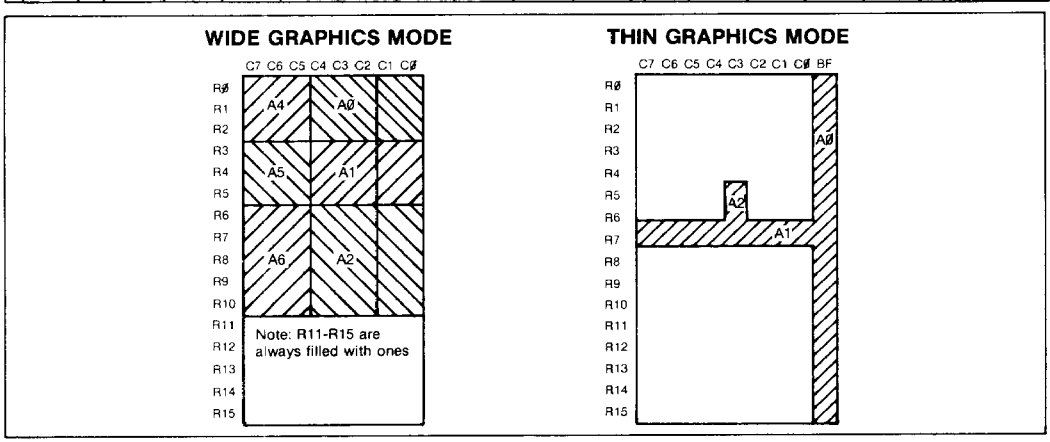
Cursor
Cursor will be a blinking reverse video block, blinking at 3.75 Hz

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a double line at rows R5 and R6

CRT Video Display-Controller Video Generator VDAC™





ATTRIBUTES

Underline
Underline will be a double horizontal line at R7 and R8

Cursor
Cursor will be a reverse video block

Blink Rate
The character blink rate is 1.875 Hz

Strike-Thru
The strike-thru will be a single horizontal line at R4

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