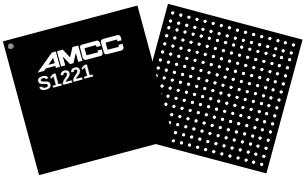


S1221

OC-3/12 SONET/SDH 8-bit Quad Transceiver

Features

- CMOS 0.13 micron technology
- Complies with Bellcore and ITU-T specifications for jitter tolerance, jitter transfer, and jitter generation
- On-chip high-frequency PLLs for clock generation and clock recovery
- Supports Data Rates for 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12)
- 8-bit LVCMOS Parallel data path
- LVDS or LVPECL differential serial interface
- Internal termination of the optic's LVPECL driver renders a seamless power saving connection
- Typical 715 mW power in LVDS I/O mode
- Directly compatible with 2.5 V or 3.3 V LVDS, 3.3 V LVPECL (DC and AC)
- Frame and Byte Boundary Detection option
- 255 PBGA Package,17x17 mm^2 with Green/RoHS compliant lead free option
- 1.2 V and 3.3 V/2.5 V supply
- Receiver lock detect outputs
- Signal detect inputs
- Selectable reference frequencies of 19.44, 77.76 or 155.52 MHz
- Internal FIFO to decouple transmit clocks
- Various diagnostic loopback modes
- Quad configuration, mixed OC-3/OC-12
- Built-In Self Test (BIST) Feature
- Independent power down of unused channels
- Drop-in-replacement for S1213

Applications

- SONET/SDH OC-3/OC-12
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

Description

The S1221 SONET/SDH transceiver is one of the latest additions to the AMCC product family. The S1221 device provides fully integrated serialization/de-serialization capabilities with four independent transceivers. The device performs all necessary parallel-to-serial and serial-to-parallel functions in conformance with the SONET/SDH transmission standards.

Clock and Data Recovery are provided for the standard operating rates of 155.52 Mbps (OC-3) and 622.08 Mbps (OC-12).

The S1221 can also be provisioned to a mix and match OC-3 and OC-12 data streams within the same device.

The S1221 can be configured in MII (Media Independent Interface) mode (MII Mode) or in a Non-MII mode.

The figure below, System Block Diagram, shows a typical network application.

Overview

The S1221 can be used to implement the front end of SONET/SDH equipment which consists primarily of the serial transmit interface and the serial receive interface. The Low Voltage LVDS or LVPECL interfaces guarantee compliance with the bit-error rate requirements of the Telcordia and ITU-T standards.

The S1221 is divided into four Transceiver modules with each possessing a clock recovery unit. Each of the modules can run at OC-3 or OC-12 data rates, independent of the other modules.

The S1221 performs SONET/SDH frame detection.

AMCC Suggested Interface Devices

Congo (S1201)	POS/ATM SONET Mapper
Nile (S1202)	ATM SONET Mapper
Orinoco (S1204)	STS-12/STM-4 DS3/E3/STS-1E SONET/SDH Mapper
Agilent	HFBR-5908E, SFF Module
Finisar	FTRJ1322P1xTR, SFP Module V23818-H18 SFF Module
Sumitomo	SCP6802-GL, SFP Module SCM6005, SFF Module
OCP	TRPN03 & TRPN12, SFP Mod.
JDS Uniphase	CT2-P, SFP Module

The S1221 is divided into four transmitter channels and four receiver channels.

The sequence of operations is as follows for each Channel:

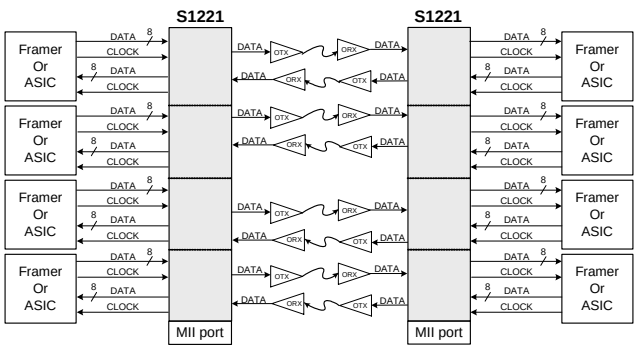
Transmitter Operations

- 8-bit parallel data input
- Parallel-to-serial conversion
- Serial data output

Receiver Operations For One Channel

- Serial data input
- Clock and Data recovery
- Serial-to-parallel data conversion
- 8-bit parallel data and clock output

Internal clocking and control functions are transparent to the user.



System Block Diagram with the S1221

S1221

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