S3160

Data Sheet

2.5 Gbps Wide Bandwidth Transimpedance Amplifier

FEATURES

- Greater than 2 GHz Bandwidth
- 3 kΩ differential transimpedance
- Single 3.3 V supply
- 6.5 pA/√(Hz) typical noise current density
- 2.2 mA peak to peak max input current
- Voltage limited outputs
- Maximum Die size: 1.27 mm by 1.27 mm

APPLICATIONS

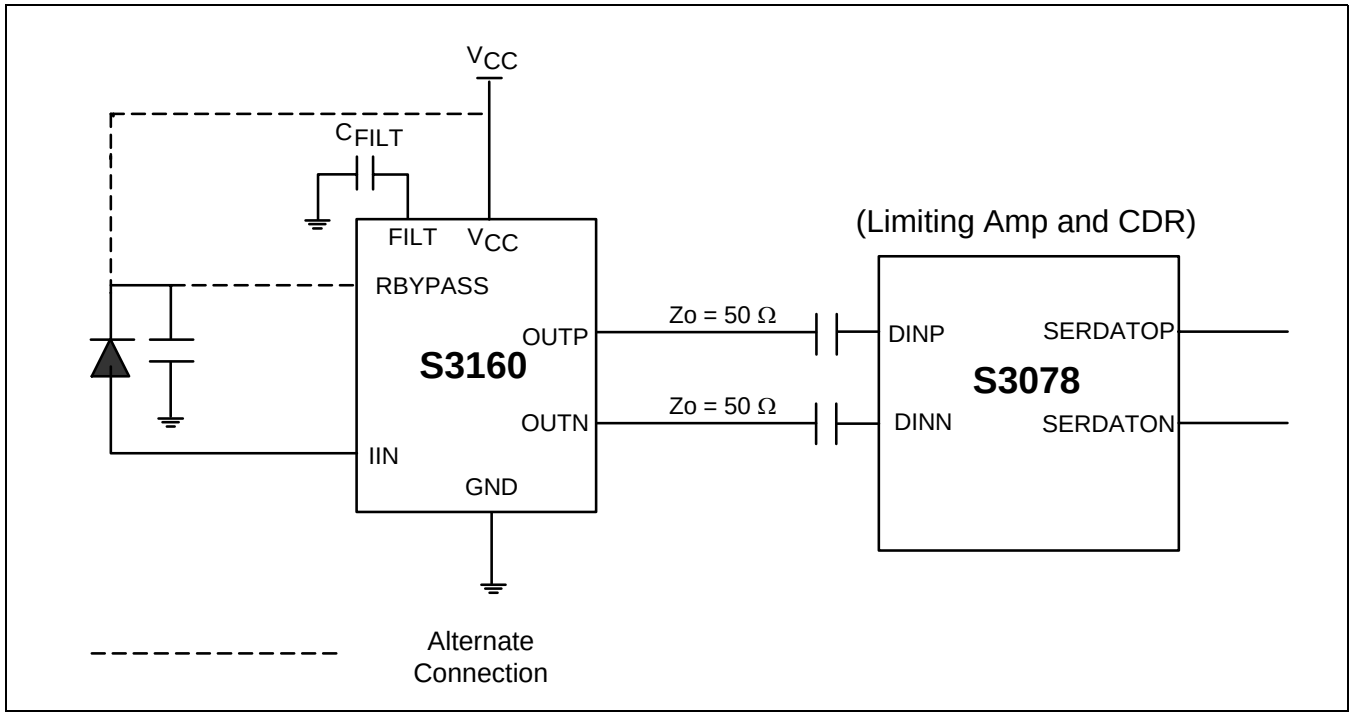
- SONET OC-48
- Fiber optic data links

GENERAL DESCRIPTION

The S3160 is a high-speed transimpedance amplifier (TIA) for 2.5 Gbps applications. Input currents as high as 2.2 mA can be amplified with low duty cycle distortion. The low input noise allows signals down to 4 μA (peak to peak) to be detected with a signal to noise ratio of 22 dB (allows for BER< 1E-10).

The outputs are voltage limited to 1000 mV, differential, in order to allow a wide input dynamic range without exceeding the input voltage range of the post (limiting) amplifier. Figure 1 shows a typical application.

Figure 1. Typical Operating Circuit



DETAILED DESCRIPTION

Figure 2 depicts the overall block diagram of the S3160 transimpedance amplifier. The amplifier circuitry consists of a transimpedance stage and an output driver stage with a 6 dB gain. The transimpedance amplifier converts the photodiode photocurrent to a voltage. The photodiode can be biased by connecting it to the RBYPASS pin or it can be connected directly to V_{CC}.

The amplifier gain is linear for an input of up to 300 μA. Above that the transimpedance of the input stage is reduced by the action of the schottky diode, to prevent overdrive of the output stage. The output of the output stage begins to fully limit when the input current reaches 700 μA. The output voltage is limited at 1000 mV, differential, peak to peak.

The output of the transimpedance stage is converted to a differential signal by the combination of the output stage and a bias block. This bias block averages the output of the transimpedance stage and establishes the DC input reference for the output stage. The bandwidth of this circuit is set by an on-chip capacitor, but can be reduced by adding an off-chip capacitor, C_{FILT}. This bandwidth corresponds to the low frequency -3 dB cutoff of the TIA. Increasing the value of C_{FILT} will reduce the low frequency -3 dB cutoff. With no C_{FILT} capacitor added it will be at 45 kHz.

Figure 2. S3160 Detailed Block Diagram

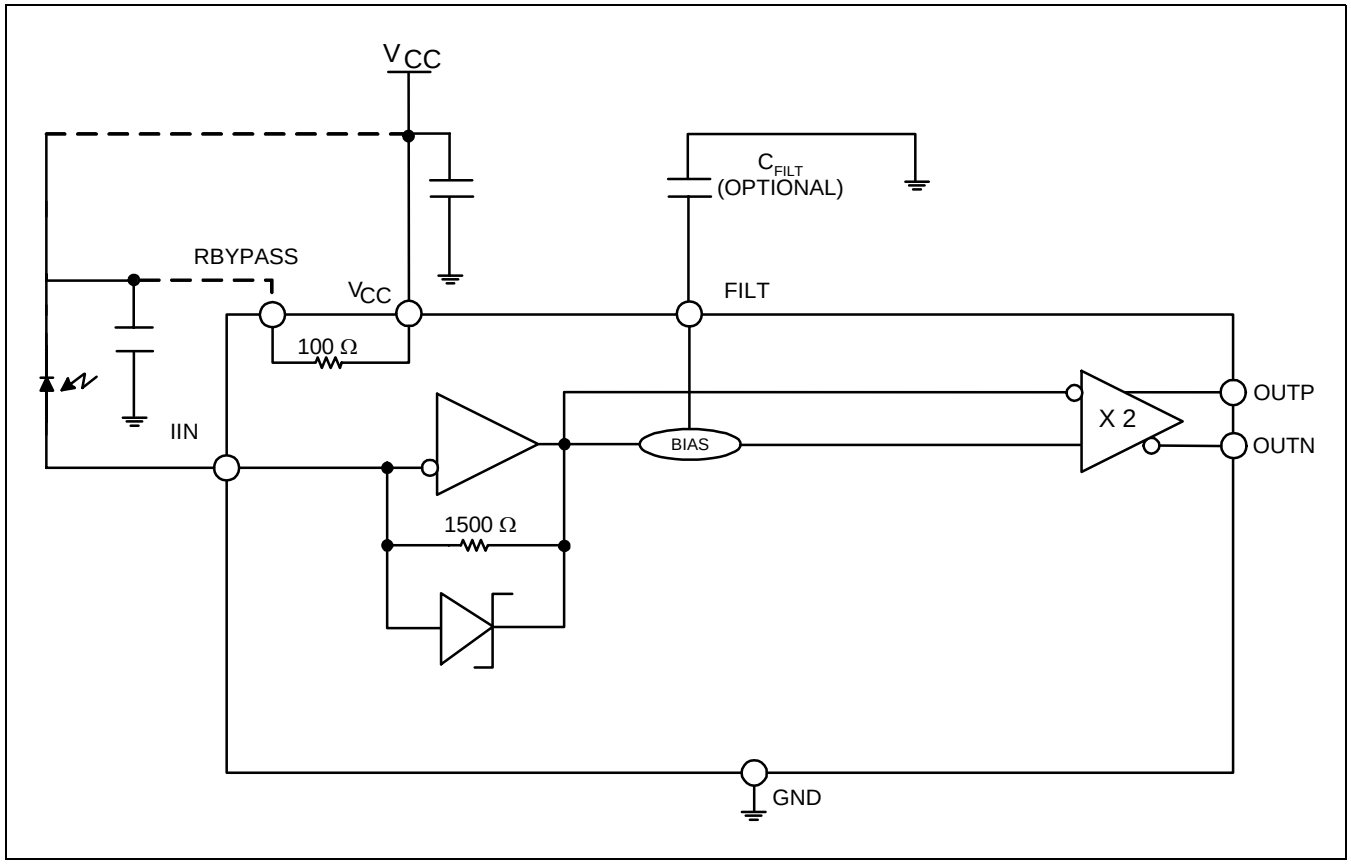
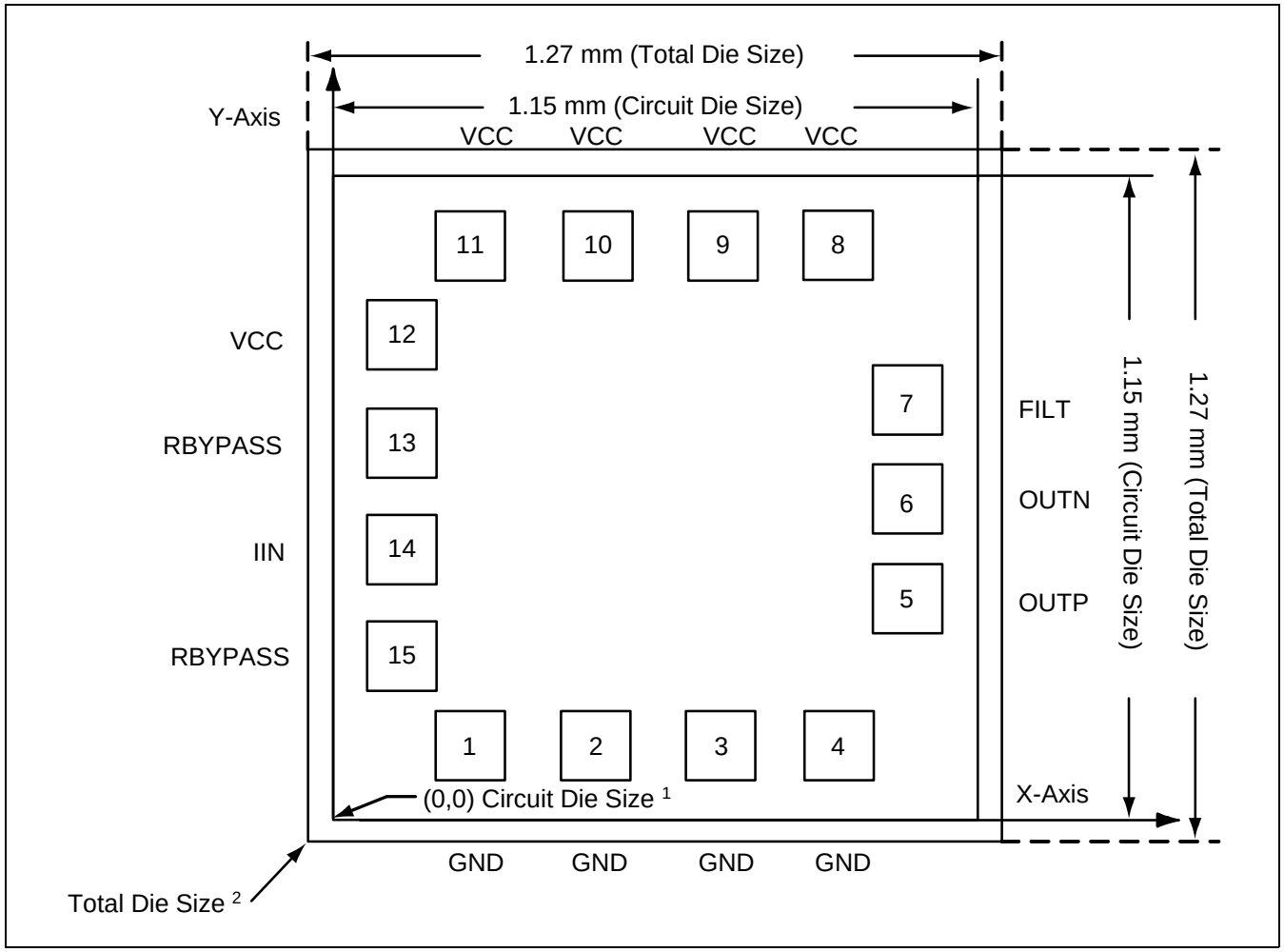


Table 1. S3160 Pad Assignment and Description

Pin Name	I/O	Pad #	Coordinates [X,Y] (1)	Description
VCC	S	8 9 10 11 12	[868.9, 1051.4] [669.6, 1051.4] [470.8, 1051.4] [271.8, 1051.4] [90.8, 892.5]	+3.3 V Power supply.
GND	S	1 2 3 4	[273, 91.4] [472, 91.4] [670.8, 91.4] [870.1, 91.4]	Ground.
RBYPASS	I	13 15	[100.925, 702.425] [90.9, 293.3]	Bypass connection for cathode of photodiode.
IIN	I	14	[97.575, 473.975]	PIN diode input.
FILT	I	7	[1052.3. 777]	Filter capacitor input. A capacitor to ground can be added at this pad to reduce the low frequency -3 dB cutoff. (See Design Procedures).
OUTN	O	6	[1049.275, 567.475]	Negative transimpedance amplifier output.
OUTP	O	5	[1049.275, 375.225]	Positive transimpedance amplifier output.

1. The coordinates represent the position of the center of the pad in µm, with respect to the lower left corner of the circuit die.
2. Note: I = Input pin, O = Output pin, S = Supply pin.

Figure 3. S3160 Bonding Pad Location



Note: Pad Size is 94 μm X 94 μm. The exposed area of the pad is 80 μm X 80 μm.
Die thickness is 254 μm (10 mils).

1. The circuit die size is the smallest possible size of the die. The lower left-hand corner of the circuit die is the origin of the xy-coordinate system. Pad coordinates indicated in Table 1 are measured from this origin to the pad's center.
2. The total die size is the largest possible size of the die. It includes a splicing area around the circuit die. The actual size of any given die may vary in size from the minimum (circuit die) size to the maximum (total die) size.

Table 2. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature, T_A	-40		+85	°C
Junction Operating Temperature, T_J	-20		+105	°C
Voltage on V_{CC} with respect to GND	3.135	3.3	3.465	V

Table 3. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S3160. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other conditions beyond those indicated in the "Recommended Operating Conditions" of this document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units
Voltage on V_{CC} with respect to GND	-0.5		4	V
Voltage on all Other Pads	-0.5		V_{CC} +0.3	V
Storage Temperature Range	-55		150	°C

Electrostatic Discharge (ESD) Sensitivity Rating - Human Body Model (HBM):

The S3160 is rated to the following ESD voltages based upon JEDEC standard: JESD22-A114-B

CLASS 0 - All pins are rated at or above 1000 volts except pins I_{IN}, OUTP and OUTN. OUTP and OUTN are rated at 500 V and I_{IN} is rated to 100 volts.

Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for applicable ESD application notes.

Table 4. AC Electrical Characteristics (Vcc = 3.3 V ± 5%, T_A = -40°C to +85°C)

Parameter	Description	Min	Typ	Max	Units	Conditions
R_T	AC Transimpedance	2.56	2.95	3.34	kV/A	50 Ohm load
BW	-3 dB Bandwidth	2.7	3.2	3.6	GHz	0.5 pF photodiode capacitance, 1.5 nH input bond wire inductance.
BW_{LF}	Low Frequency -3 dB Cutoff		45	57	kHz	No C_{FILT} connected
I_{PK}	Maximum Input Current	2.2			mA	Peak-to-peak
V_{OD}	Maximum Differential output voltage		1000	1200	mV	Peak-to-peak, differential
$I_{IN, CL}$	Input Current before clipping	250	300		μA	1 dB compression point
I_{ND}	Input Noise Current Density		6.5	9.3	pA/√(Hz)	0 - 2.5 GHz
I_N	Input Noise Current		325	465	nA	(Output rms noise)/RT, 2.5 GHz bandwidth
J_T	Total Jitter (Pk to Pk) (At 1E-12 BER)			0.12	UI	Input is 2.488 Gbps, 2^{23}-1 PRBS. I_{IN} = 2.2 mA
RIPPLE	Output Ripple	-0.5		+0.5	dB	1 - 2000 MHz
Group Delay	Group Delay Variation	-25		+25	pS	100 - 2500 MHz
S22	Output Reflection Coeffi-cient			-18	dB	1 - 3500 MHz
R_{OUT}	Output Impedance	45	50	58	Ω	

Table 5. DC Electrical Characteristics (Vcc = 3.3 V ± 5%, T_A = -40°C to +85°C)

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{CC}	Supply Current		40	57	mA	
V_{BIAS}	Input Bias Voltage	0.79	0.92	1.0	V	
V_{CM}	Common Mode Output Voltage	V_{CC} -0.9	V_{CC} -0.65	V_{CC} -0.25	V	50 Ω line termination to GND (AC Coupled) or 100 Ω line-to-line termination.

Note: AC Electrical Characteristics are guaranteed by characterization.

DESIGN PROCEDURES

Determining Capacitor Values

C_{FILT} can be selected using the formula:

Low frequency –3 dB cutoff = 1 / [2π*400kΩ*(10pF + C_{FILT})]

APPLICATION INFORMATION

Filtering Through RBYPASS

To reduce the effect of supply voltage noise at the cathode of the photodiode, the cathode connection to V_{CC} should be made through the RBYPASS resistor. The RBYPASS resistor and an external capacitor to ground at the cathode of the photodiode will act as a filter to reduce this noise and dampen any resonance at the cathode of the photodiode.

Wire Bonding and Layout Information

For best performance all GND pads should be connected and the bond wire inductance between the photodiode and the IIN pin should be kept to below 1.5 nH – 2 nH. The back of the die is not metallized and should be connected to ground or left electrically unconnected.

The outputs OUTP and OUTN should be terminated equally to prevent instabilities. Figures 4 and 5 show the differential and single-ended terminations.

Figure 4. Output Differential Termination

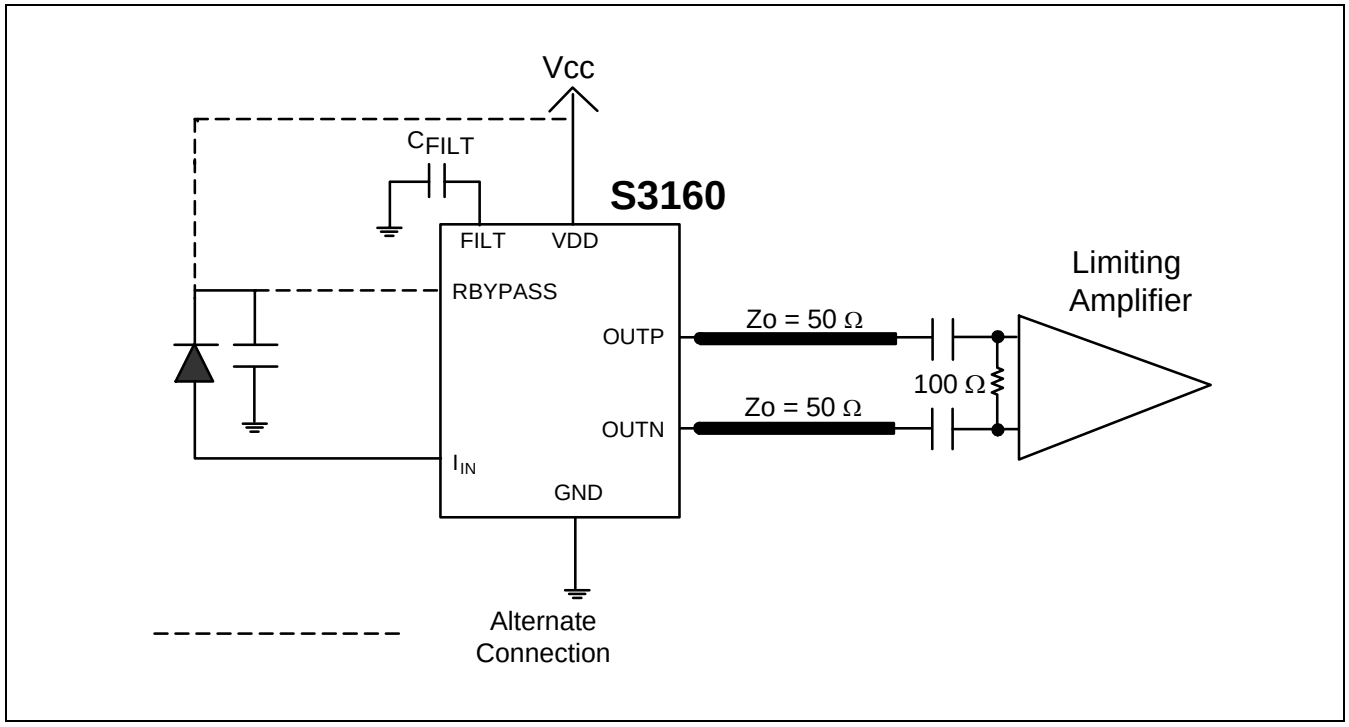
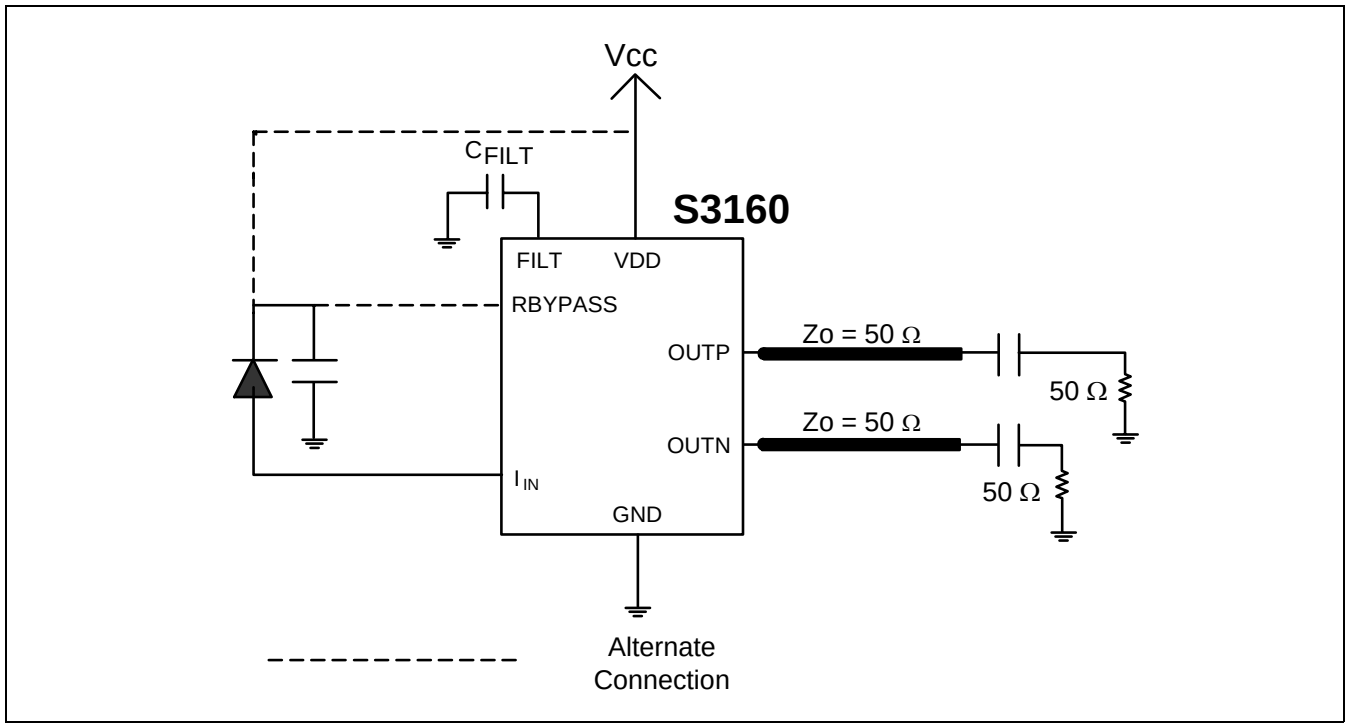


Figure 5. Output Single-Ended Termination



Typical Operating Characteristics

Figure 6. Frequency Response (Gain vs. Frequency)

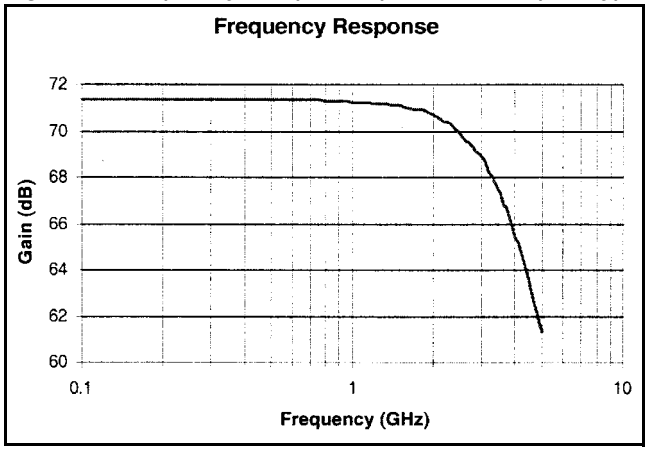


Figure 7. Eye Diagram (at 2.5 Gbps) (I_{IN} = 2.2 mA)

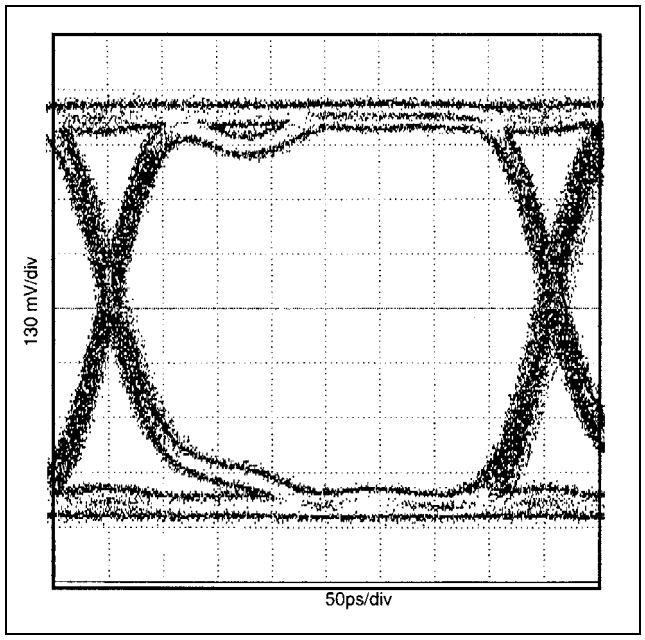


Figure 8. Output Voltage vs. Input Current

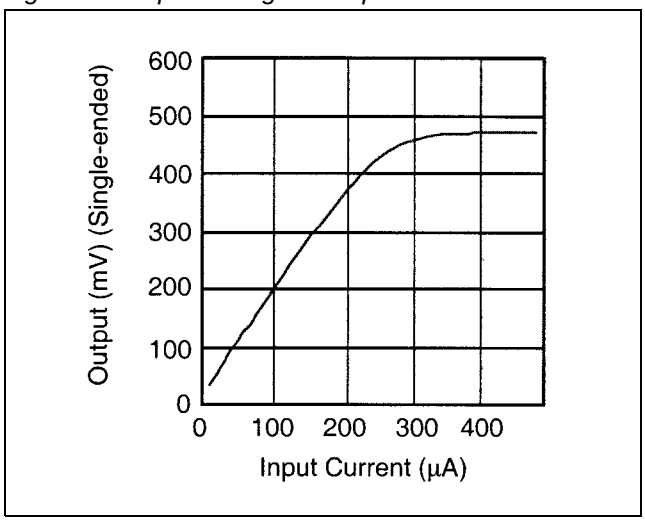
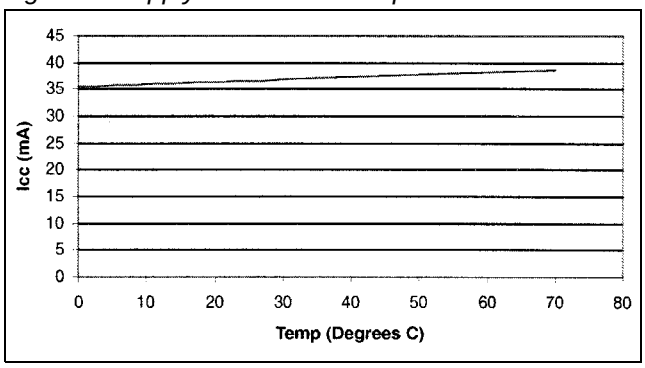


Figure 9. Supply Current vs. Temperature

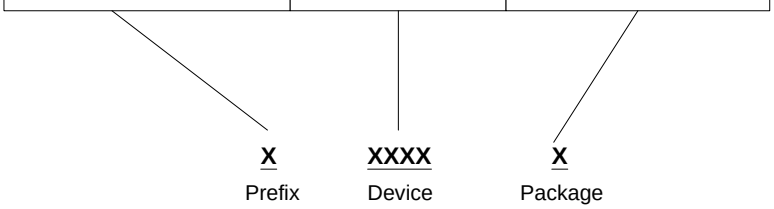


DOCUMENT REVISION HISTORY

Revision	Date	Description
A	08/12/04	• Pg. 6, Table 4, changed S22 Max from -22 dB to -18 dB; changed R_{out} Max from 55 Ω to 58 Ω.
NC	2/28/01	• Production release version.

Ordering Information

Prefix	Device	Package
S–Integrated Circuit	3160	DI–Industrial Grade Die



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