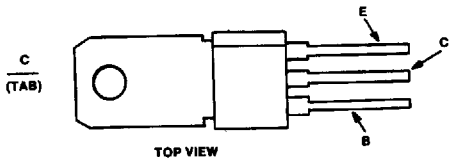
3-Ampere Silicon P-N-P Power Transistors

Complementary to the D42C Series

Features:

- High free-air power dissipation
- Low collector saturation voltage (-0.5V typ. @ -3A I_C)
- Excellent linearity
- Fast switching

TERMINAL DESIGNATIONS



92CS-43473

JEDEC TO-202AB

POWER

The D43C-series of silicon p-n-p power transistors are designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1 MHz; series, shunt and switching regulators; and low and high frequency inverters/converters.

These devices are supplied in the JEDEC TO-202AB plastic package.

MAXIMUM RATINGS (T_A = 25° C) (unless otherwise specified)

RATING	SYMBOL	D43C1, 2, 3	D43C4, 5, 6	D43C7, 8, 9	D43C10, 11, 12	UNITS
Collector-Emitter Voltage	V_{CEO}	-30	-45	-60	-80	Volts
Collector-Emitter Voltage	V_{CES}	-40	-55	-70	-90	Volts
Emitter Base Voltage	V_{EBO}	-5	-5	-5	-5	Volts
Collector Current — Continuous Peak(1)	I_C I_{CM}	-3 -5	-3 -5	-3 -5	-3 -5	A
Base Current — Continuous	I_B	-2	-2	-2	-2	A
Total Power Dissipation @ T_A = 25°C @ T_C = 25°C	P_D	2.1 12.5	2.1 12.5	2.1 12.5	2.1 12.5	Watts
Operating and Storage Junction Temperature Range	T_J,T_{stg}	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	60	60	60	60	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	10	10	10	10	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L	+260	+260	+260	+260	°C

(1) Pulse Test Pulse Width = 300ms Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

T-33-17

CHARACTERISTIC		SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (I_C = -100ma)	D43C1, 2, 3	$V_{CEO(sus)}$	-30	—	—	Volts
	D43C4, 5, 6		-45	—	—	
	D43C7, 8, 9		-60	—	—	
	D43C10, 11, 12		-80	—	—	
Collector Cutoff Current (V_{CE} = Rated V_{CES})		I_{CES}	—	—	-10	μA
Emitter Cutoff Current (V_{EB} = -5V)		I_{EBO}	—	—	-100	uA
SECOND BREAKDOWN						
Second Breakdown with Base Forward Biased		FBSOA	SEE FIGURE 3			
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = -200mA, V_{CE} = -1V)	D43C1, 4, 7, 10	h_{FE}	25	—	—	—
	D43C2, 5, 8, 11		40	—	120	
	D43C3, 6, 9, 12		40	—	120	
(I_C = -1A, V_{CE} = -1V)	D43C1, 4, 7, 10	h_{FE}	10	—	—	—
	D43C2, 5, 8, 11		20	—	—	
(I_C = -2A, V_{CE} = -1V)	D43C3, 6, 9, 12		20	—	—	
Collector-Emitter Saturation Voltage (I_C = -1A, I_B = -50mA)	D43C2, 5, 8, 11	$V_{CE(sat)}$	—	—	-0.5	Volts
	D43C3, 6, 9, 12		—	—	-0.5	
(I_C = -1A, I_B = -100mA)	D43C1, 4, 7, 10	$V_{CE(sat)}$	—	—	-0.5	Volts
Base-Emitter Saturation Voltage (I_C = -1A, I_B = -100mA)		$V_{BE(sat)}$	—	—	-1.3	Volts
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = -10V, f = 1M_{Hz})		C_{CBO}	—	—	125	pF
Current-Gain — Bandwidth Product (I_C = -20mA, V_{CE} = -4V)		f_T	—	40	—	MHz
SWITCHING CHARACTERISTICS						
Resistive Load						
Delay Time + Rise Time	I_C = -1A, I_{B1} = I_{B2} = -0.1A	$t_d + t_r$	—	50	—	nS
Storage Time	V_{CC} = 30V, t_p = 25 μsec	t_s	—	500	—	
Fall Time		t_f	—	50	—	

(1) Pulse Test PW = 300ms Duty Cycle ≤ 2%.

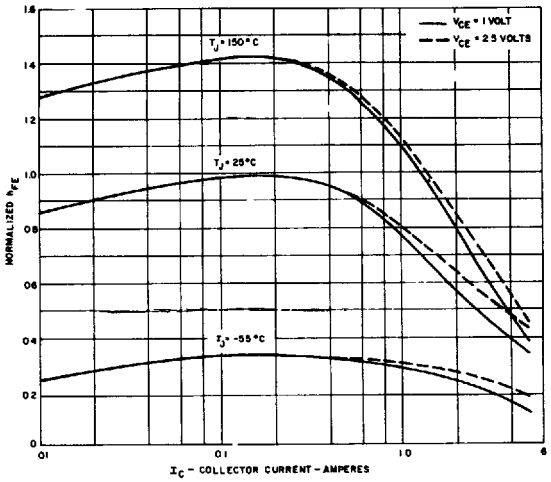


FIG. 1 TYPICAL NORMALIZED h_{FE} VS. I_C

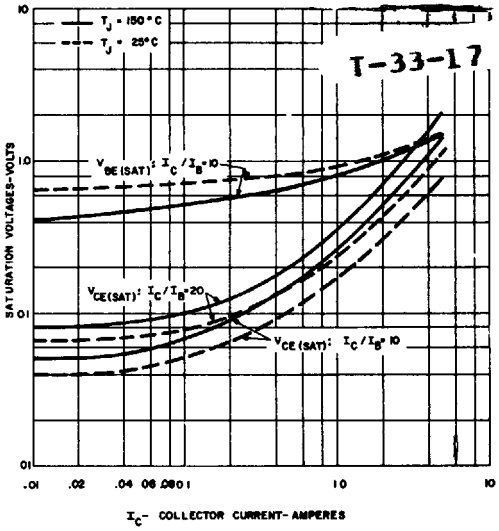


FIG. 2 TYPICAL SATURATION VOLTAGE CHARACTERISTICS

HARRIS SEMICOND SECTOR

POWER TRANSISTORS

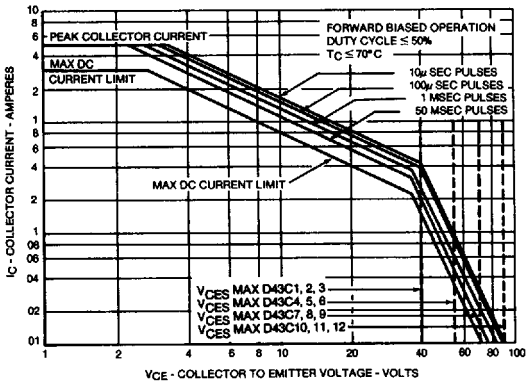


FIG. 3 SAFE REGION OF OPERATION

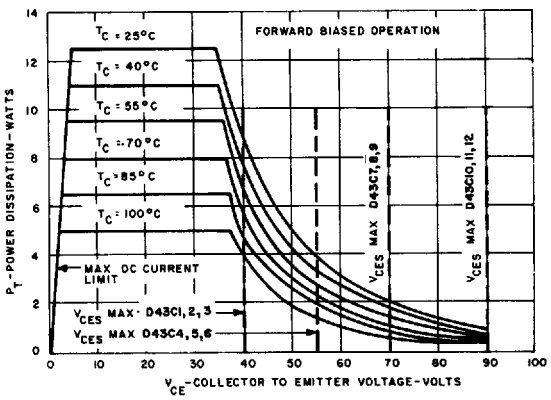


FIG. 4 MAXIMUM PERMISSIBLE DC POWER DISSIPATION

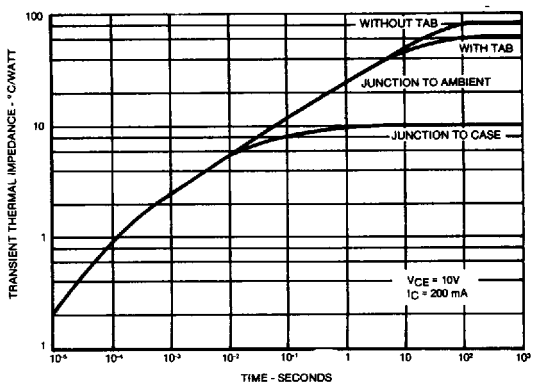


FIG. 5 MAXIMUM TRANSIENT THERMAL IMPEDANCE