EN29F800
8 Megabit (1024K x 8-bit / 512K x 16-bit) Flash Memory Boot Sector Flash Memory, CMOS 5.0 Volt-only

FEATURES

- 5.0V ± 10%, single power supply operation
  - Minimizes system level power requirements
- Manufactured on 0.32 µm process technology
- High performance
  - Access times as fast as 45 ns
- Low power consumption
  - 25 mA typical active read current
  - 30 mA typical program/erase current
  - 1 µA typical standby current (standard access time to active mode)
- Flexible Sector Architecture:
  - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and fifteen 64 Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16 Kword and fifteen 32 Kword sectors (word mode)
  - Supports full chip erase
  - Individual sector erase supported
  - Sector protection:
    Hardware locking of sectors to prevent program or erase operations within individual sectors
    Additionally, temporary Sector Group Unprotect allows code changes in previously locked sectors.
- High performance program/erase speed
  - Byte program time: 10µs typical
  - Sector erase time: 500ms typical
  - Chip erase time: 3.5s typical
- Low Standby Current
  - 1µA CMOS standby current-typical
  - 1mA TTL standby current
- Low Power Active Current
  - 30mA active read current
  - 30mA program/erase current
- JEDEC Standard program and erase commands
- JEDEC standard $\overline{\text{DATA}}$ polling and toggle bits feature
- Single Sector and Chip Erase
- Sector Unprotect Mode
- Embedded Erase and Program Algorithms
- Erase Suspend / Resume modes:
  Read and program another Sector during Erase Suspend Mode
- 0.32 µm double-metal double-poly triple-well CMOS Flash Technology
- Low Vcc write inhibit ≤ 3.2V
- >100K program/erase endurance cycle
- 48-pin TSOP (Type 1)
- Commercial Temperature Range

GENERAL DESCRIPTION

The EN29F800 is a 8-Megabit, electrically erasable, read/write non-volatile flash memory, organized as 1,048,576 bytes or 524,288 words. Any byte can be programmed typically in 10µs. The EN29F800 features 5.0V voltage read and write operation, with access times as fast as 45ns to eliminate the need for WAIT states in high-performance microprocessor systems.

The EN29F800 has separate Output Enable ($\overline{\text{OE}}$), Chip Enable ($\overline{\text{CE}}$), and Write Enable ($\overline{\text{WE}}$) controls, which eliminate bus contention issues. This device is designed to allow either single (or multiple) Sector or full chip erase operation, where each Sector can be individually protected against program/erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 100K program/erase cycles on each Sector.

CONNECTION DIAGRAMS

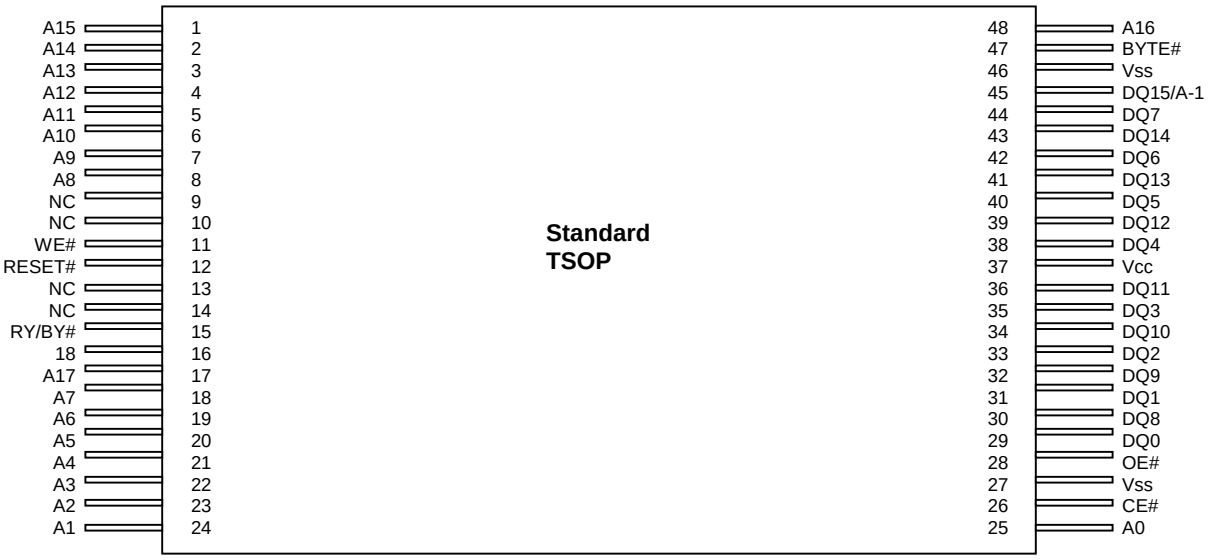


TABLE 1. PIN DESCRIPTION

Pin Name	Function
A0-A19	Addresses
DQ0-DQ14	15 Data Inputs/Outputs
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{Reset}$	Hardware Reset Pin
$\overline{RY/BY}$	Ready/Busy Output
$\overline{WE}$	Write Enable
Vcc	Supply Voltage (5V ± 10%)
Vss	Ground
NC	Internally connected pin

FIGURE 1. LOGIC DIAGRAM

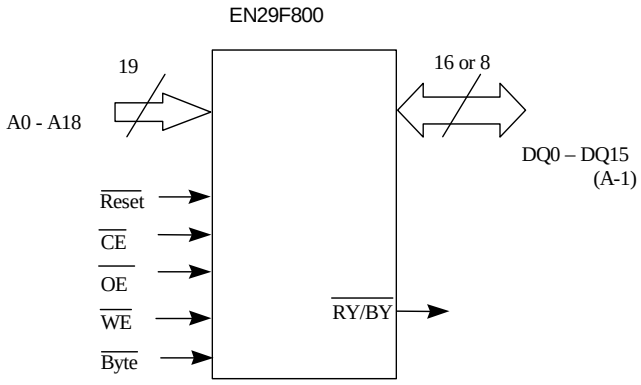


TABLE 2A. TOP BOOT BLOCK SECTOR ARCHITECTURE

Sector	ADDRESS RANGE		SECTOR SIZE (Kbytes / Kwords)	A18	A17	A16	A15	A14	A13	A12
	(X16)	(X8)								
18	7E000h-7FFFFh	FC000h-FFFFFh	16/8	1	1	1	1	1	1	X
17	7D000h-7DFFFh	FA000h-FBFFFh	8/4	1	1	1	1	1	0	1
16	7C000h-7CFFFh	F8000h-F9FFFh	8/4	1	1	1	1	1	0	0
15	78000h-7BFFFh	F0000h – F7FFFh	32/16	1	1	1	1	0	X	X
14	70000h-77FFFh	E0000h - EFFFFh	64/32	1	1	1	0	X	X	X
13	68000h-6FFFFh	D0000h - DFFFFh	64/32	1	1	0	1	X	X	X
12	60000h-6FFFFh	C0000h - CFFFFh	64/32	1	1	0	0	X	X	X
11	58000h-5FFFFh	B0000h - BFFFFh	64/32	1	0	1	1	X	X	X
10	50000h-57FFFh	A0000h - AFFFFh	64/32	1	0	1	0	X	X	X
9	48000h-4FFFFh	90000h - 9FFFFh	64/32	1	0	0	1	X	X	X
8	40000h-47FFFh	80000h - 8FFFFh	64/32	1	0	0	0	X	X	X
7	38000h-3FFFFh	70000h - 7FFFFh	64/32	0	1	1	1	X	X	X
6	30000h-37FFFh	60000h - 6FFFFh	64/32	0	1	1	0	X	X	X
5	28000h-2FFFFh	50000h – 5FFFFh	64/32	0	1	0	1	X	X	X
4	20000h-27FFFh	40000h – 4FFFFh	64/32	0	1	0	0	X	X	X
3	18000h-1FFFFh	30000h – 3FFFFh	64/32	0	0	1	1	X	X	X
2	10000h-17FFFh	20000h - 2FFFFh	64/32	0	0	1	0	X	X	X
1	08000h-0FFFFh	10000h - 1FFFFh	64/32	0	0	0	1	X	X	X
0	00000h-07FFFh	00000h - 0FFFFh	64/32	0	0	0	0	X	X	X

TABLE 2B. BOTTOM BOOT BLOCK SECTOR ARCHITECTURE

Sector	ADDRESS RANGE		SECTOR SIZE (Kbytes/ Kwords)	A18	A17	A16	A15	A14	A13	A12
	(X16)	(X8)								
18	78000h-7FFFFh	F0000h – FFFFFh	64/32	1	1	1	1	X	X	X
17	70000h-77FFFh	E0000h – EFFFFh	64/32	1	1	1	0	X	X	X
16	68000h-6FFFFh	D0000h – DFFFFh	64/32	1	1	0	1	X	X	X
15	60000h-67FFFh	C0000h – CFFFFh	64/32	1	1	0	0	X	X	X
14	58000h-5FFFFh	B0000h - BFFFFh	64/32	1	0	1	1	X	X	X
13	50000h-57FFFh	A0000h - AFFFFh	64/32	1	0	1	0	X	X	X
12	48000h-4FFFFh	90000h – 9FFFFh	64/32	1	0	0	1	X	X	X
11	40000h-47FFFh	80000h – 8FFFFh	64/32	1	0	0	0	X	X	X
10	38000h-3FFFFh	70000h –7FFFFh	64/32	0	1	1	1	X	X	X
9	30000h-37FFFh	60000h – 6FFFFh	64/32	0	1	1	0	X	X	X
8	28000h-2FFFFh	50000h – 5FFFFh	64/32	0	1	0	1	X	X	X
7	20000h-27FFFh	40000h – 4FFFFh	64/32	0	1	0	0	X	X	X
6	18000h-1FFFFh	30000h – 3FFFFh	64/32	0	0	1	1	X	X	X
5	10000h-17FFFh	20000h – 2FFFFh	64/32	0	0	1	0	X	X	X
4	08000h-0FFFFh	10000h – 1FFFFh	64/32	0	0	0	1	X	X	X
3	04000h-07FFFh	08000h – 0FFFFh	32/16	0	0	0	0	1	X	X
2	03000h-03FFFh	06000h – 07FFFh	8/4	0	0	0	0	0	1	1
1	02000h-02FFFh	04000h – 05FFFh	8/4	0	0	0	0	0	1	0
0	00000h-01FFFh	00000h – 01FFFh	16/8	0	0	0	0	0	0	X

PRODUCT SELECTOR GUIDE

Product Number		EN29F800			
Speed Option	Vcc=5.0V ± 10%	**-45**	**-55**	**-70**	**-90**
Max Access Time, ns (t_{acc})		45	55	70	90
Max CE# Access, ns (t_{ce})		45	55	70	90
Max OE# Access, ns (t_{oe})		25	30	30	35

BLOCK DIAGRAM

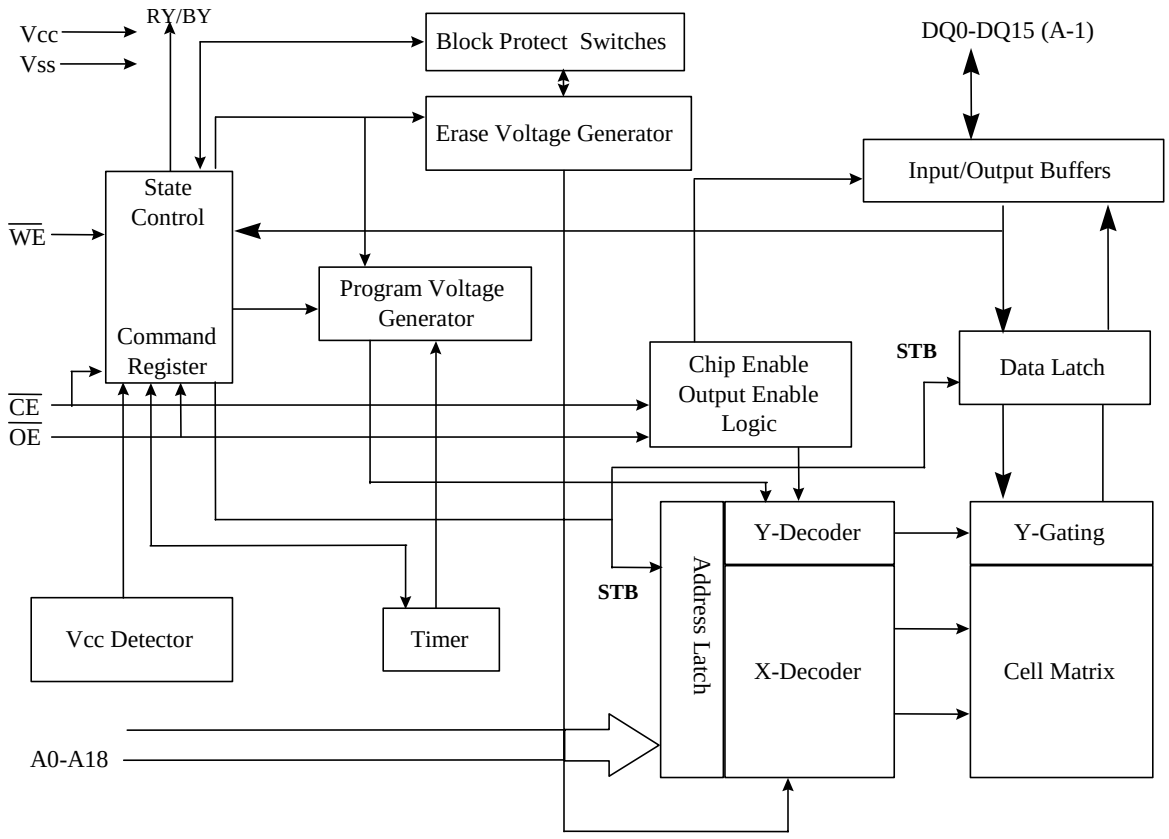


TABLE 3. OPERATING MODES

8M FLASH USER MODE TABLE

Operation	CE#	OE#	WE #	Reset#	A0-A18	DQ0-DQ7	DQ8-DQ15	
							Byte# = V_{IH}	Byte# = V_{IL}
Read	L	L	H	H	A_{IN}	D_{OUT}	D_{OUT}	High-Z
Write	L	H	L	H	A_{IN}	D_{IN}	D_{IN}	High-Z
CMOS Standby	V_{cc} ± 0.5V	X	X	V_{cc} ± 0.5V	X	High-Z	High-Z	High-Z
TTL Standby	H	X	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	High-Z	High-Z	High-Z
Hardware Reset	X	X	X	L	X	High-Z	High-Z	High-Z
Temporary Sector Unprotect	X	X	X	V_{ID}	A_{IN}	D_{IN}	D_{IN}	X

Notes:
L=logic low= V_{IL}, H=Logic High= V_{IH}, V_{ID} =11.0 ± 0.5V, X=Don't Care, D_{IN}=Data In, D_{OUT}=Data Out, A_{IN}=Address In

TABLE 4. DEVICE IDENTIFICTION

8M FLASH MANUFACTURER/DEVICE ID TABLE

Description	Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A18 to A12	A11 to A10	A9	A8	A7	A6	A5 to A2	A1	A0	DQ8 to DQ15	DQ7 to DQ0
Manufacturer ID: EON		L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	L	X	1Ch
Device ID (top boot block)	Word	L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	H	22h	89h
	Byte	L	L	H										X	89h
Device ID (bottom boot block)	Word	L	L	H	X	X	V_{ID}	H[1]	X	L	X	L	H	22h	8Ah
	Byte	L	L	H										X	8Ah
Sector Protection Verification		L	L	H	SA	X	V_{ID}	H[1]	X	L	X	H	L	X	01h (Unprotected)
														X	00h (Protected)

Note:
1. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh. A further Manufacturing ID must be read with A8=H.
2. If a device ID is read with A8=L, the chip will output configuration code 7Fh. A further Device ID must be read with A8=H.

USER MODE DEFINITIONS

Word / Byte Configuration

The signal set on the BYTE# Pin controls whether the device data I/O pins DQ15-DQ0 operate in the byte or word configuration. When the Byte# Pin is set at logic '1', then the device is in word configuration, DQ15-DQ0 are active and are controlled by CE# and OE#.

On the other hand, if the Byte# Pin is set at logic '0', then the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

Standby Mode

The EN29F800 has a CMOS-compatible standby mode, which reduces the current to < 1µA (typical). It is placed in CMOS-compatible standby when the $\overline{CE}$ pin is at $V_{CC} \pm 0.5$. RESET# and BYTE# pin must also be at CMOS input levels. The device also has a TTL-compatible standby mode, which reduces the maximum V_{CC} current to < 1mA. It is placed in TTL-compatible standby when the $\overline{CE}$ pin is at V_{IH}. When in standby modes, the outputs are in a high-impedance state independent of the $\overline{OE}$ input.

Read Mode

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See "Erase Suspend/Erase Resume Commands" for more additional information.

The system must issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See the "Reset Command" additional details.

Output Disable Mode

When the $\overline{CE}$ or $\overline{OE}$ pin is at a logic high level (V_{IH}), the output from the EN29F800 is disabled. The output pins are placed in a high impedance state.

Auto Select Identification Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ15–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (10.5 V to 11.5 V) on address pin A9. Address pins A6, A1, and A0 must be as shown in Autoselect Codes (High Voltage Method) table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Refer to the corresponding Sector Address Tables. The Command Definitions table shows the remaining address bits that are don't-care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15–DQ0.

To access the autoselect codes in-system; the host system can issue the autoselect command via the command register, as shown in the Command Definitions table. This method does not require V_{ID}. See “Command Definitions” for details on using the autoselect mode.

Write Mode

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. The Command Definitions in Table 5 show the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. See “Write Operation Status” for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a “0” back to a “1”.** Attempting to do so may halt the operation and set DQ5 to “1”, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still “0”. Only erase operations can convert a “0” to a “1”.

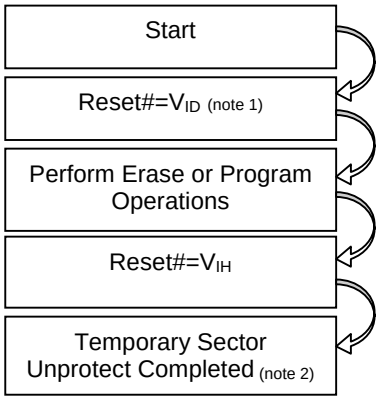
Sector Protection/Unprotection

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors.

Sector protection/unprotection must be implemented using programming equipment. The procedure requires a high voltage (V_{ID}) on address pin A9 and the control pins. Details on this method are provided in a supplement, which can be obtained by contacting a representative of Eon Silicon Devices, Inc.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sector groups to change data while in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sector groups can be programmed or erased by simply selecting the sectgor addresses. Once is removed from the RESET# pin, all the previously protected sector are protected again. See accompanying figure and timing diagrams for more details.



Notes:
1. All protected sectors unprotected.
2. Previously protected sectors protected again.

Hardware Data protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes as seen in the Command Definitions table. Additionally, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by false system level signals during Vcc power up and power down transitions, or from system noise.

Low V_{CC} Write Inhibit

When Vcc is less than V_{LKO}, the device does not accept any write cycles. This protects data during Vcc power up and power down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until Vcc is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when Vcc is greater than V_{LKO}.

Write Pulse "Glitch" protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of $\overline{CE}$ = V_{IH}, or $\overline{WE}$ = V_{IH}. To initiate a write cycle, $\overline{CE}$ and $\overline{WE}$ must be a logical zero. If $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ are all logical zero (not recommended usage), it will be considered a write.

Power-up Write Inhibit

During power-up, the device automatically resets to READ mode and locks out write cycles. Even with $\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the device will not accept commands on the rising edge of $\overline{WE}$.

COMMAND DEFINITIONS

The operations of the EN29F800 are selected by one or more commands written into the command register to perform Read/Reset Memory, Read ID, Read Sector Protection, Program, Sector Erase, Chip Erase, Erase Suspend and Erase Resume. Commands are made up of data sequences written at specific addresses via the command register. The sequences for the specified operation are defined in the Command Definitions table (Table 5). Incorrect addresses, incorrect data values or improper sequences will reset the device to Read Mode.

Table 5. EN29F800 Command Definitions

Command Sequence			Cycles	Bus Cycles											
				1st Write Cycle		2nd Write Cycle		3rd Write Cycle		4th Write Cycle		5th Write Cycle		6th Write Cycle	
				Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read			1	RA	RD										
Reset			1	xxx	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	000/100	7F/1C				
		Byte		AAA		555		AAA							
	Device ID Top Boot	Word	4	555	AA	2AA	55	555	90	001/101	7F/2289				
		Byte		AAA		555		AAA		002/102	7F/89				
	Device ID Bottom Boot	Word	4	555	AA	2AA	55	555	90	001/101	7F/228A				
		Byte		AAA		555		AAA		002/102	7F/8A				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA)X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA)X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend			1	xxx	B0										
Erase Resume			1	xxx	30										

Address and Data values indicated in hex
RA = Read Address: address of the memory location to be read. This is a read cycle.
RD = Read Data: data read from location RA during Read operation. This is a read cycle.
PA = Program Address: address of the memory location to be programmed. X = Don't-Care.
PD = Program Data: data to be programmed at location PA
SA = Sector Address: address of the Sector to be erased or verified. Address bits A18-A12 uniquely select any Sector.

Reading Array Data

The device is automatically set to reading array data after power up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

Following an Erase Suspend command, Erase Suspend mode is entered. The system can read array data using the standard read timings, with the only difference in that if it reads at an address within erase suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception.

The Reset command must be issued to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See next section for details on Reset.

Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't-care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete. The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. The Command Definitions table shows the address and data requirements. This is an alternative method which is intended for PROM programmers and requires V_{ID} on address bit A9.

Two unlock cycles followed by the autoselect command initiate the autoselect command sequence. Autoselect mode is then entered and the system may read at any address any number of times, without needing another command sequence.

The system must write the reset command to exit the autoselect mode and return to reading array data.

Word / Byte Programming Command

The device may be programmed by byte or by word, depending on the state of the Byte# Pin. Programming the EN29F800 is performed by using a four bus-cycle operation (two unlock write cycles followed by the Program Setup command and Program Data Write cycle). When the program command is executed, no additional CPU controls or timings are necessary. An internal timer terminates the program operation automatically. Address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever is last; data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever is first.

Programming status may be checked by sampling data on DQ7 ($\overline{DATA}$ polling) or on DQ6 (toggle bit). When the program operation is successfully completed, the device returns to read mode and the user can read the data programmed to the device at that address. Note that data can not be programmed from a 0 to a 1. Only an erase operation can change a data from 0 to 1. When programming time limit is exceeded, DQ5 will produce a logical "1" and a Reset command can return the device to Read mode.

Chip Erase Command

Chip erase is a six-bus-cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. The Command Definitions table shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Embedded Chip Erase algorithm are ignored.

The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. See “Write Operation Status” for information on these status bits. When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Flowchart 4 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in “AC Characteristics” for parameters, and to the Chip/Sector Erase Operation Timings for timing waveforms.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two un-lock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The Command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to “Write Operation Status” for information on these status bits. Flowchart 4 illustrates the algorithm for the erase operation. Refer to the Erase/Program Operations tables in the “AC Characteristics” section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

Erase Suspend / Resume Command

The Erase Suspend command allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don’t-cares when writing the Erase Suspend command.

When the Erase Suspend command is written during a sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation.

After the erase operation has been suspended, the system can read array data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Normal read and write timings and command definitions apply. Reading at any address within erase-suspended sectors produces status data on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. See “Write Operation Status” for information on these status bits.

After an erase-suspended program operation is complete, the system can once again read array data within non-suspended sectors. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See “Write Operation Status” for more information. The Autoselect command is not supported during Erase Suspend Mode.

The system must write the Erase Resume command (address bits are don’t-care) to exit the erase suspend mode and continue the sector erase operation. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the device has resumed erasing.

WRITE OPERATION STATUS

DQ7
$\overline{\text{DATA}}$ Polling

The EN29F800 provides $\overline{\text{DATA}}$ Polling on DQ7 to indicate to the host system the status of the embedded operations. The $\overline{\text{DATA}}$ Polling feature is active during the Byte Programming, Sector Erase, Chip Erase, Erase Suspend. (See Table 6)

When the Byte Programming is in progress, an attempt to read the device will produce the complement of the data last written to DQ7. Upon the completion of the Byte Programming, an attempt to read the device will produce the true data last written to DQ7. For the Byte Programming, $\overline{\text{DATA}}$ polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the four-cycle sequence.

When the embedded Erase is in progress, an attempt to read the device will produce a "0" at the DQ7 output. Upon the completion of the embedded Erase, the device will produce the "1" at the DQ7 output during the read. For Chip Erase, the $\overline{\text{DATA}}$ polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse in the six-cycle sequence. For Sector Erase, $\overline{\text{DATA}}$ polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ or $\overline{\text{CE}}$ pulse.

$\overline{\text{DATA}}$ Polling must be performed at any address within a sector that is being programmed or erased and not a protected sector. Otherwise, $\overline{\text{DATA}}$ polling may give an inaccurate result if the address used is in a protected sector.

Just prior to the completion of the embedded operations, DQ7 may change asynchronously when the output enable ($\overline{\text{OE}}$) is low. This means that the device is driving status information on DQ7 at one instant of time and valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status of valid data. Even if the device has completed the embedded operations and DQ7 has a valid data, the data output on DQ0-DQ6 may be still invalid. The valid data on DQ0-DQ7 will be read on the subsequent read attempts.

The flowchart for $\overline{\text{DATA}}$ Polling (DQ7) is shown on Flowchart 5. The $\overline{\text{DATA}}$ Polling (DQ7) timing diagram is shown in Figure 8.

RY/BY: Ready/Busy

The $\overline{\text{RY/BY}}$ is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The $\overline{\text{RY/BY}}$ status is valid after the rising edge of the final $\overline{\text{WE}}$ pulse in the command sequence. Since $\overline{\text{RY/BY}}$ is an open-drain output, several $\overline{\text{RY/BY}}$ pins can be tied together in parallel with a pull-up resistor to Vcc.

In the output is low, signifying Busy, the device is actively erasing or programming. This includes programming in the Erase Suspend mode. If the output is high, signifying the Ready, the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

DQ6 Toggle Bit I

The EN29F800 provides a "Toggle Bit" on DQ6 to indicate to the host system the status of the embedded programming and erase operations. (See Table 6)

During an embedded Program or Erase operation, successive attempts to read data from the device at any address (by toggling $\overline{\text{OE}}$ or $\overline{\text{CE}}$) will result in DQ6 toggling between "zero" and "one". Once the embedded Program or Erase operation is complete, DQ6 will stop toggling and valid data will be

read on the next successive attempts. During Byte Programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{WE}$ pulse in the four-cycle sequence. For Chip Erase, the Toggle Bit is valid after the rising edge of the sixth-cycle sequence. For Sector Erase, the Toggle Bit is valid after the last rising edge of the Sector Erase $\overline{WE}$ pulse.

In Byte Programming, if the sector being written to is protected, DQ6 will toggles for about 2 µs, then stop toggling without the data in the sector having changed. In Sector Erase or Chip Erase, if all selected blocks are protected, DQ6 will toggle for about 100 µs. The chip will then return to the read mode without changing data in all protected blocks.

Toggling either $\overline{CE}$ or $\overline{OE}$ will cause DQ6 to toggle.

The flowchart for the Toggle Bit (DQ6) is shown in Flowchart 6. The Toggle Bit timing diagram is shown in Figure 9.

DQ5 Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1.” This is a failure condition that indicates the program or erase cycle was not successfully completed. Since it is possible that DQ5 can become a 1 when the device has successfully completed its operation and has returned to read mode, the user must check again to see if the DQ6 is toggling after detecting a “1” on DQ5.

The DQ5 failure condition may appear if the system tries to program a “1” to a location that is previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, DQ5 produces a “1.” Under both these conditions, the system must issue the reset command to return the device to reading array data.

DQ3 Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be used to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from “0” to “1.” This device does not support multiple sector erase command sequences so it is not very meaningful since it immediately shows as a “1” after the first 30h command. Future devices may support this feature.

DQ2 Erase Toggle Bit II

The “Toggle Bit” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for era-sure. Thus, both status bits are required for sector and mode information. Refer to Table 5 to compare outputs for DQ2 and DQ6.

Flowchart 6 shows the toggle bit algorithm, and the section “DQ2: Toggle Bit” explains the algorithm. See also the “DQ6: Toggle Bit I” subsection. Refer to the Toggle Bit Timings figure for the toggle bit timing diagram. The DQ2 vs. DQ6 figure shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Flowchart 6 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling.

Typically, a system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Flowchart 6).

Write Operation Status

Operation		DQ7	DQ6	DQ5	DQ3	DQ2	RY/BY #
Standard Mode	Embedded Program Algorithm	DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm	0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Reading within Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	1
	Reading within Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend Program	DQ7#	Toggle	0	N/A	N/A	0

Table 6. Status Register Bits

DQ	Name	Logic Level	Definition
7	$\overline{\text{DATA}}$ POLLING	‾‾‾‾ ‘1’	Erase Complete or erase Sector in Erase suspend
		‘0’	Erase On-Going
		DQ7	Program Complete or data of non-erase Sector during Erase Suspend
		DQ7	Program On-Going
6	TOGGLE BIT	‘-1-0-1-0-1-0-1-’	Erase or Program On-going
		DQ6	Read during Erase Suspend
		‘-1-1-1-1-1-1-1-‘	Erase Complete
5	ERROR BIT	‘1’	Program or Erase Error
		‘0’	Program or Erase On-going
3	ERASE TIME BIT	‘1’	Erase operation start
		‘0’	Erase timeout period on-going
2	TOGGLE BIT	‘-1-0-1-0-1-0-1-’	Chip Erase, Erase or Erase suspend on currently addressed Sector. (When DQ5=1, Erase Error due to currently addressed Sector. Program during Erase Suspend on-going at current address
		DQ2	Erase Suspend read on non Erase Suspend Sector

Notes:

DQ7 $\overline{\text{DATA}}$ Polling: indicates the P/E C status check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.

DQ6 Toggle Bit: remains at constant level when P/E operations are complete or erase suspend is acknowledged. Successive reads output complementary data on DQ6 while programming or Erase operation are on-going.

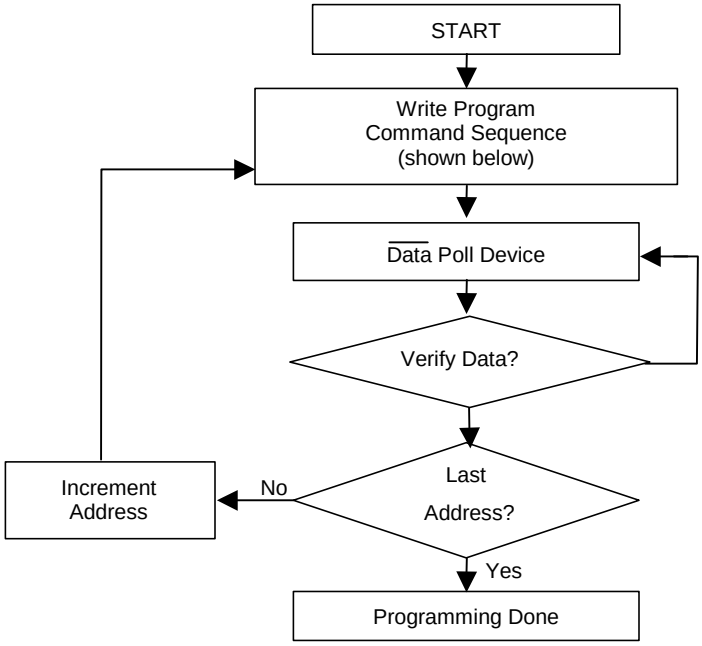
DQ5 Error Bit: set to “1” if failure in programming or erase

DQ3 Sector Erase Command Timeout Bit: Operation has started. Only possible command is Erase suspend (ES).

DQ2 Toggle Bit: indicates the Erase status and allows identification of the erased Sector.

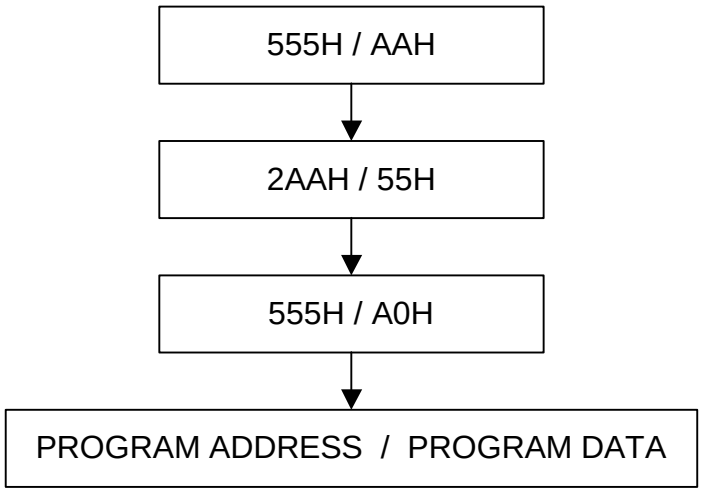
EMBEDDED ALGORITHMS

Flowchart 1. Embedded Program

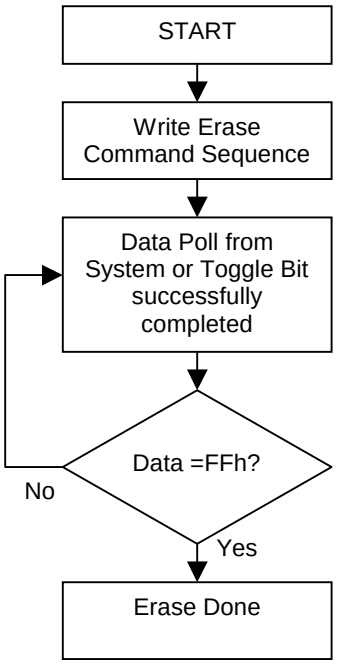


Flowchart 2. Embedded Program Command Sequence

See the Command Definitions section for more information.

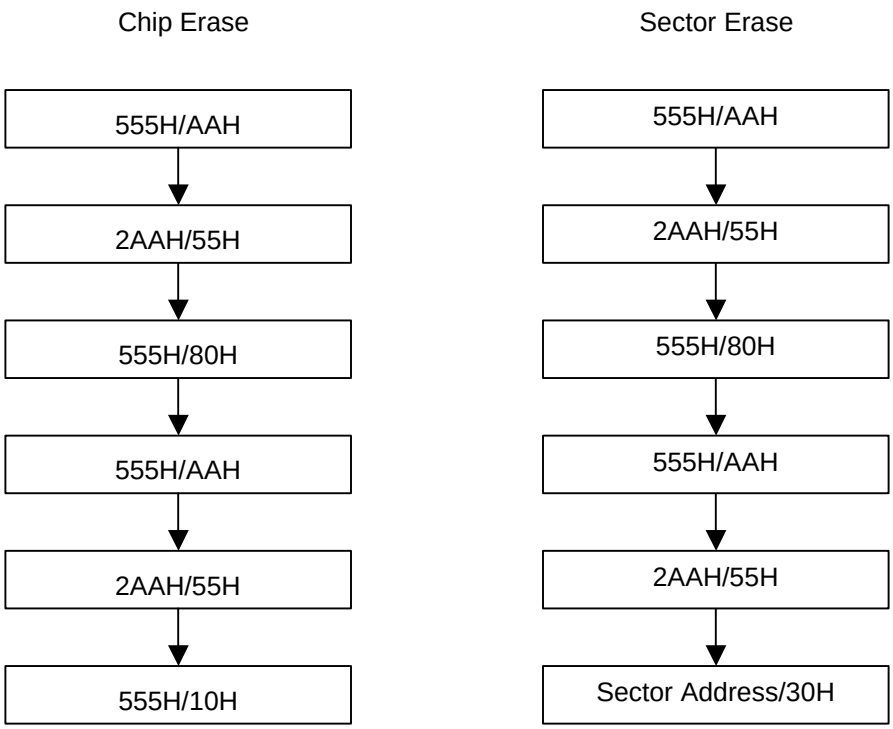


Flowchart 3. Embedded Erase

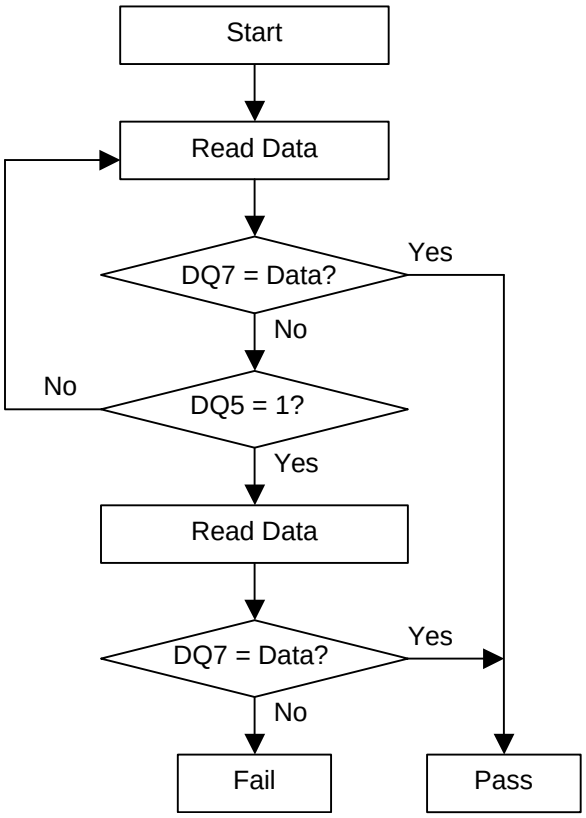


Flowchart 4. Embedded Erase Command Sequence

See the Command Definitions section for more information.



Flowchart 5. $\overline{\text{DATA}}$ Polling Algorithm



Flowchart 6. Toggle Bit Algorithm

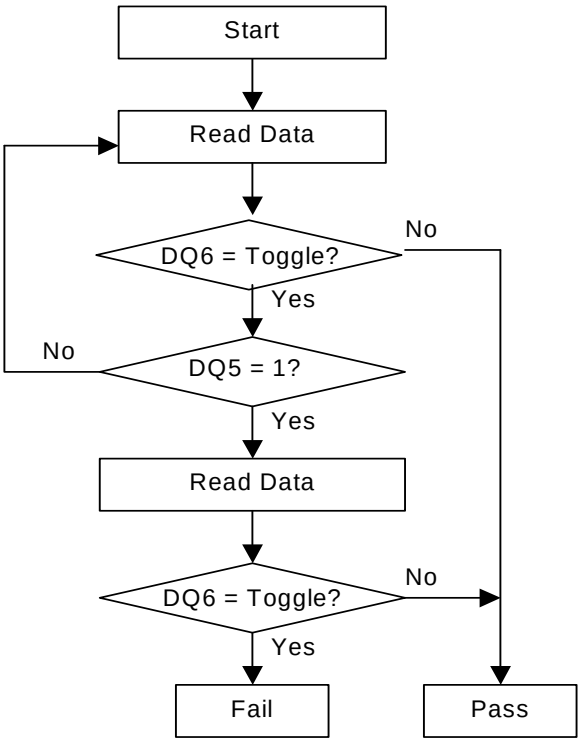


Table 7. DC Characteristics

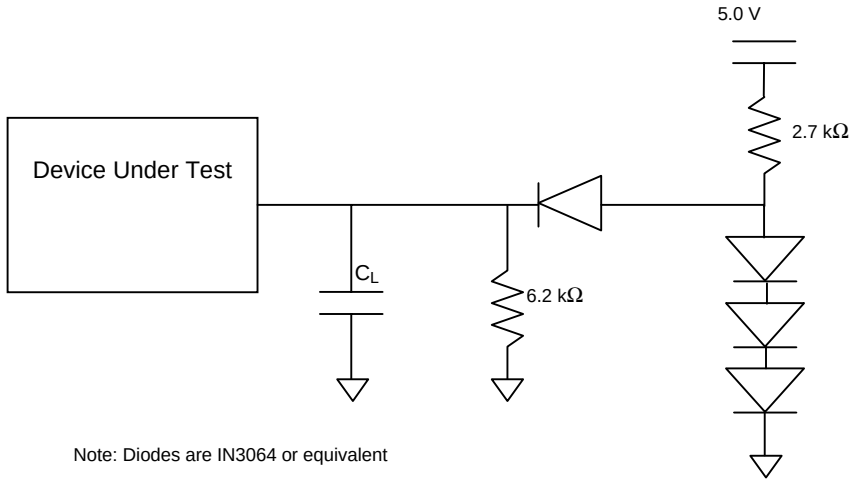
(T_a = 0°C to 70°C or - 40°C to 85°C; V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	0V≤ V_{IN} ≤ Vcc			±5	µA
I_{LO}	Output Leakage Current	0V≤ V_{OUT} ≤ Vcc			±5	µA
I_{CC1}	Supply Current (read) TTL	CE# = V_{IL}; OE# = V_{IH}; f = 5MHz		19	30	mA
	(read) CMOS Byte			20	40	mA
	(read) CMOS Word			28	50	mA
I_{CC2}	Supply Current (Standby - TTL)	CE# = V_{IH}		0.4	1.0	mA
	(Standby - CMOS) (1)	BYTE# = RESET# = CE# = Vcc ± 0.2V		0.3	5.0	µA
I_{CC3}	Supply Current (Program or Erase)	Byte program, Sector or Chip Erase in progress		30	60	mA
V_{IL}	Input Low Voltage		-0.5		0.8	V
V_{IH}	Input High Voltage		2		Vcc ± 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = -2.5 mA	2.4			V
	Output High Voltage CMOS	I_{OH} = -100 µA	Vcc - 0.4V			V
V_{ID}	A9 Voltage (Electronic Signature)		10.5		11.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}			100	µA
V_{LKO}	Supply voltage (Erase and Program lock-out)		3.2		4.2	V

Notes:

(1) BYTE# and RESET# pin input buffers are always enabled so that they draw power if not at full CMOS supply voltages

Test Conditions



Note: Diodes are IN3064 or equivalent

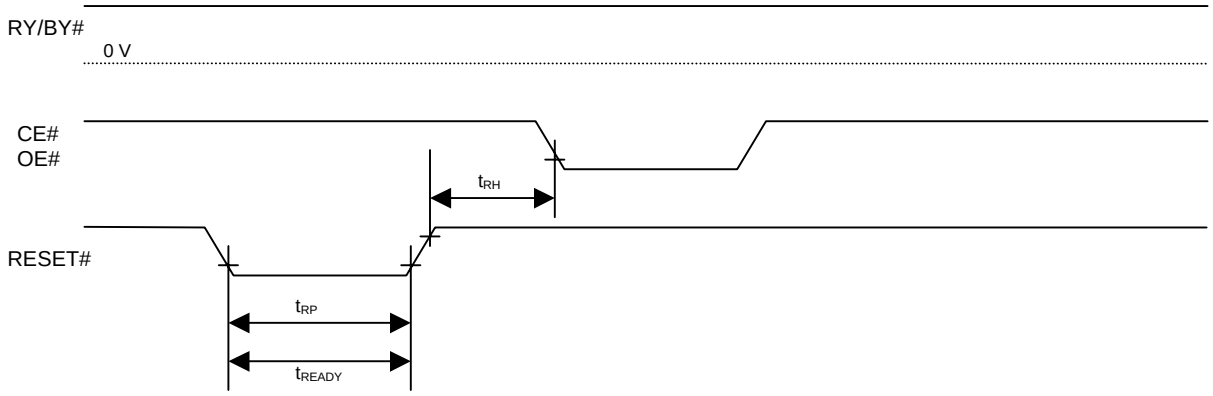
Test Specifications

Test Conditions	-45	-55	-70	-90	Unit
Output Load	1 TTL Gate				
Output Load Capacitance, C_L	30	30	100	100	pF
Input Rise and Fall times	5	5	20	20	ns
Input Pulse Levels	0.0-0.3	0.0-0.3	0.45-2.4	0.45-2.4	V
Input timing measurement reference levels	1.5	1.5	0.8, 2.0	0.8, 2.0	V
Output timing measurement reference levels	1.5	1.5	0.8, 2.0	0.8, 2.0	V

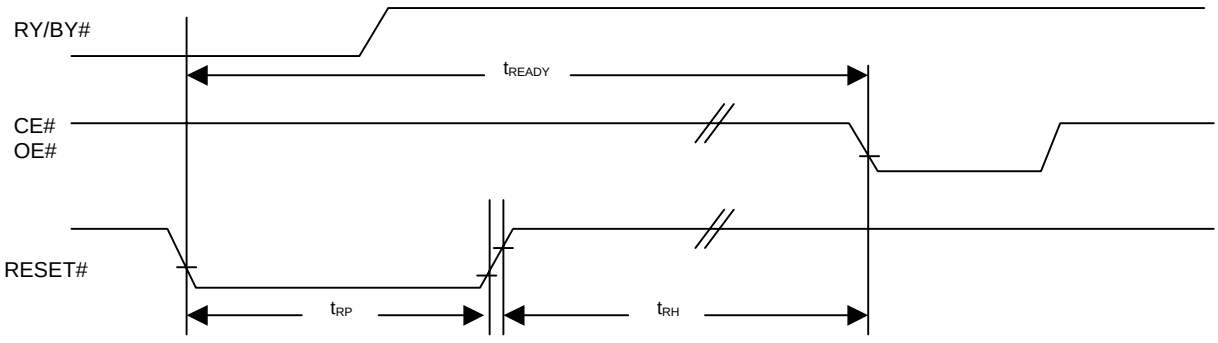
AC CHARACTERISTICS
Hardware Reset (Reset#)

Parameter Std	Description	Test Setup	Speed options				Unit
			-45	-55	-70	-90	
t_{READY}	Reset# Pin Low to Read or Write Embedded Algorithms	Max	20				µs
t_{READY}	Reset# Pin Low to Read or Write Non Embedded Algorithms	Max	500				ns
t_{RP}	Reset# Pulse Width	Min	500				ns
t_{RH}	Reset# High Time Before Read	Min	50				ns

Reset# Timings



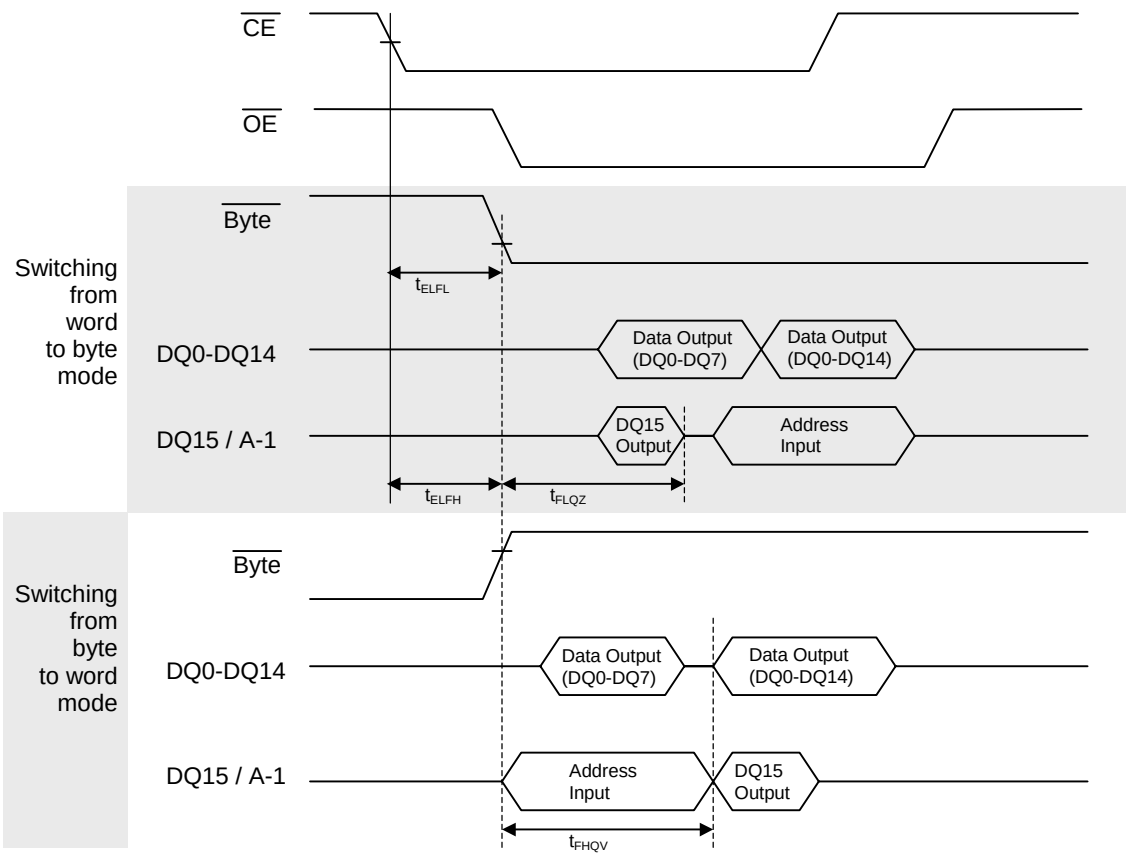
Reset Timings NOT During Automatic Algorithms



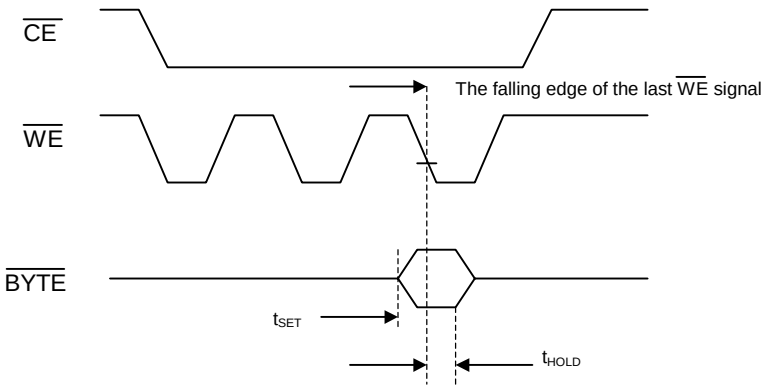
Reset Timings During Automatic Algorithms

AC CHARACTERISTICS
Word / Byte Configuration (Byte#)

Std Parameter	Description		Speed					Unit
			-45	-55	-70	-90	-120	
t_{ELFL}/t_{ELFH}	CE# to Byte# switching Low or High	Max	0	0	0	0	0	ns
t_{FLQZ}	Byte# switching Low to Output HIGH Z	Max	20	20	20	20	30	ns
t_{FHQV}	Byte# switching High to Output Active	Min	45	55	70	90	120	ns



Byte timings for Read Operations



Byte timings for Read Operations

Table 8. AC CHARACTERISTICS
Read-only Operations Characteristics

Parameter Symbols			Test Setup		Speed Options				
JEDEC	Standard	Description			-45	-55	-70	-90	Unit
t_{AVAV}	t_{RC}	Read Cycle Time		Min	45	55	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	45	55	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable To Output Delay	$\overline{OE} = V_{IL}$	Max	45	55	70	90	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	25	30	30	35	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z		Max	20	20	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z		Max	20	20	20	20	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, $\overline{CE}$ or $\overline{OE}$, whichever occurs first		Min	0	0	0	0	ns

Notes:

For - 50
Vcc = 5.0V ± 5%
Output Load : 1 TTL gate and 30pF
Input Rise and Fall Times: 5ns
Input Rise Levels: 0.0 V to 3.0 V
Timing Measurement Reference Level, Input and Output: 1.5 V

For all others:
Vcc = 5.0V ± 10%
Output Load: 1 TTL gate and 100 pF
Input Rise and Fall Times: 20 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level, Input and Output: 0.8 V and 2.0 V

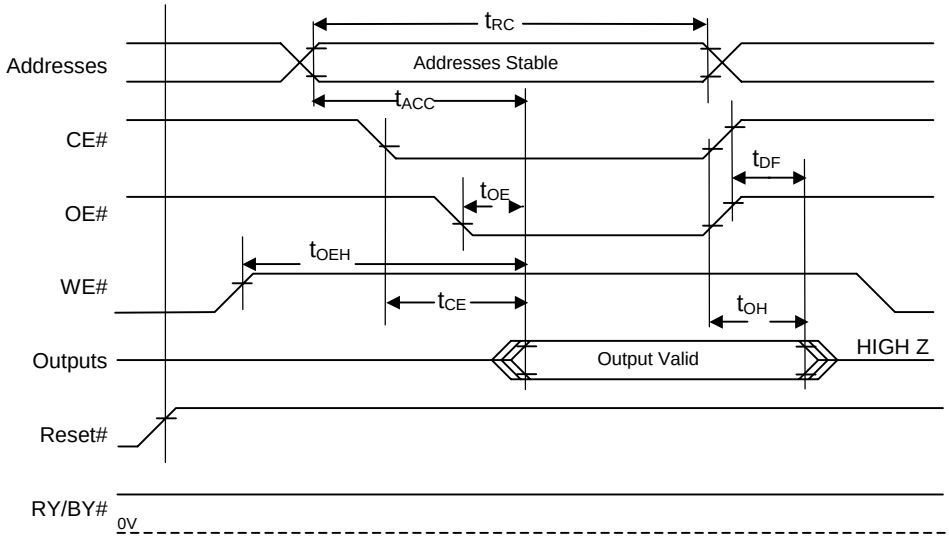


Figure 5. AC Waveforms for READ Operations

Table 9. AC CHARACTERISTICS

Write (Erase/Program) Operations

Parameter Symbols		Description			Speed Options				
JEDEC	Standard				-45	-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min	45	55	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	25	30	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	MIn	0	0	0	0	ns
			Toggle and $\overline{DATA}$ Polling	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ SetupTime		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	35	45	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (Word AND Byte Mode)		Typ	7	7	7	7	µs
				Max	200	200	200	200	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.3	0.3	0.3	0.3	s
				Max	5	5	5	5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation		Typ	3	3	3	3	s
				Max	35	35	35	35	s
	t_{VCS}	Vcc Setup Time		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns

Table 10. AC CHARACTERISTICS
Write (Erase/Program) Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols					Speed Options				
JEDEC	Standard	Description			-45	-55	-70	-90	Unit
t_{AVAV}	t_{WC}	Write Cycle Time		Min	45	55	70	90	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	20	25	30	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read	0	0	0	0	0	ns
			Toggle and Data Polling	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time before Write ($\overline{OE}$ High to $\overline{CE}$ Low)		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ SetupTime		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width		Min	25	30	35	45	ns
t_{EHEL}	t_{CPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation (byte AND word mode)		Typ	7	7	7	7	µs
				Max	200	200	200	200	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.3	0.3	0.3	0.3	s
				Max	5	5	5	5	s
t_{WHWH3}	t_{WHWH3}	Chip Erase Operation		Typ	3	3	3	3	s
				Max	35	35	35	35	s
	t_{VCS}	Vcc Setup Time		Min	50	50	50	50	µs
	t_{VIDR}	Rise Time to V_{ID}		Min	500	500	500	500	ns

Table 11. ERASE AND PROGRAMMING PERFORMANCE

Parameter		Limits			Comments
		Typ	Max	Unit	
Sector Erase Time		1	8	sec	Excludes 00H programming prior to erasure
Chip Erase Time		19	35	sec	
Byte Programming Time		7	300	µs	Excludes system level overhead
Word Programming Time		7	300	µs	
Chip Programming Time	Byte	8.2	24.5	sec	
	Word	4.1	12.2		
Erase/Program Endurance		100K		cycles	Minimum 100K cycles guaranteed

Table 12. LATCH UP CHARACTERISTICS

Parameter Description	Min	Max
Input voltage with respect to V_{ss} on all pins except I/O pins (including A9, Reset and $\overline{OE}$)	-1.0 V	12.0 V
Input voltage with respect to V_{ss} on all I/O Pins	-1.0 V	Vcc + 1.0 V
Vcc Current	-100 mA	100 mA

Note : These are latch up characteristics and the device should never be put under these conditions. Refer to Absolute Maximum ratings for the actual operating limits.

Table 14. 32-PIN TSOP PIN CAPACITANCE @ 25°C, 1.0MHz

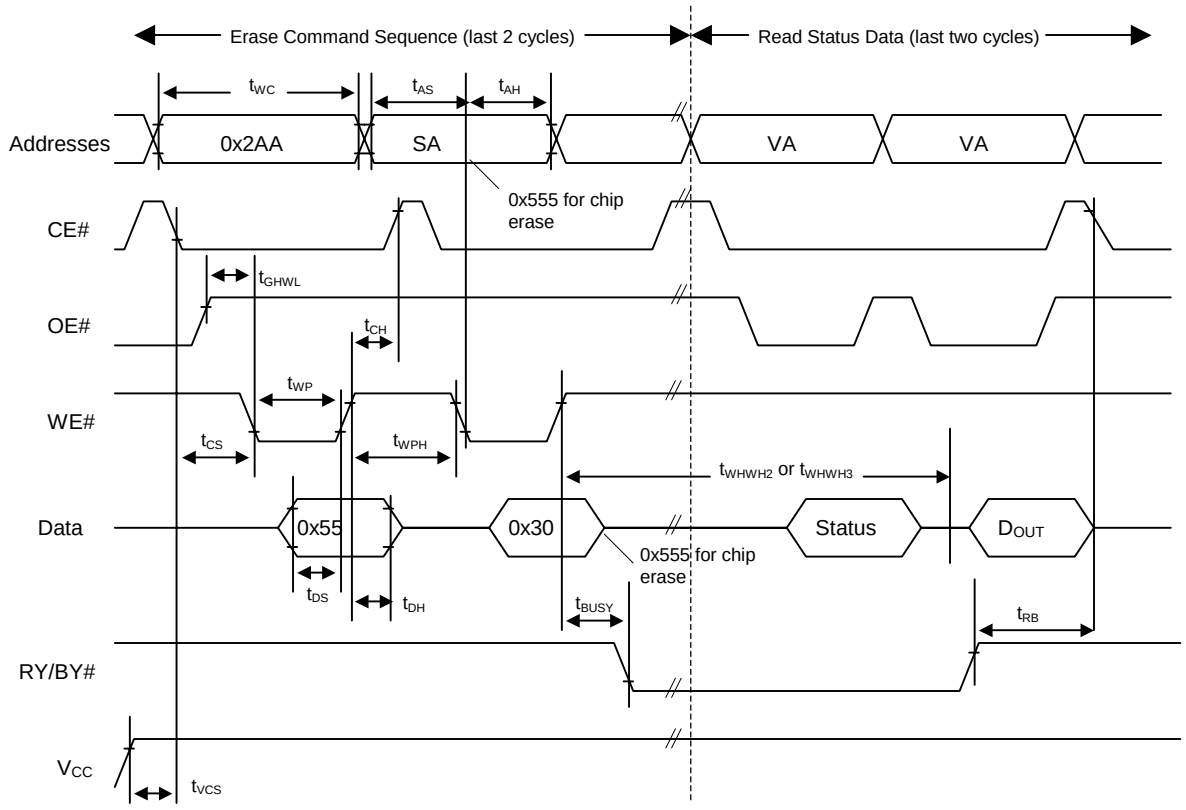
Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Table 15. DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

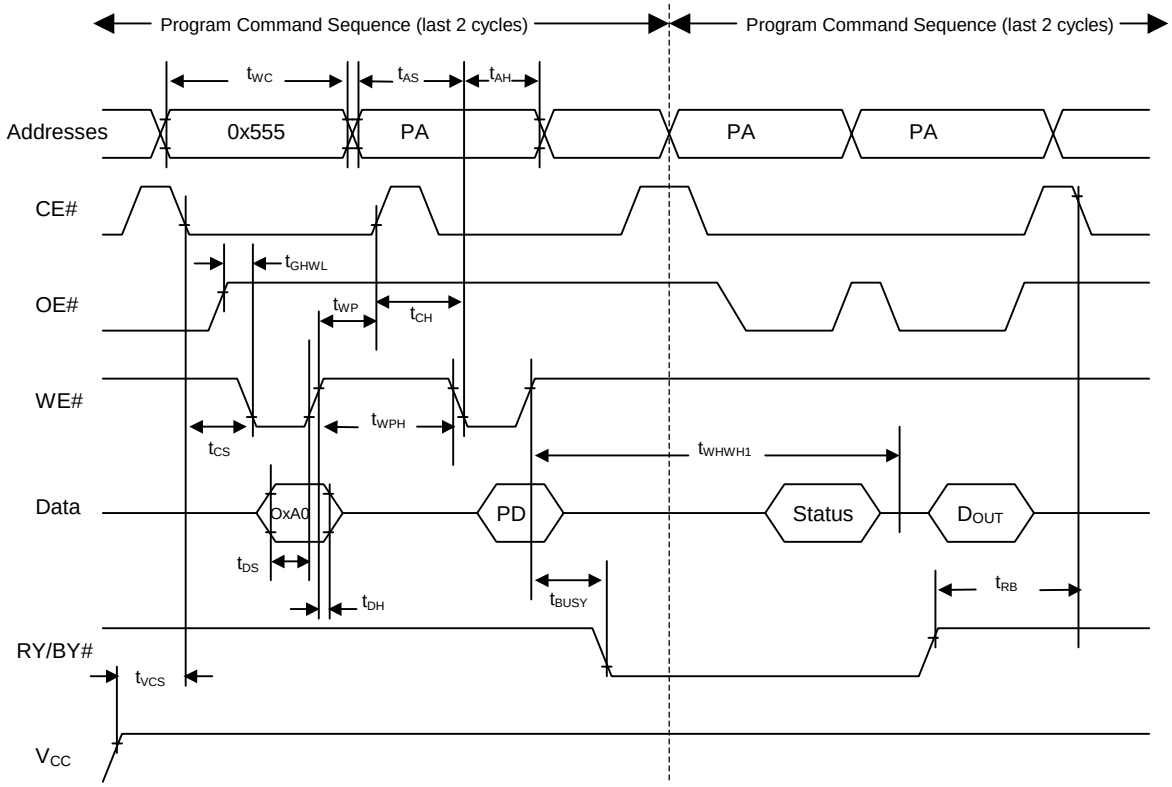
SWITCHING WAVEFORMS

Figure 6. AC Waveforms for Chip/Sector Erase Operations Timings



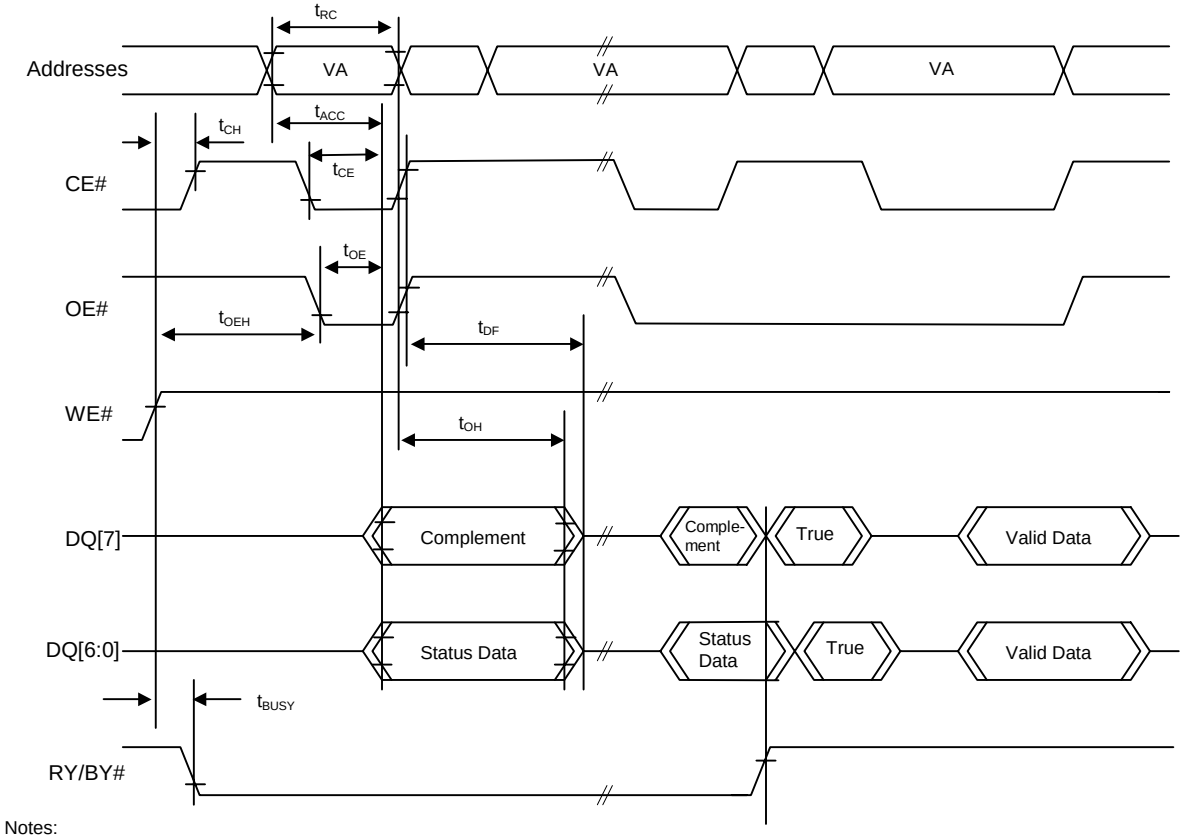
Notes:
1. SA=Sector Address (for sector erase), VA=Valid Address for reading status, D_{out}=true data at read address.
2. V_{cc} shown only to illustrate t_{vcs} measurement references. It cannot occur as shown during a valid command sequence.

Figure 7. Program Operation Timings



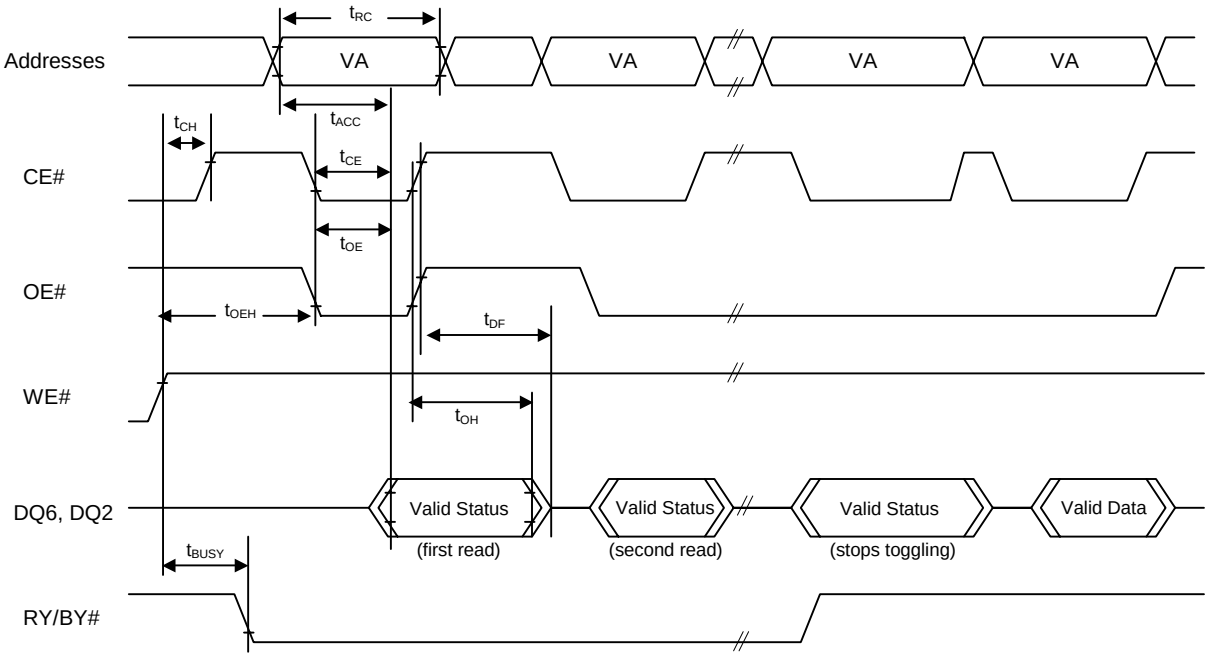
Notes:
1. PA=Program Address, PD=Program Data, D_{OUT} is the true data at the program address.
2. V_{CC} shown in order to illustrate t_{VCS} measurement references. It cannot occur as shown during a valid command sequence.

Figure 8. AC Waveforms for /DATA Polling During Embedded Algorithm Operations

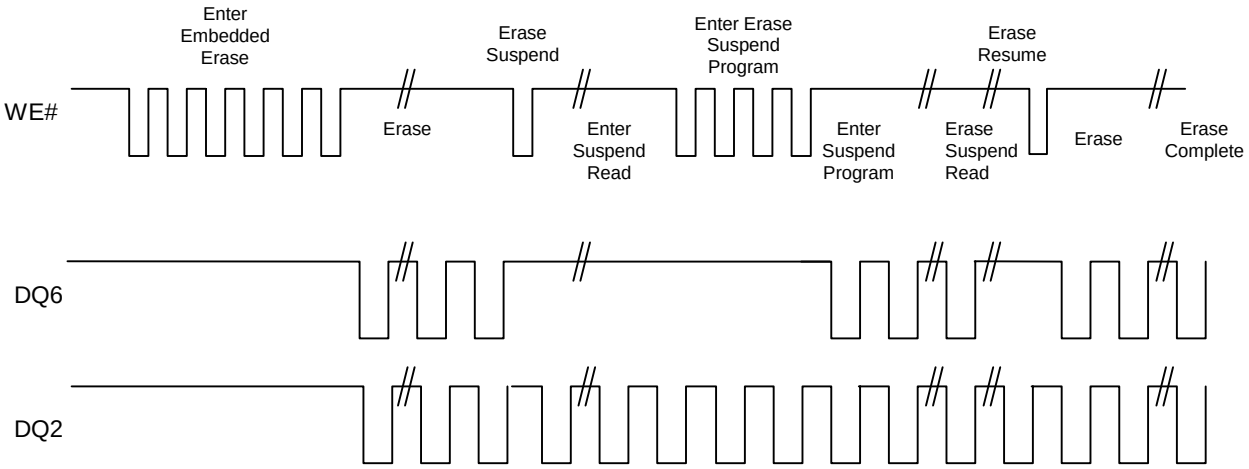


Notes:
1. VA=Valid Address for reading Data# Polling status data
2. This diagram shows the first status cycle after the command sequence, the last status read cycle and the array data read cycle.

Figure 9. AC Waveforms for Toggle Bit During Embedded Algorithm Operations



AC CHARACTERISTICS



DQ2 vs. DQ6

Temporary Sector Unprotect

Parameter Std	Description		Speed Option				Unit
			-45	-55	-70	-90	
t_{VIDR}	V_{ID} Rise and Fall Time	Min	500				Ns
t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4				µs

Temporary Sector Unprotect Timing Diagram

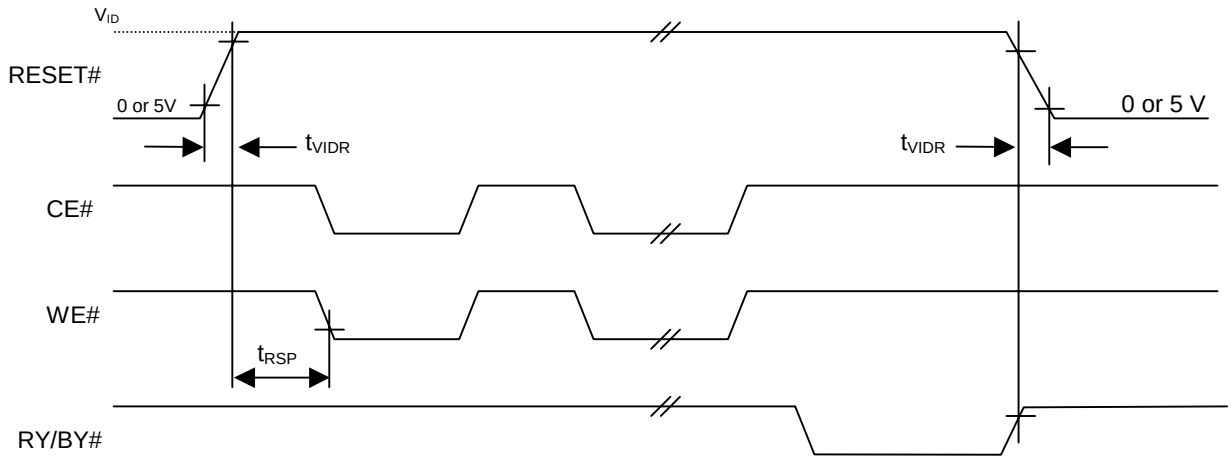
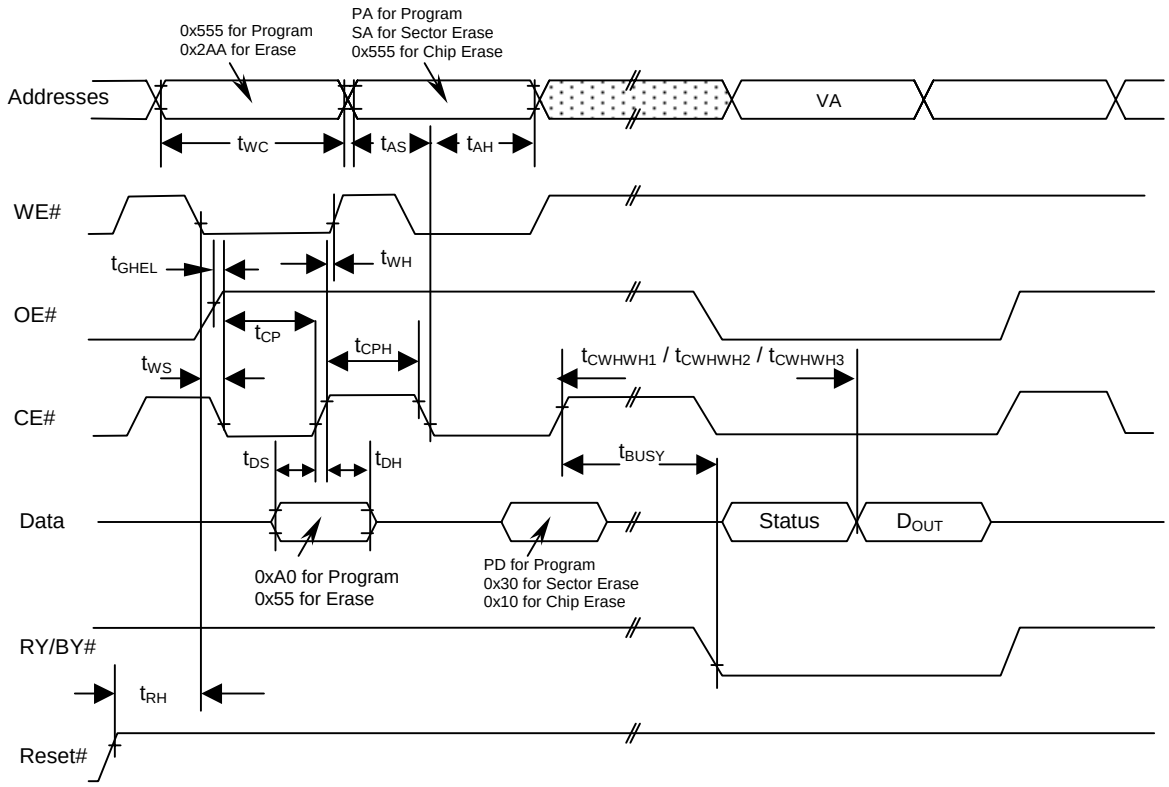


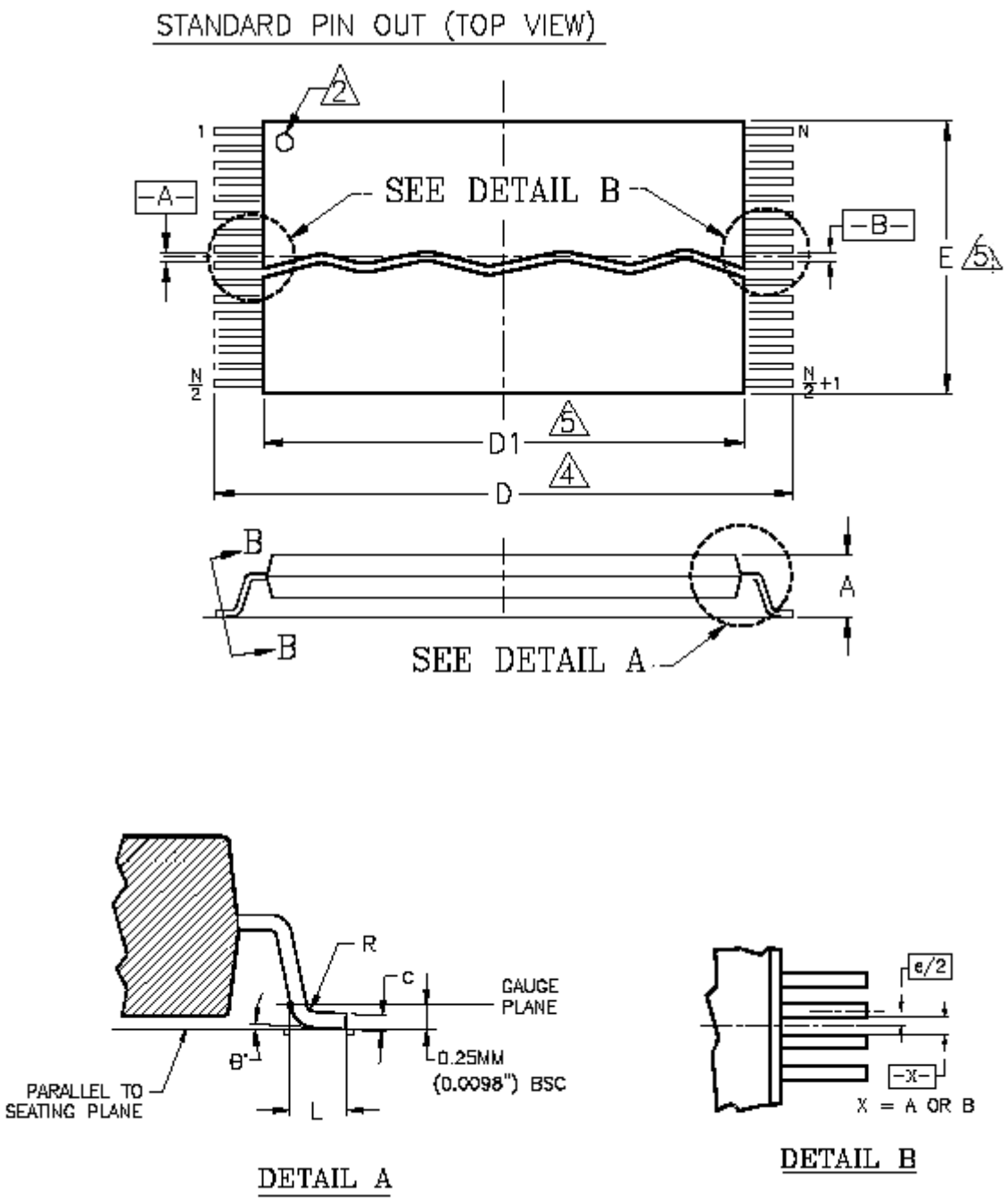
Figure 10. Alternate CE# Controlled Write Operation Timings

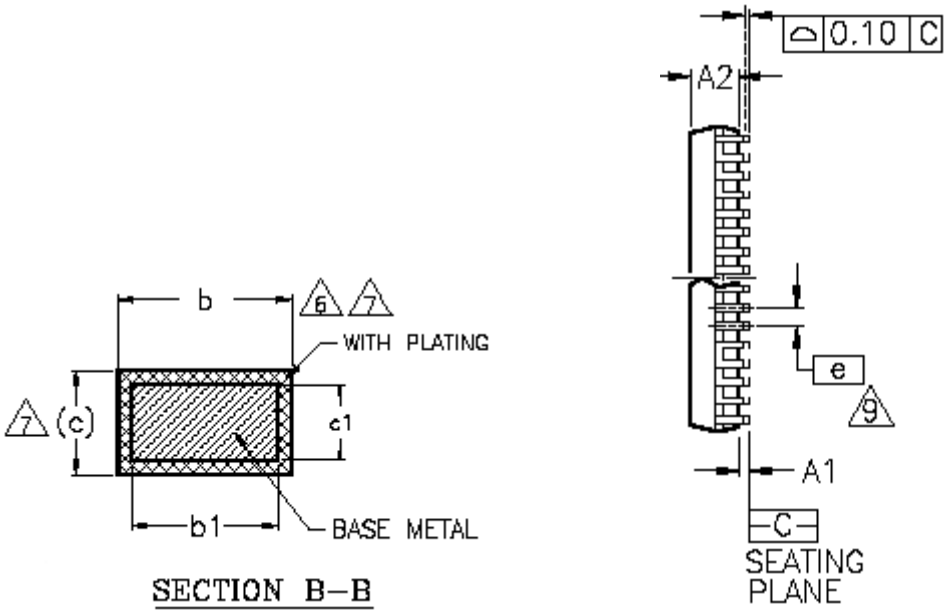


Notes:

PA = address of the memory location to be programmed.
PD = data to be programmed at byte address.
VA = Valid Address for reading program or erase status
D_{out} = array data read at VA
Shown above are the last two cycles of the program or erase command sequence and the last staus read cycle
Reset# shown to illustrate t_{RH} measurement references. It cannot occur as shown during a valid command sequence.

FIGURE 4. TSOP





Package			
Jedec			
Symbol	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	9.90	10.00	10.10
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	3°	5°
R	0.08	—	0.20
N	40		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982)
2. 'PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
4. TO BE DETERMINED AT THE SEATING PLANE -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15mm (.0059") PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08mm (0.0031") TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm (0.0028").
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm (.0039") AND 0.25mm (0.0098") FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm (0.004") AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

ABSOLUTE MAXIMUM RATINGS

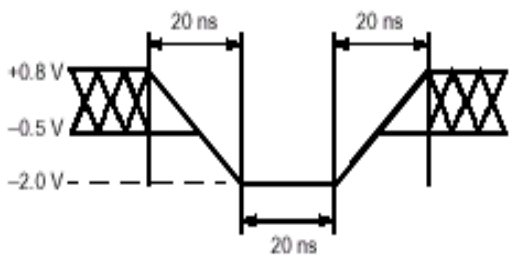
Parameter		Value	Unit
Storage Temperature		-65 to +125	°C
Plastic Packages		-65 to +125	°C
Ambient Temperature With Power Applied		-55 to +125	°C
Output Short Circuit Current[1]		200	mA
Voltage with Respect to Ground	A9, OE#, Reset# [2]	-0.5 to +11.5	V
	All other pins [3]	-0.5 to Vcc+0.5	V
	Vcc	-0.5 to +7.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# pins is –0.5V. During voltage transitions, A9, OE#, RESET# pins may undershoot V_{SS} to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 11.5V which may overshoot to 12.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{SS} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

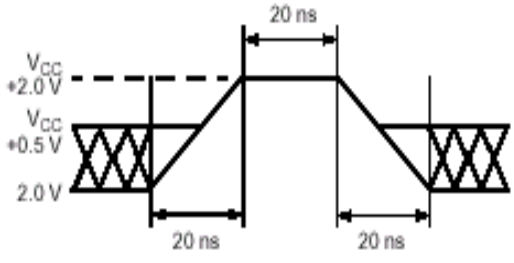
RECOMMENDED OPERATING RANGES[1]

Parameter	Value	Unit
Ambient Operating Temperature Commercial Devices Industrial Devices	 0 to 70 -40 to 85	°C
Operating Supply Voltage Vcc for ± 5% devices Vcc for ± 10% devices	 4.75 to 5.25 4.5 to 5.5	V

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



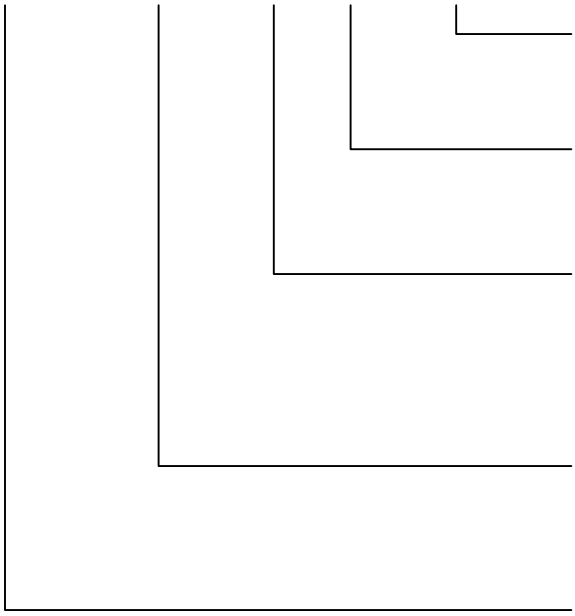
Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

ORDERING INFORMATION

EN29F800 T 45 T I



TEMPERATURE RANGE
(Blank) = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE
T = 48-pin TSOP
S = Small Outline Package

SPEED
45 = 45ns
55 = 55ns
70 = 70ns
90 = 90ns

BOOT CODE SECTOR ARCHITECTURE
T = Top Sector
B = Bottom Sector

BASE PART NUMBER
EN = EON Silicon Devices
29F = FLASH, 5V Read Program Erase
800 = 8 Megabit (1024K x 8 / 512 x 16)

Revisions List

A,B,C:

Preliminary

D (2001.07.03):

Table 7. Icc2 is with BYTE# and RESET# pin at full CMOS levels

Pg. 9 Logical Inhibit section now says that if $\overline{CE}$, $\overline{WE}$, and $\overline{OE}$ are all logical zero (not recommended usage), it will be considered a write.

VID is everywhere changed to be V_{ID} =11.5 ± 0.5V

E (2001.07.05):

“block” changed to “sector”

LACTHUP >= 200mA line removed from first page

Deleted Sector Un/Protect flowcharts

Chip erase and Sector Erase command descriptions modified.

DQ7,DQ5,DQ3 status polling descriptions modified.

Table 12 Latchup characteristics modified

Changed P/E endurance to 100K everywhere

Changed Absolute Maximum Ratings