ESS Technology, Inc.

ES2838
V.90/V.92 PCI HSP Modem
Product Brief

DESCRIPTION

The ES2838 is a high-performance, single-chip, host-based modem solution that delivers high connectivity and throughput without the need for a dedicated DSP. With the addition of an external transformer DAA, the ES2838 *Tele***Drive**® modem chip provides a very low-cost modem solution for add-in cards, desktops, and notebooks.

The ES2838 modem is capable of send/receive data and fax and supports telephone answering machine (TAM), and is capable data/fax/voice call discrimination. With its built-in ACPI and ***D3$_{cold}$*** wake-on-ring support, the ES2838 is an ideal modem solution for notebooks and battery-operated devices.

The ES2838 includes a PCI bus interface and a codec. It also includes ADC and DAC conversion of modem/voice signal data and provide the interface and control logic needed to transfer data between its serial I/O terminals and the PCI interface. The ES2838 ADC and DAC operate synchronously so that data reception at the ADC channel and data transmission from the DAC channel occur during the same time interval.

The ES2838 modem solution meets all the requirements Microsoft WHQL certification, as well as V.250, V.251, and V.253 commands.

The ES2838 is available in a 100-pin low-profile quad flat pack (LQFP) package.

FEATURES

- V.90/V.92 analog data/fax/TAM modem
- Data mode capabilities:
  - —— V.90/V.92: 56 kbps
  - —— ITU-T V.34: 33.6 kbps and fallbacks
- Fax mode capabilities:
  - —— ITU-T V.17, V.29, V.27ter, and V.21ch2
  - —— Group 3 (TIA/EIA-578 Class 1 and Class 2)
- Requires minimum 166-MHz Pentium with MMX technology
- PC99/PC2001-compliant with support for V.250, V.251, and V.253 commands
- V.80 (H.324 software-stack -compatible)
- Buzzer generator feature generates oscillation on handshaking
- Caller ID
- Data/fax/voice call discrimination
- Worldwide homologation
- Compliance with ACPI 1.0 and PCI Power Management Interface 1.0, supporting the ***D3$_{cold}$*** wake-on-ring
- 16-bit ADC and DAC with built-in anti-aliasing and reconstruction filters
- Separate analog (5V) and digital (3.3V with 5V-tolerant input pads) power supplies
- Internal PLL requiring a lower-frequency crystal for 18.816-MHz input
- EEPROM interface for subsystem vendor ID
- Supports Microsoft Windows™ Unimodem V and TAPI specifications
- Supports Microsoft Windows 98/SE/ME/2000
- Supports Microsoft Windows NT 4.0

SYSTEM BLOCK DIAGRAM

Figure 1 shows the ES2838 system block diagram.

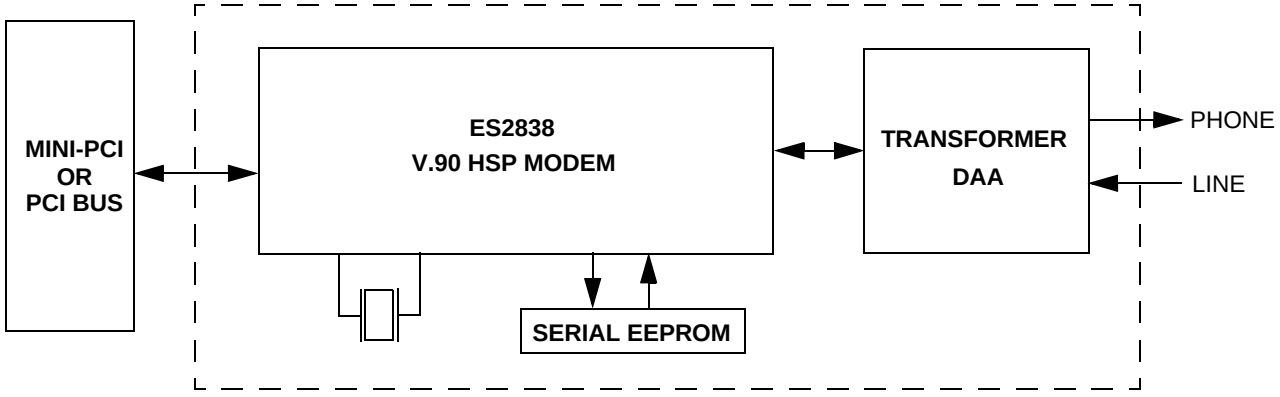

Figure 1 ES2838 System Block Diagram

PINOUT

Figure 2 shows the ES2838 pinout diagram.

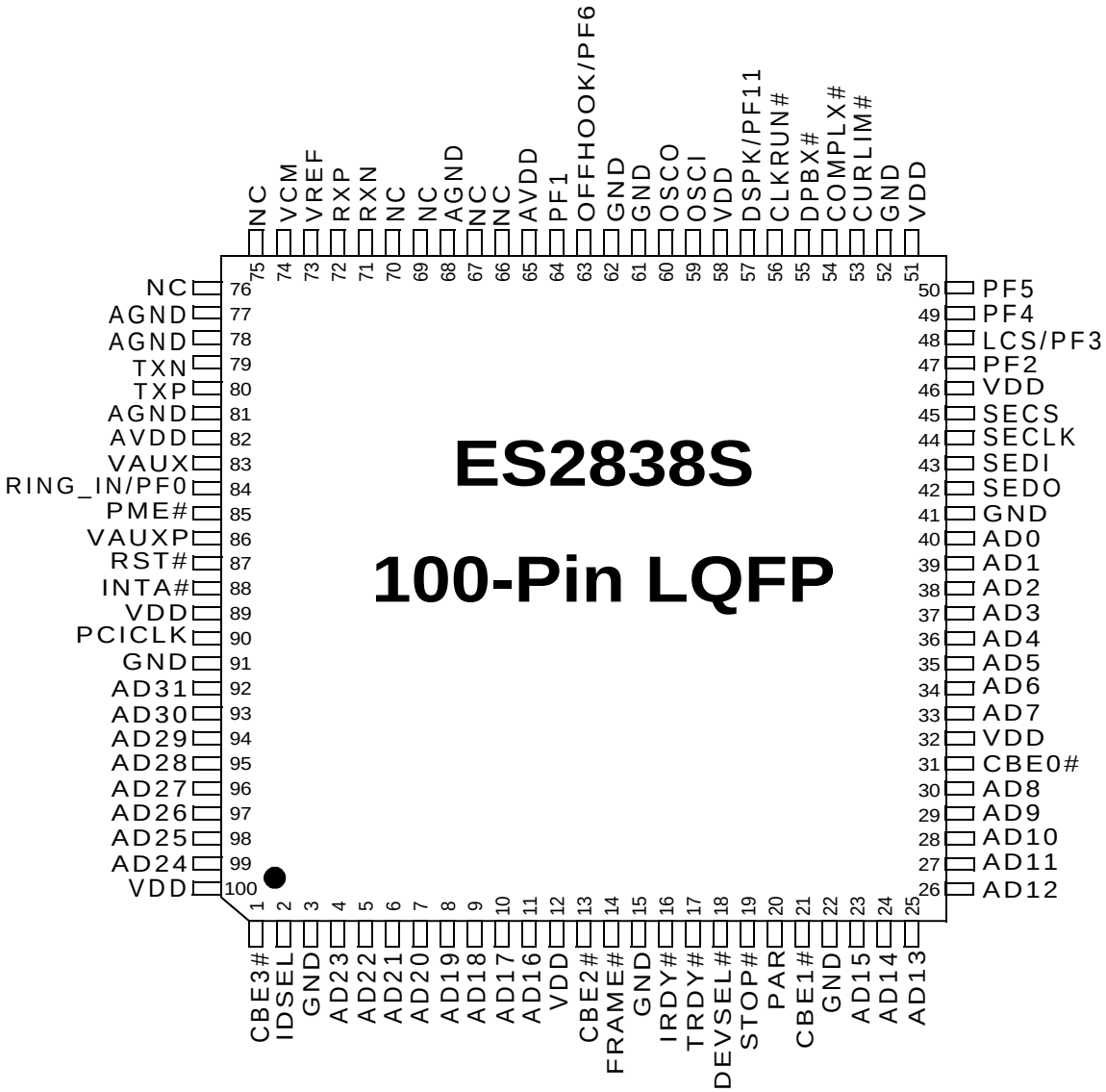

Figure 2 ES2838 Pinout Diagram

ES2838 PIN DESCRIPTIONS

Table 1 lists the ES2838 pin descriptions.

Table 1 ES2838 Pin Descriptions

Names	Pin Numbers	I/O	Definitions
C/BE3:0#	1, 13, 21, 31	I/O	Multiplexed bus command/byte enable. These pins indicate cycle type during the address phase of a transaction. They indicate active-low byte enable information for the current data phase during the data phases of a transaction. These pins are inputs during slave operation and outputs during bus mastering operation.
IDSEL	2	I	Initialization device select, active-high. Used as a chip select during PCI configuration read and write cycles.
GND	3, 15, 22, 41, 52, 61, 91	G	Digital ground.
VDD	12, 32, 46, 51, 58, 89, 100	P	Digital voltage [VDD (3.3V)].
AD31:0	4:11, 23:30, 33:40, 92:99	I/O	Address and data AD31:0.
FRAME#	14	I/O	Cycle frame, active-low. The current PCI bus master drives this pin to indicate the beginning and duration of a transaction.
IRDY#	16	I/O	Initiator ready, active-low. The current PCI bus master drives this pin to indicate that as the initiator it is ready to transmit or receive data (and complete the current data phase).
TRDY#	17	I/O	Target ready pin, active-low. The current PCI bus master drives this pin to indicate that as the target device it is ready to transmit or receive data (and complete the current data phase).
DEVSEL#	18	I/O	Device select, active-low. The PCI bus target device drives this pin to indicate that it has decoded the address of the current transaction as its own chip select range.
STOP#	19	I/O	Stop transaction, active-low. The current PCI bus target drives this pin active to indicate a request to the master to stop the current transaction.
PAR	20	I/O	Parity pin, active-high. Indicates even parity across AD[31:0] and C/BE[3:0]# for both address and data phases. The signal is delayed one PCI clock from either the address or data phase for which parity is generated.
SEDO	42	I	Serial EPROM data output pin with internal pullup.
SEDI	43	O	Serial EPROM data input pin.
SECLK	44	O	Serial EPROM data clock input pin with internal pulldown.
SECS	45	O	Serial EPROM port chip select pin with internal pulldown.
LCS / PF3	48	I	Local current sense input when selected.
PF[5:4] and PF[2:1]	47, 49, 50, 64	I/O	General-purpose programmable bidirectional flag. Can be used for interfacing with a telephone or other device, performing such functions as phone off-hook, phone on-hook, ring, and caller ID.
CURLIM#	53	O	Current limit control output.
COMPLX#	54	O	Complex impedance select output.
DPBX#	55	I	Digital PBX detection input.
CLKRUN#	56	I/O	PCI clock state for power management.
DSPK	57	O	Modem speaker digital output.
PF11		O	General-purpose programable flag.
OSCI	59	I	18.816-MHz crystal oscillator input.
OSCO	60	O	18.816-MHz crystal oscillator output.

Table 1 ES2838 Pin Descriptions (Continued)

Names	Pin Numbers	I/O	Definitions
OFFHOOK	63	O	Offhook output driving 5V.
PF6		O	General-purpose programmable flag.
AVDD	65, 82	P	Analog voltage pins [AVDD (5V)].
NC	66, 67, 69, 70, 75, 76	—	No connect.
AGND	68, 77, 78, 81	G	Analog ground.
RXN	71	I	Codec analog differential negative input. The DC level is Vcm, and the full-scale input is either 0.22 Vp-p ±5% or 1.1 Vp-p±5%, depending on the gain setting.
RXP	72	I	Codec analog differential positive input. The DC level is Vcm, and the full-scale input is either 0.22 Vp-p ±5% or 1.1 Vp-p±5%, depending on the gain setting.
VREF	73	O	Voltage reference bypass. Has a range of 1.2356V±5%. Bypass to AGND with 0.1-µF ceramic chip capacitor parallel with 10-µF tantalum capacitor.
VCM	74	O	Common mode voltage bypass. Has a range of 2.16V±5%. Bypass to AGND with 0.1-µF ceramic chip capacitor parallel with 10-µF tantalum capacitor.
TXN	79	O	Codec negative analog output. The DC level is Vcm, and the full-scale ac output is 2.8V p-p±5%. The maximum loading is 1k Ω in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD <–60 db) current is 10 mA rms.
TXP	80	O	Codec positive analog output. The DC level is Vcm, and the full-scale ac output is 2.8V p-p±5%. The maximum loading is 1k Ω in parallel with 20 pF for modem applications. For audio applications with low-impedance load, the maximum distortion-free (THD <–60 db) current is 10 mA rms.
VAUX	83	P	Power to device during implementation of the ***D3$_{cold}$*** state required by PCI Power Management Interface specification.
RING_IN	84	I	RING_IN function, using a Schmitt trigger.
PF0		O	General-purpose programable flag.
PME#	85	O	Power management enable interrupt output to wake up the system.
VAUXP	86	I	V_{AUX} support detection pin. V_{AUXP} pin is driven high to indicate that ACPI is supported with ***D3$_{cold}$*** state. No support when driven low.
RST#	87	I	Active-low ES2838 reset input.
INTA#	88	O	Interrupt request, active-low. The level triggered interrupt pin dedicated to servicing internal device interrupt sources.
PCICLK	90	I	System bus clock input.

ORDERING INFORMATION

Part Number	Description	Package
ES2838S	V.90/V.92 PCI HSP Modem	100-pin LQFP

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