ESS Technology, Inc.

ES3986
Digital-Audio Processor
Product Brief

DESCRIPTION

The ES3986 digital-audio processor chip is ESS Technology's highly integrated, optimal-quality, and cost-effective single-chip solution for the emerging digital-audio market. Its target applications include internet audio platforms, MP3 CD players in boom box and combination systems, portable MP3 CD player, etc.

Based on the programmable multimedia processor (PMP) architecture, the ES3986 integrates software-configurable 32-bit reduced instruction set computing (RISC) processor and a 64-bit vector processor core. The RISC CPU can be used in place of a microcontroller to provide the functions of system management, user interface, and peripheral control. The vector processor is dedicated for audio-specific processing. In addition to MPEG audio decoding, it will generate 3D sound effects, and support karaoke features, such as key control and echo. The chip also provides the voice-activated ADPCM codec for voice recording and language learning through MIC input.

The ES3986 supports a variety of CD servos directly to provide the system solution of lower BOM cost and manufacturing flexibility. With its low system power consumption, the built-in antishock capabilities, and 16-Mbit DRAM support, the ES3986 is very suitable for portable audio applications.

Figure 1 shows a typical standalone system using a MP3 player, where the MP3 stream from a CD-ROM is passed to the ES3986, which parses the system layer and decodes the audio layer. The decoded MPEG audio and 3D sound enhancement is then passed to the external audio DAC.

FEATURES

- Programmable multimedia processor (PMP) architecture
- MPEG1/MPEG2 and MP3 audio decoder
- CD block decoder functions
- STC interpretation and audio phase-lock loop (PLL)
- 256/384 fs for audio system clock
- Programmable master clock for external audio DAC
- Independent bit clock for audio transmit and receive
- Power management
- 2.5V power supply with 5V-tolerant I/Os
- 3D sound and surround sound
- Karaoke function
- Vocal reverb: simulates a theater acoustic environment
- 0.3W power dissipation
- 2-Mb DRAM support
- 100-pin plastic quad flat pack (PQFP) package digital-audio processor

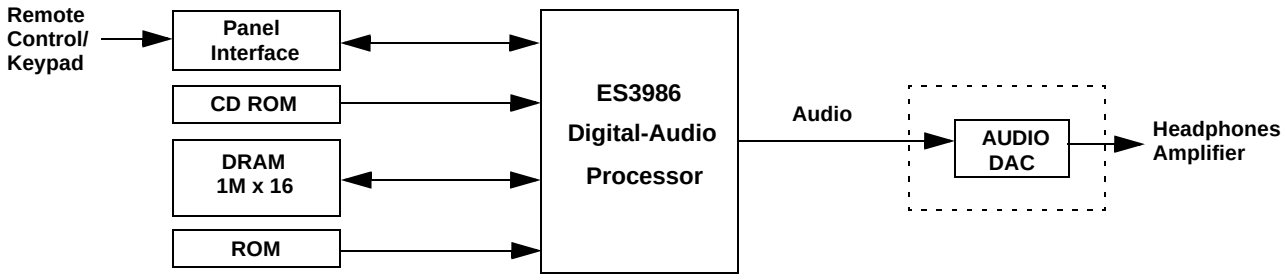

Figure 1 ES3986 VCD Processor System Block Diagram

PINOUT

The pinouts for the ES3896 are shown in Figure 2.

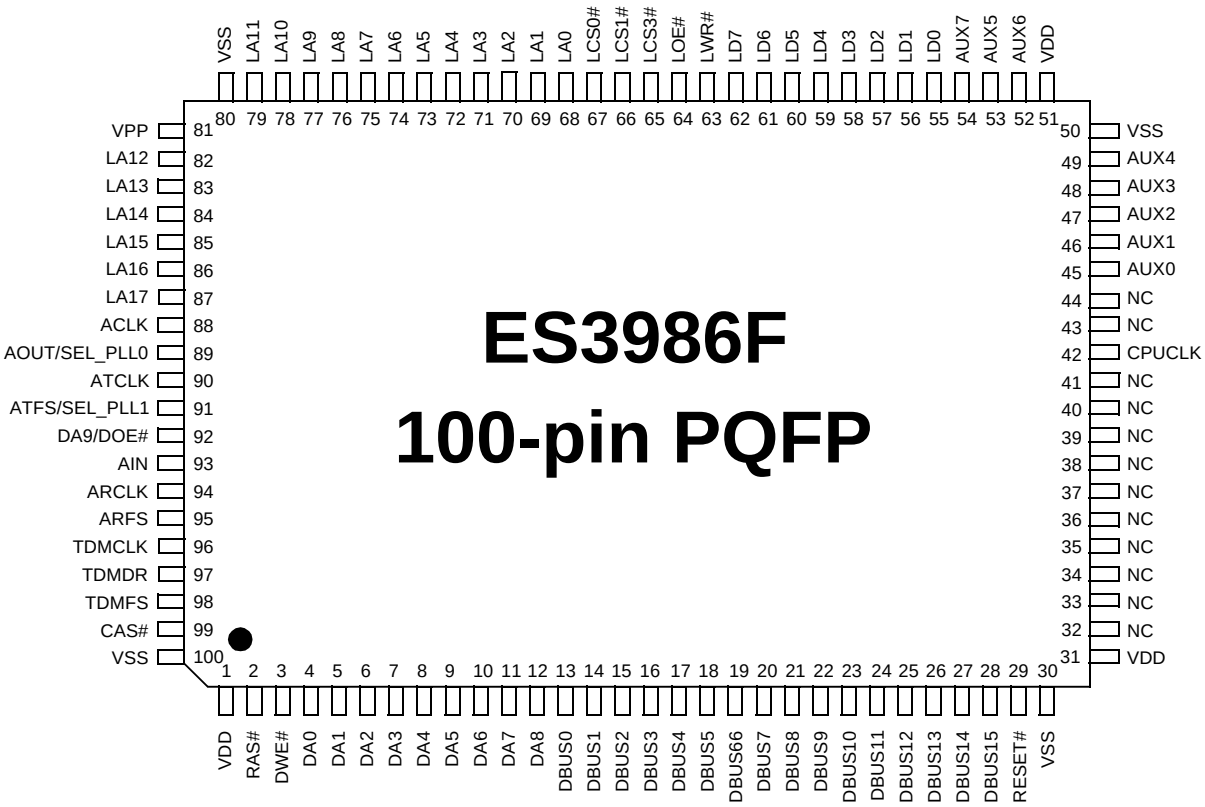

Figure 2 ES3986 Pinout Diagram

ES3986 PIN DESCRIPTIONS

The ES3986 pins are listed and described in Table 1.

Table 1 ES3896 Pin Descriptions

Names	Pin Numbers	I/O	Definitions
VDD	1, 31, 51	I	Voltage supply for 2.5V.
RAS#	2	O	DRAM row address strobe (active low).
DWE#	3	O	DRAM write enable (active low).
DA[8:0]	4:12	O	DRAM multiplexed row and column address bus.
DBUS[15:0]	13:28	I/O	DRAM data bus.
RESET#	29	I	System reset (active low).
VSS	30, 50, 80, 100	I	Ground.
NC	32:41, 43, 44	—	No Connect.
CPUCLK	42	I	RISC and system clock input. CPUCLK is used only if SEL_PLL[1:0] = 00.
AUX[7:0]	44:49, 54, 52, 53,	I/O	Auxiliary control pins (AUX0 and AUX1 are open collectors.)
LD[7:0]	55:62	I/O	RISC interface data bus.
LWR#	63	O	RISC interface write enable (active low).
LOE#	64	O	RISC interface output enable (active low).
LCS[3,1,0]#	65, 66, 67	O	RISC interface chip select (active low).
LA[17:0]	68:79, 82:87	O	RISC interface address bus.
VPP	81	I	Digital supply voltage for 5V.
ACLK	88	I/O	Master clock for external audio DAC (8.192 MHz, 11.2896 MHz, 12.288 MHz, 16.9344 MHz, and 18.432 MHz)
AOUT/ SEL_PLL0	89	O	Dual-purpose pin. AOUT is the audio interface serial data output.
		I	Pins SEL_PLL[1:0] select phase-lock loop (PLL) clock frequency CPUCLK for the ES3986: 00 = bypass PLL 01 = 54-MHz PLL 10 = 67.5-MHz PLL 11 = 81-MHz PLL.
ATCLK	90	I/O	Audio transmit bit clock.
ATFS/ SEL_PLL1	91	O	Dual-purpose pin. ATFS is the audio interface transmit frame sync.
		I	Pins SEL_PLL[1:0] select phase-lock loop clock frequency CPUCLK for the ES3986. (Refer to the SEL_PLL0 pin above for the settings.)
DA9/DOE#	92	O	Dual-purpose pin: DRAM output enable (active low)/DRAM multiplexed row and column address bus.
AIN	93	I	Audio interface serial data input.
ARCLK	94	I	Audio receive bit clock.
ARFS	95	I	Audio interface receive frame sync.
TDMCLK	96	I	TDM interface serial clock.
TDMDR	97	I	TDM interface serial data receive.
TDMFS	98	I	TDM interface frame sync.
CAS#	99	O	DRAM column address strobe bank 0 (active low).

ORDERING INFORMATION

Part Number	Description	Package
ES3986F	Digital-Audio Processor	100-pin PQFP

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