承永資訊科技
CYRUSTEK CO.

ES51966

4 3/4 and 5 3/4 A/D (Peak &Cap)

Features

- **External crystal oscillator**
  4MHz: count up to 44,000 counts
  (input range: ±440mV)
  10MHz: count up to 440,000 counts
  (input range: ±440mV)
- **Four selectable conversion rates:**
  20, 10, 5, 2 conversion/sec
- **On chip resistance switches for range Changing.**
- **Voltage (DC/AC), current(DC/AC), resistor, diode, capacitance, frequency and duty cycle measurement**
- **400mV independent input**
- **on chip OP amp' for AC/DC conversion**
- **Auto zeroing function**
- **Peak hold function with calibration mode**
- **X10 function**
- **I/O port for microprocessor**
- **Capacitance measurement**
  -4nF to 40mF, count up to 40,000 counts
  -Discharging indication
- **400MHz Frequency counter and 1MHz duty cycle measurement**
- **On chip buzzer driving: 2KHz**
- **Single 5V or 6V DC power supply (V+ to V-)**
- **Low battery detection**
- **SLEEP mode**
- **56-pin SSOP**

Description

The ES51966 is a 44,000/440,000-count dual-slope analog-to-digital converter (ADC) with X10 and PEAK Hold functions. The ES51966 also include capacitance, frequency and duty cycle measurement. The conversion rate and resolution can be selected/decided by external microprocessor. In additional, other functions are also provided for low battery detection, on chip buzzer driving, and I/O port with microprocessor.

Absolute Maximum Ratings

Characteristic	Rating
Positive Supply Voltage (V+ to AGND)	3.5V
Negative Supply Voltage (V- to AGND)	-3.5V
Analog I/O Voltage	((V-) - 0.5V) to ((V+) + 0.5V)
Digital I/O Voltage	((V-) - 0.5V) to ((V+) + 0.5V)
Power Dissipation	800mW
Operating Temperature	0°C to 70°C
Storage Temperature	-25°C to 125°C
Lead Temperature (soldering, 10sec)	270°C

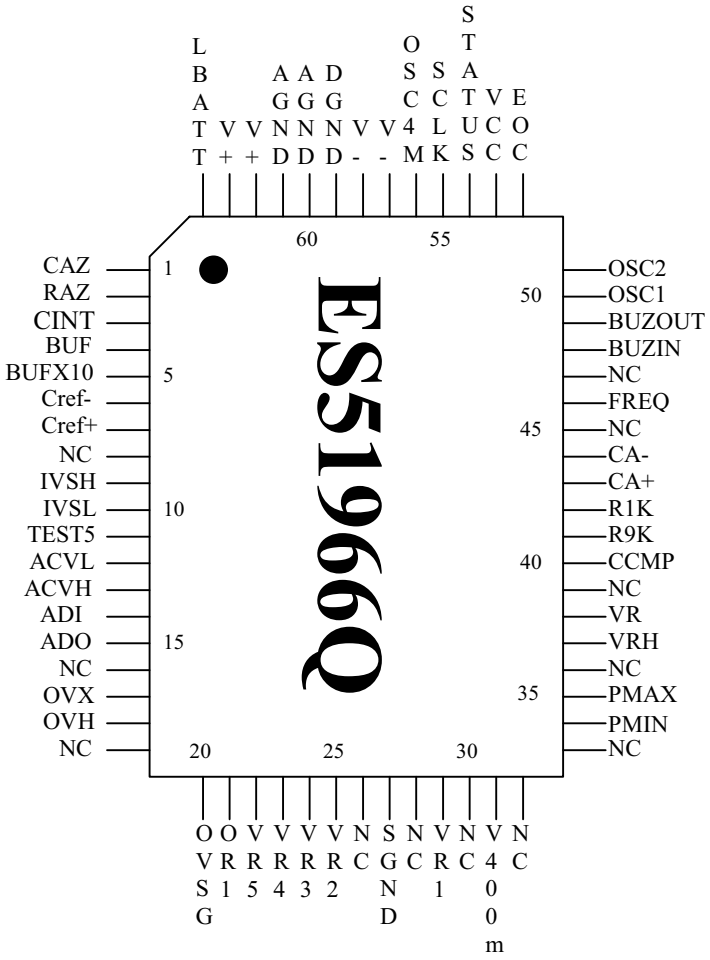
Electrical Characteristics

TA=25°C, DGND=AGND=0V

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V+	Positive Power Supply		2.3	2.5	3.3	V
V-	Negative Power Supply		-2.3	-2.5	-3.3	V
I(V+)	Operation Supply Current	Normal power on (V+ to V-)	-	1.0	1.7	mA
I(GND)	Supply Current of DGND to V-	ΔV between DGND and V- is -0.2V	5	10	-	mA
Zero	Zero Input Reading	1 MΩ input resistor, null to zero by uP.	-0	0	+0	count
NLV1	Nonlinearity (Voltage x1)	Best case straight line	-0.07	-	0.07	%F.S.
REV1	Rollover Error (Voltage x1)	1 MΩ input resistor	-0.07	-	0.07	%F.S.
NLV10	Nonlinearity (Voltage x10)	Best case straight line	-0.1	-	0.1	%F.S.
REV10	Rollover Error (Voltage x10)	1 MΩ input resistor	-0.1	-	0.1	%F.S.
V12	Band Gap Voltage Reference	100 kΩ between V12 and AGND	-1.31	-1.23	-1.10	V
LBATT	Low Battery Detection	LBATT to V12	-60	0	60	mV
	PEAK Hold value accuracy (10us)	使用 10nF 聚乙酯薄膜電容 (polyester, Mylar)	-1.2 -25	-	+1.2 +25	%F.S. ±count
TCRF	Reference Voltage (V12) Temperature Coefficient	100 kΩ between V12 and AGND (0°C to 70°C)	-	50	-	ppm/°C

Pin configuration

QFP-64pin



Pin Description

Pin No.	Symbol	Type	Description
1	CAZ	O	Auto-zero capacitor connection
2	RAZ	O	Auto-zero resistance connection
3	CINT	O	Integration capacitor connection
4	BUF	O	Integration resistor connection output
5	BUFX10	O	Integration resistor connection output
6	Cref-	I/O	Negative connection for reference capacitor
7	Cref+	I/O	Positive connection for reference capacito
9	IVSH	I	High current measurement input
10	IVSL	I	Low current measurement input
11	TEST5	I/O	Test Pin
12	ACVL	O	Negative output of AC to DC converter
13	ACVH	O	Positive output of AC to DC converter.
14	ADI	I	Negative input of internal AC to DC OpAmp
15	ADO	O	Output of internal AC to DC OpAmp.

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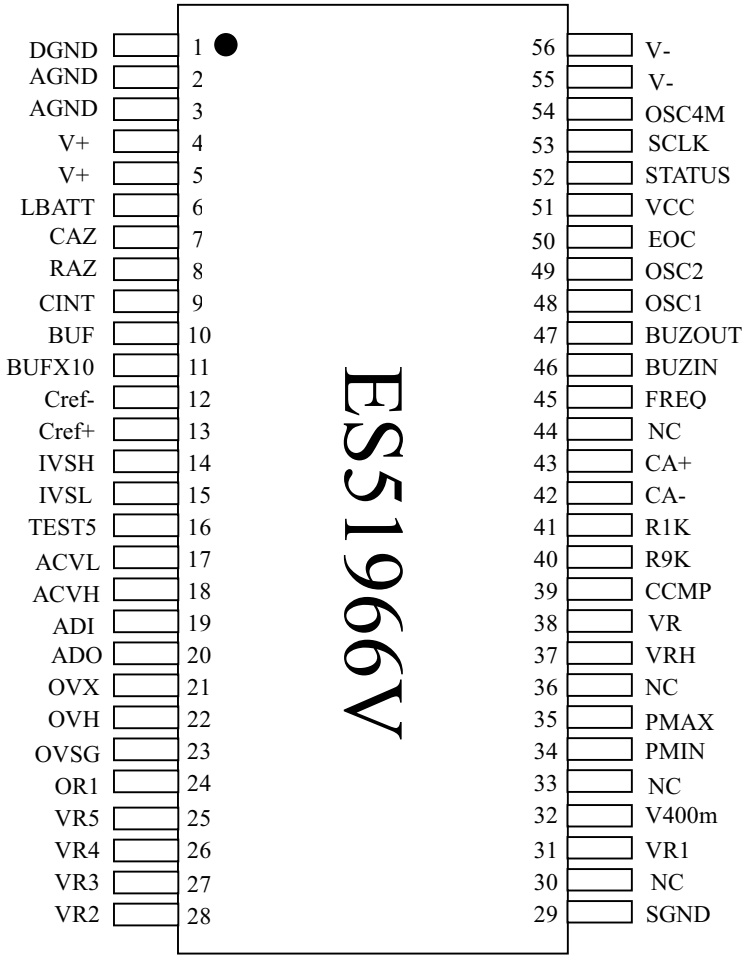
Pin No.	Symbol	Type	Description
17	OVX	I	Input high voltage for resistance measurement.
18	OVH	I	Output connection for resistance measurement.
20	OVSG	I	Sense low voltage for resistance measurement.
21	OR1	O	Reference resistor connection for 399.9Ω range.
22	VR5	O	Voltage measurement ÷ 10000 attenuator (4000V.)
23	VR4	O	Voltage measurement ÷ 1000 attenuator (400.0V.)
24	VR3	O	Voltage measurement ÷ 100 attenuator (40.00V.)
25	VR2	O	Voltage measurement ÷ 10 attenuator (4.000V.)
27	SGND	G	Signal Ground.
29	VR1	I	Measurement input.
32	V400m	I	400mV independent input.
34	PMIN	O	Minimum peak hold output.
35	PMAX	O	Maximum peak hold output.
37	VRH	O	Output of band-gap voltage reference. Typically -1.2V
38	VR	O	Reference input voltage connection. Typically -200mV
40	CCMP	I	In capacitor mode, a compensation capacitor is connected.
41	R9K	O	Connect to a 9KΩ resistor for capacitor measurement
42	R1K	O	Connect to a 1KΩ resistor for capacitor measurement.
43	CA-	I/O	Negative auto-zero capacitor connection for capacitor measurement.
44	CA+	I/O	Positive auto-zero capacitor connection for capacitor measurement.
46	FREQ	I	Frequency counter input, offset to V-/2
48	BUZIN	I	Enables the buzzer. Low action.
49	BUZOUT	O	Outputs a 2KHz audio frequency signal for driving piezoelectric buzzer when BUZIN is low.
50	OSC1	I	Crystal oscillator input connection.
51	OSC2	O	Crystal oscillator output connection.
52	EOC	O	End of conversion indicator
53	VCC	I	The high level of digital I/O signals, which is connected to VCC pin of microprocessor.
54	STATUS	I/O	ES51966 sends current status to microprocessor or receives controlled status from microprocessor.
55	SCLK	I	Clock input from microprocessor.
56	OSC4M	I	Crystal oscillator selection. NC for 4MHz; connect to V- for 10MHz.
57	V-	P	Negative supply voltage, connected to cathode of battery typically.
58	V-	P	Negative supply voltage, connected to cathode of battery typically.
59	DGND	G	Digital Ground
60	AGND	G	Analog Ground
61	AGND	G	Analog Ground
62	V+	P	Positive supply voltage, output of on-chip DC-DC converter.
63	V+	P	Positive supply voltage, output of on-chip DC-DC converter.
64	LBATT	I	Low battery voltage detection
8 , 16 , 19 , 26 , 28 , 30 , 32 , 33 , 36 , 39 , 45 , 47			No connected
P: Power, G: Ground, I: Input, O: Output			

Pin configuration

SSOP-56pin



Pin Description

Pin No.	Symbol	Type	Description
1	DGND	G	Digital Ground
2	AGND	G	Analog Ground
3	AGND	G	Analog Ground
4	V+	P	Positive supply voltage, output of on-chip DC-DC converter.
5	V+	P	Positive supply voltage, output of on-chip DC-DC converter.
6	LBATT	I	Low battery voltage detection
7	CAZ	O	Auto-zero capacitor connection.
8	RAZ	O	Auto-zero resistance connection.
9	CINT	O	Integration capacitor connection.
10	BUF	O	Integration resistor connection output.
11	BUFX10	O	Integration resistor connection output.

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Pin No.	Symbol	Type	Description
12	Cref-	I/O	Positive connection for reference capacitor.
13	Cref+	I/O	Negative connection for reference capacitor.
14	IVSH	I	High current measurement input.
15	IVSL	I	Low current measurement input.
16	TEST5	I/O	Test pin
17	ACVL	O	Negative output of AC to DC converter.
18	ACVH	O	Positive output of AC to DC converter.
19	ADI	I	Negative input of internal AC to DC OpAmp
20	ADO	O	Output of internal AC to DC OpAmp.
21	OVX	I	Input high voltage for resistance measurement.
22	OVH	I	Output connection fir resistance measurement.
23	OVSG	I	Sense low voltage for resistance measurement.
24	OR1	O	Reference resistor connection for 399.9Ω range.
25	VR5	O	Voltage measurement ÷10000 attenuator (4000V.)
26	VR4	O	Voltage measurement ÷1000 attenuator (400.0V.)
27	VR3	O	Voltage measurement ÷100 attenuator (40.00V.)
28	VR2	O	Voltage measurement ÷10 attenuator (4.000V.)
29	SGND	G	Signal Ground.
30	NC		
31	VR1	I	Measurement input.
32	V400m	I	400mV independent input.
33	NC		
34	P_{MIN}	O	Minimum peak hold output.
35	P_{MAX}	O	Maximum peak hold output.
36	NC		
37	VRH	O	Output of band-gap voltage reference. Typically –1.2V
38	VR	I	Reference input voltage connection. Typically –200mV.
39	CCMP	I	In capacitor mode, a compensation capacitor is connected.
40	R9K	O	Connect to a 9KΩ resistor for capacitor measurement.
41	R1K	O	Connect to a 1KΩ resistor for capacitor measurement.
42	CA-	I/O	Negative auto-zero capacitor connection for capacitor measurement.
43	CA+	I/O	Positive auto-zero capacitor connection for capacitor measurement.
44	NC		
45	FREQ	I	Frequency counter input, offset to V-/2
46	BUZIN	I	Enables the buzzer. Low action.
47	BUZOUT	O	Outputs a 2KHz audio frequency signal for driving piezoelectric buzzer when BUZIN is low.
48	OSC1	I	Crystal oscillator input connection.
49	OSC2	O	Crystal oscillator output connection.
50	EOC	O	End of conversion indicator
51	VCC	I	The high level of digital I/O signals, which is connected to VCC pin of microprocessor.
52	STATUS	I/O	ES51966 sends current status to microprocessor or receives controlled status from microprocessor.
53	SCLK	I	Clock input from microprocessor.
54	OSC4M	I	Crystal oscillator selection. NC for 4MHz; connect to V- for 10MHz.
55	V-	P	Negative supply voltage, connected to cathode of battery typically.
56	V-	P	Negative supply voltage, connected to cathode of battery typically.
30, 33, 36, 44			No connected.

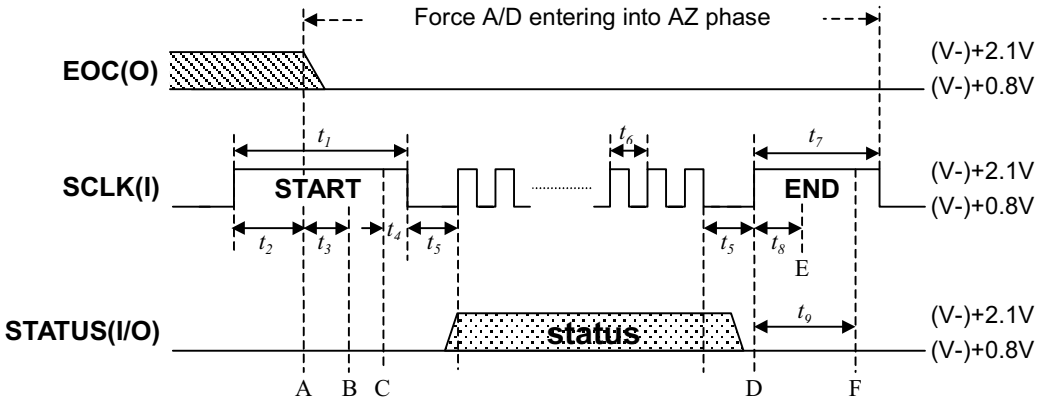
P: Power, G: Ground, I: Input, O: Output

Operation Mode

(1) Digital Interface between ES51966 and Microprocessor

The EOC, SCLK and STATUS of the ES51966 are used as digital communicating interface between ES51966 and microprocessor. The STATUS pin is bi-directional, and the others are unilateral: EOC is from ES51966 to microprocessor and SCLK is from microprocessor to ES51966. The timing and data of the communication are as follows:

mode 1: ES51966 receives controlled status from microprocessor.



Timing of the above figure: (T = 0.25μs)

t_1	(1040 ~ 4096) T	t_6	(32 ~ 512) T
t_2	512 T	t_7	(520 ~ 1020) T
t_3	(4 ~ 256) T	t_8	(0 ~ 256) T
t_4	> 4 T	t_9	520 T
t_5	(16 ~ 1024) T		

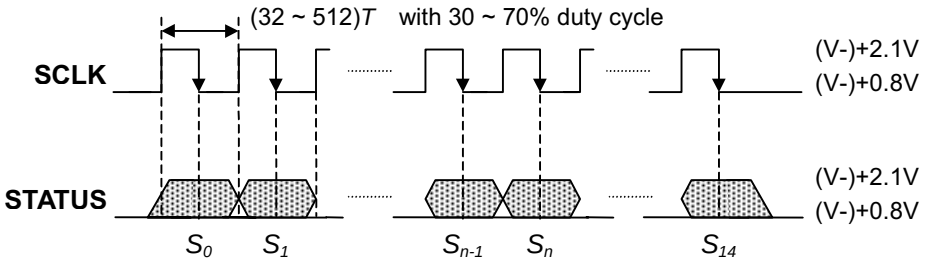
Note: 1. At START:

After time A, the EOC's state is forced to low (V-) and ES51966 enter into AZ phase. And at the same time, STATUS is changed from output pin to input pin with a 3uA pull low current provided by ES51966 internally. Then microprocessor can send control status to STATUS. It is suggested that microprocessor begins to drive STATUS between B and C.

2. At END:

The microprocessor stopped driving STATUS between D and E, and ES51966 will begin to drive STATUS after F.

3. The detail timing between SCLK and STATUS is as follow:



Serial Data Format (STATUS):

F0	F1	F2	Q0	Q1	Q2	C0	C1
0	1	2	3	4	5	6	7

C2	AC	ZERO	PEAK	PHCAL	X10	SLEEP
8	9	10	11	12	13	14

(All defaults are '0')

F0, F1, F2 measurement selection.

F0	F1	F2	Measurement
0	0	0	Voltage[2]
0	0	1	Voltage with frequency[3]
0	1	0	Current[2]
0	1	1	Current with frequency[3]
1	0	0	Resistance
1	0	1	Diode
1	1	0	Frequency and duty cycle[1]
1	1	1	Capacitance

[1] In Frequency and duty cycle measurement, ES51966 measures both the frequency and duty cycle of the input signal FREQ (pin 45) simultaneously.

[2] In Voltage/Current measurement, only voltage/current is measured.

[3] In Voltage/Current with frequency measurement, the frequency of FREQ is also measured in addition to voltage/current. Detailed descriptions of these measurement modes, please see the following sections.

Q0, Q1, Q2 range selection.

Q0	Q1	Q2	V[1]	A[1]	Ω[1]	F[2 3]	C[2]
0	0	0	440mV	IVSL (pin15)[4]	420Ω	40Hz	4nF
0	0	1	4.4V	IVSH (pin 14)[4]	4.2KΩ	400Hz	40nF
0	1	0	44V		42KΩ	4KHz	400nF
0	1	1	440V		420KΩ	40KHz	4uF
1	0	0	4400V		4.2MΩ	400KHz	40uF
1	0	1			42MΩ	4MHz	400uF
1	1	0				40MHz	4000uF
1	1	1				400MHz	40000uF

[1] When oscillator is 4MHz, voltage/current/resistance can be counted up to 44,000; When oscillator is 10MHz, voltage/current/resistance can be counted up to 440,000.

[2] Both frequency and capacitance measurement could only be counted up to 40,000 regardless the oscillator frequency.

[3] In 40Hz range, ES51966 can count from 0.5Hz to 40Hz; in 400Hz range, it can count from 2.5Hz to 400Hz; in 4000Hz, it can count from 25Hz to 4000Hz.
[4] In Current measurement, two input pins (IVSH and IVSL) are provided and can be selected by Q2.

C0, C1, C2 In voltage (F[0:2] = "000") and current ("010") measurement, C0 & C1 are used for conversion rate selection:

C0	C1	Conversion/sec	Conversion period
0	1	20	50ms
0	0	10	100ms
1	0	5	200ms
1	1	2	500ms

10, 5, and 2 conversion/sec are 50Hz rejection, while 2 conversion/sec is both of 50 Hz and 60Hz rejections.

In resistance measurement, the conversion period is:

C0	C1	Conversion period
0	1	70ms
0	0	140ms
1	0	280ms
1	1	700ms

When PEAK or PHCAL function is ON, the conversion period becomes:

C0	C1	Conversion period
0	1	55ms
0	0	110ms
1	0	220ms
1	1	550ms

In frequency and duty cycle (F[0:2] = "110") measurement, only C0 is used for conversion period selection. When the range is from 40Hz to 4000Hz, the conversion periods are not selectable (see the description in Frequency and duty cycle measurement); and when the range is from 40KHz to 400MHz, the conversion period is decided by C0:

C0	Conversion period
0	110ms
1	1.1s

In voltage/current with frequency mode (F[0:2] = "001" and "011"), the conversion period is fixed at 110ms, and C0, C1 & C2 decide the range of the frequency measurement:

C0	C1	C2	Range
0	-	-	40KHz
1	0	0	400KHz
1	0	1	4MHz
1	1	0	40MHz
1	1	1	400MHz

In capacitance measurement, these bits are no use.

AC 'L' for DC; 'H' for AC in Voltage/Current measurement. If not in voltage or current measurement, this bit will be ignored.

ZERO 'H' for zero calibration.

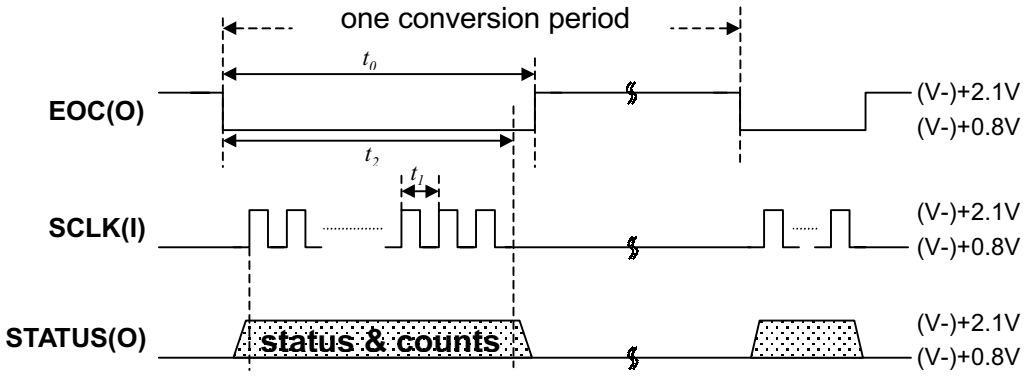
PEAK 'H' for PEAK Hold function in Voltage/Current measurement.

PHCAL 'H' for PEAK Hold calibration mode in Voltage/Current measurement.

X10 'H' for X10 function.

SLEEP 'H' for DMM in sleep mode.

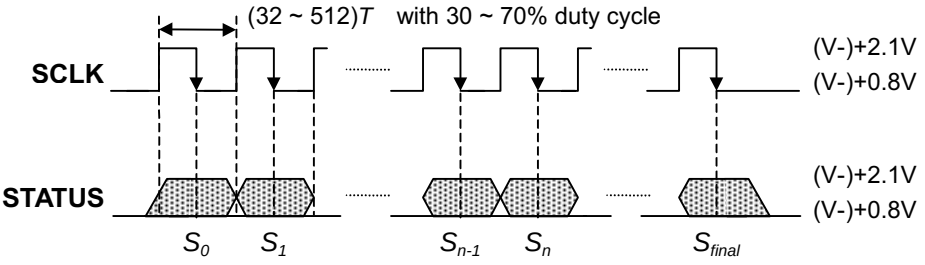
mode 2: ES51966 sends the status and counts (counter from DINT) to uP.



t_0 is at least 5ms and t_1 must be (32 ~ 512)T, where T = 0.25μs.

t_2 is the time from the falling edge of EOC to the last data been transferred. t_2 is no more than 4.9ms. That is, all results must be transferred within 4.9ms from the falling edge of EOC.

The detail timing between SCLK and STATUS is as follow:



Serial Data Format (STATUS):

- Voltage ("000"), current ("010"), resistance ("100") and diode ("101") measurement

SIGN	PMAX	BATT	D0<0:19> (20 bits)
0	1	2	3 ~ 22

SIGN 'H' for negative; 'L' for positive. In AC, Ω and diode measurement, this bit can be ignored.

PMAX When PEAK or PHCAL is executed, 'H' for PEAK MAX. measurement, 'L' for PEAK MIN. measurement.

BATT 'H' for battery-low indication.

D0<0:19> Conversion results (magnitude). The format is 2's complement. LSB outputs first. When oscillator is 4MHz, D0<0:19> is up to 44,000 counts. When oscillator is 10MHz, if the conversion rate is 20/sec, it counts to 220,000; if the conversion rate is not 20/sec, it counts to 440,000.

- Capacitance ("111") measurement:

DISCH	0	BATT	D0<0:19> (20 bits)
0	1	2	3 ~ 22

DISCH 'H' indicates that DMM is under discharging. If this bit is 'H', ES51966 enters AZ mode, and discharges the capacitor automatically. However, discharging through ES51966 is slow, and the customer had better discharge by shorting two pins of the capacitor. When DISCH is 'H', all the STATUS never outputs (EOC is never high), but the status of DISCH will be on the STATUS pin. Therefore, uP should keep an eye on the STATUS pin when capacitance measurement to know if the capacitor needs to be discharged.

0 This bit is always zero.

BATT 'H' for battery-low indication.

D0<0:19> Conversion results (magnitude). The format is 2's complement. LSB outputs first.

- Voltage/current with frequency ("001" & "010") measurement:

SIGN	PMAX	BATT	D0<0:19> (20 bits)	D1<0:17> (18 bits)
0	1	2	3 ~ 22	23 ~ 40

SIGN For voltage/current measurement. 'H' for negative; 'L' for positive. In AC, Ω and diode measurement, this bit can be ignored.

PMAX For voltage/current measurement. When PEAK or PHCAL is executed, 'H' for PEAK MAX. measurement, 'L' for PEAK MIN. measurement.

BATT 'H' for battery-low indication.

D0<0:19> Conversion result of voltage or current measurement.

D1<0:17> Conversion result of frequency measurement.

- Frequency ("110") measurement:

OL	UL	BATT	D0<0:19> (20 bits)	D1<0:17> (18 bits)	D2<0:5> (6 bits)
0	1	2	3 ~ 22	23 ~ 40	41 ~ 46

OL Overflow when in 40, 400 and 4000Hz ranges.

UL Underflow when in 40, 400 and 4000Hz ranges.

BATT 'H' for battery-low indication.

D0<0:19>, D1<0:17>, D2<0:5> Please see the description in frequency and duty cycle measurement.

(2) Dual Slope A/D—four phases timing

The ES51966's measurement cycle contains four phases, ZI, AZ, INT, and DINT. The timing will be changed as conversion rate changed. There are some examples as follow, and the others are alike.

ES51966 is a dual-slope analog-to-digital converter (ADC). Figure 2.1 is a structure of dual-slope integrator. Its measurement cycle has two distinct phases: input signal integration (INT) phase and reference voltage integration (DINT) phase.

In INT phase, the input signal is integrated for a fixed time period, then A/D enters DINT phase in which an opposite polarity constant reference voltage is integrated until the integrator output voltage becomes to zero. Since both the time for input signal integration and the reference voltage are fixed, the de-integration time is proportional to the input signal. Hence, we can define the mathematical equation about input signal, reference voltage integration (see Figure 2.1):

$$\frac{1}{Buf \times C\,\text{int}} \int_0^{T_{INT}} V_{IN}(t)dt = \frac{1}{Buf \times C\,\text{int}} \times V_{REF} \times T_{DINT}$$

where, $V_{IN}(t)$ = input signal

V_{REF} = reference voltage

T_{INT} = integration time (fixed)

T_{DINT} = de-integration time (proportional to $V_{IN}(t)$)

If $V_{IN}(t)$ is a constant, we can rewrite above equation:

$$T_{DINT} = \frac{T_{INT}}{V_{REF}} \times V_{IN}$$

Besides the INT phase and DINT phase, ES51966 exploits auto zero (AZ) phase and zero integration (ZI) phase to achieve accurate measurement. In AZ phase, the system offset is stored. The offset error will be eliminated in DINT phase. Thus a higher accuracy could be obtained. In ZI phase, the internal status will be recovered quickly to that of zero input.

Thus the succeeding measurements won't be disturbed by current measurement especially in case of overload.

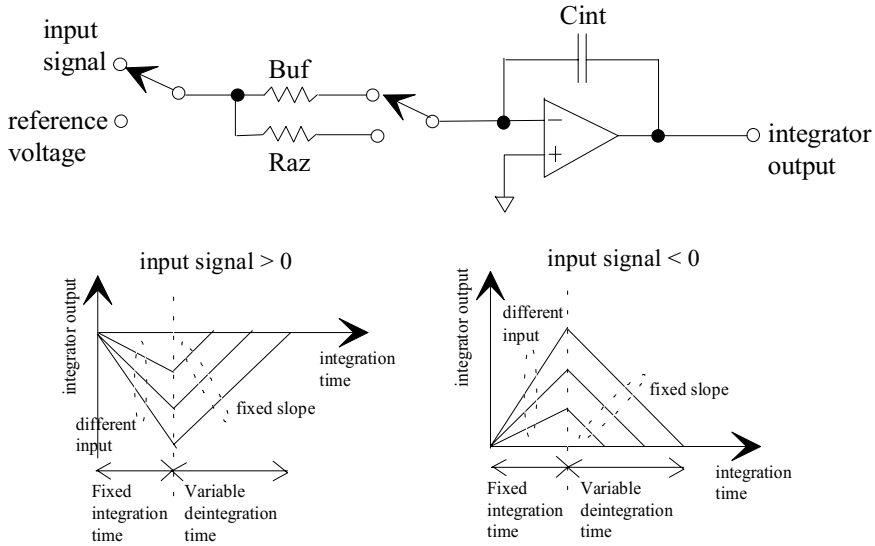


Figure 2.1 the structure of dual-slope integrator and its output waveform.

As mentioned above, the measurement cycle of ES51966 contains four phases:

(1) auto zero phase (AZ)

(2) input signal integration phase (INT)

(3) reference voltage integration phase (DINT)

(4) zero integration phase (ZI)

Normally, the time ratios of these four phases, AZ, INT, DINT and ZI to the entire measurement cycle are 20%, 20%, 44% and 16% respectively. However the actual duration of each phase depends on conversion rate. The time of each conversion rate are shown in the table below in which voltage/current (without PEAK HOLD or frequency), and diode measurement use this conversion time.

C[0:1]	CR (times/sec)	ZI (ms)	AZ (ms)	INT (ms)	DINT (ms)
01	20	8	10	10	22
00	**10**	**16**	**20**	**20**	**44**
10	5	32	40	40	88
11	2	80	100	100	220

Note: Vref = -200 mV.

(3) Component Value Selection for ADC

For various application requirements on conversion rate and input full range, we suggest nominal values for external components of ADC in Figure 2.1 to obtain better performance. Under default condition with operating clock = 4 MHz:

(1) conversion rate = 10 times/sec

(2) reference voltage = -200 mV

(3) input signal full scale = 440 mV (sensitivity = 10 uV)

we suggest that Cint = 33 nF, Buf = 200 kΩ, Raz = 200 kΩ.

If a user selects a different conversion rate rather than default, the integration capacitor Cint value must be changed according to the following rule for better performance:

Cint × (conversion rate) = (33 nF) × (10 times/sec).

It is important that the actual Cint value should be no less than the nominal value. A smaller Cint reduces the input full range. However a larger Cint might have weaker noise immunity than the suggested one.

A user could enlarge the input full range by changing reference voltage (Vref) and the amount of integration resistor (Buf and Raz). For example, if Vref, Buf and Raz are enlarged as twice than the default values then the input full range becomes 880 mV. The input full range can be enlarged up to 1.1V (2.5 times than the default case). We list general rules in below which might be helpful in determining component values.

Buf / (reference voltage) = 200 kΩ / (-200 mV)

(4) Voltage Measurement

DC/AC voltage measurement

A re-configurable voltage divider provides a suitable full-scale range voltage measurement mode. The following table summarizes the full-scale ranges in each configuration.

Configuration	Full Scale Range	Divider Ratio	Resister Connection
VR1	440.00mV	1	-
VR2	4.4000V	1/10	R2 / (R1+R2)
VR3	44.000V	1/100	R3 / (R1+R3)
VR3	440.00V	1/1000	R4 / (R1+R4)
VR5	4400.0V	1/10000	R5 / (R1+R5)

In configuration VR1, the full range is 440mV, and the voltage inputs from V400m pin to prevent the influence of noise when floating. In other configurations, the voltage inputs from VR1 pin.

Pin 19 to 23 are used for AC measurement. Figure 4.1 is the AC-to-DC circuit. AC-

to-DC circuit extracts the AC part of the voltage (ADO - TEST5). ADC then converts the voltage of (ACVH – ACVL) to acquire the AC value of input voltage. Variable resistor 5KΩ is used to adjust the DC offset. Light shielding for diode D1 and D2 is required to prevent leakage current. This circuit works properly only when the input voltage is sinusoidal. If the input is not sinusoidal (e.g., square waves), a true RMS-to-DC converter chip will be needed to obtain the correct true RMS value of input signal.

If ADO and ADI short directly, ADI is the divided voltage of the input signal. Therefore, it can be used for oscillator display.

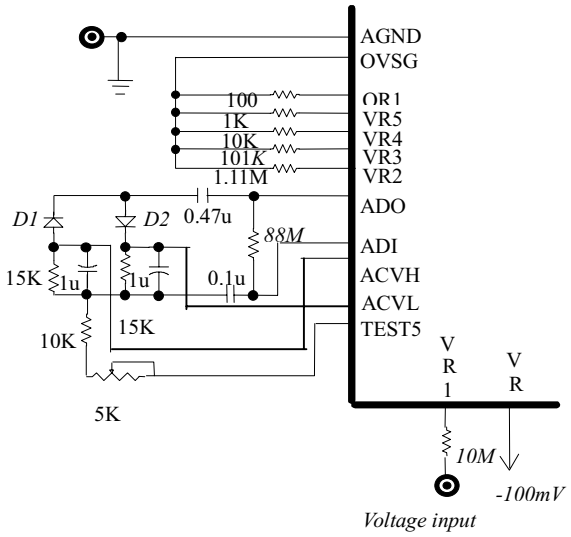


Figure 4.1 AC-to-DC circuit

The measurement of true RMS using ES636

If ES636 is used for true RMS measurement, the suggested application circuit is shown in Figure 4.2. When ES636 is used for true RMS, ADO and ADI pin short together, TEST5 pin keeps floating, and ACVL pin connects to SGND.

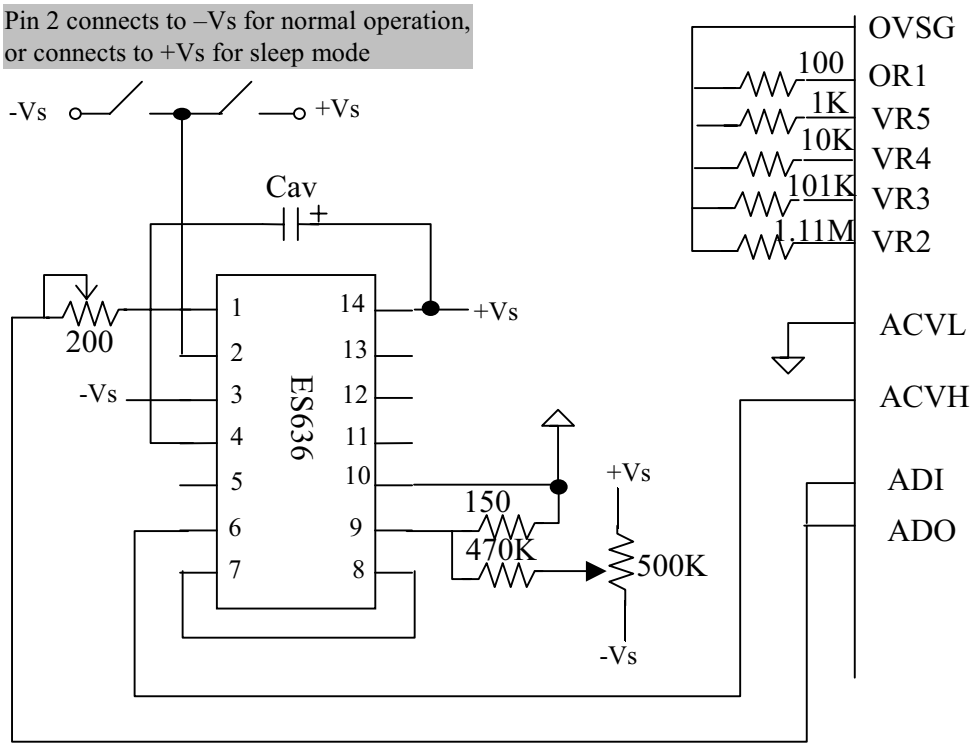


Figure 4.2 AC-to-DC circuit using ES636

(5) Diode Measurement

Diode measuement mode shares the same configuration with 4.4000V voltage mode. The range select bits Q0, Q1 and Q2 are not active in this mode.

(6) Current measurement

Current measurement has three mode. The following table summarizes the full scale range of each mode.

Mode	Range Selection	Full scale
uA	IVSL / IVSH	440.00uA / 4400.0uA
mA	IVSL / IVSH	44.000mA / 440.00mA
10A	IVSH	44.000A

*Operation Mode is based on application circuit .

*Range selection : IVSL (Q0,Q1,Q2) = (0,0,0)

IVSH (Q0,Q1,Q2) = (0,0,1)

(7) Multiplying by 10 (X10) Function

ES51966 includes X10 function. In X10 function mode, the output will be increasing tenfold. But the input range will be reduced to ±44mV. For example, if X10 function is enabled and the input is 10mV, output will be 10,000 counts, rather than 1,000 counts. To achieve X10 function, the integration resistor is 20KΩ, not 200KΩ at INT phase, and remains 200 kΩ at DINT phase. Because the resistor (20KΩ) requires exactly 1/10 of

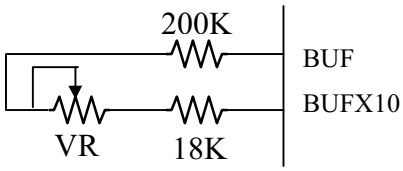


Figure 5.1 X10 function

integration resistor (200KΩ), a variable resistor VR is used to compensate these two resisters.

Resistor scheme of AZ/INT/DINT phases

In ES51966, an on-chip resistor is used for AZ mode. The internal chip is about 10 kΩ. The connection is shown in the following Figure 5.2.

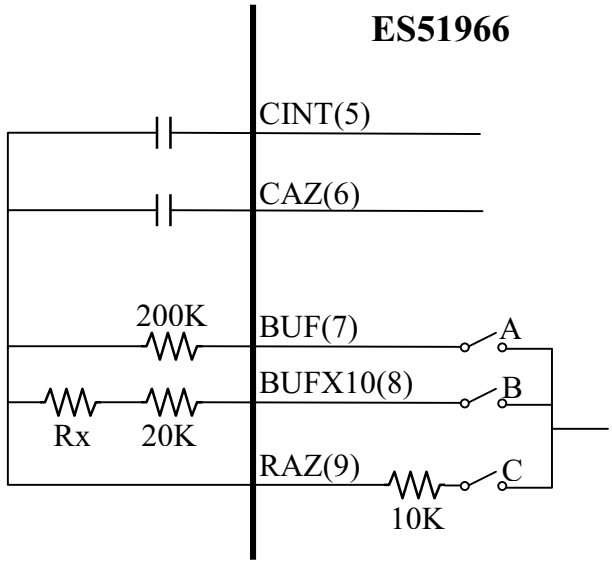


Figure 5.2 Resistor scheme of AZ phase

The status of switches A, B and C are described in the following table.

switch	X10 function is OFF			X10 function is ON		
	INT phase	DINT phase	AZ phase	INT phase	DINT phase	AZ phase
A	ON	ON	ON	OFF	ON	ON
B	OFF	OFF	ON	ON	OFF	ON
C	OFF	OFF	ON	OFF	OFF	ON

In AZ phase, all the switches is ON, the effective resistor is all the resistors in parallel. The effective resistor is therefore less than 10 kΩ. If X10 function is never used, the matching between 200 kΩ and (VR + 18 kΩ) is not necessary. In this situation, (VR + 18 kΩ) can be replaced by a resistor about 20 kΩ, or simply omitted.

(8) ZERO Calibration

In ES51966, the inherent delay of the OPAMP will introduce a few counts to the output. The method to prevent this problem is zero calibration. When zero calibration is ON, ES51966 shorts the input to SGND internally. uP needs to save the results of zero input. After zero calibration is OFF, the result of zero input is then deduct from the counts of the following measurements.

Zero calibration can be enabled on any measurement. When the ZERO bit is set by uP, ES51966 begins to execute zero calibration. ES51966 stops executing zero calibration until the ZERO bit is reset by uP.

In voltage/current/diode/capacitance measurement, the de-integration voltage is fixed, therefore zero calibration needs only be enabled once. The results could be used for all the following voltage/current/diode/capacitance measurement. However, in resistance measurement, the de-integration voltage is not fixed, and varies with the resistance to be measured. That is, zero calibration must be re-done if the resistance to be measured changes. For convenience, the result of zero input in voltage measurement could be used in resistance measurement.

(9) PEAK Hold Function

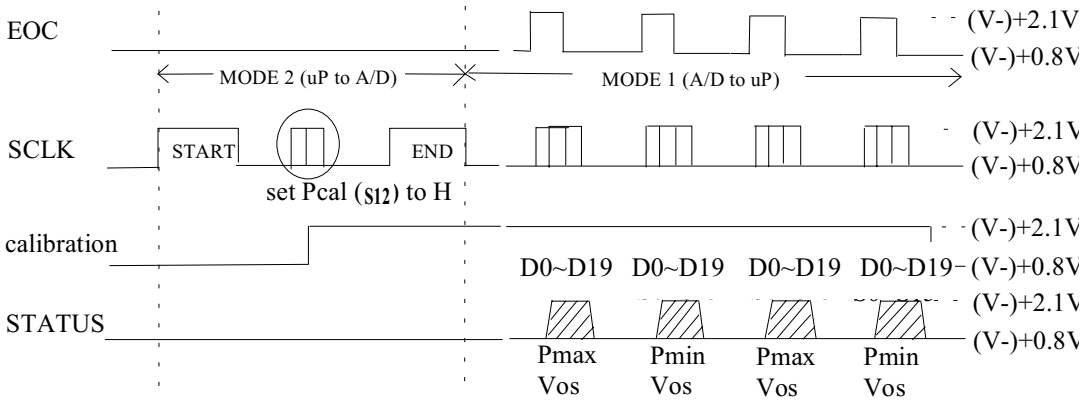
Only when voltage and current measurement (F[0:2] = “000” to “011”) could the PEAK HOLD function be executed. In PEAK HOLD measurement, the instant maximum and minimum values of the input voltage (or current) are stored and transferred to digital data through ADC. Pmax and Pmin are measured alternately while Pmax first. PEAK HOLD calibration measures the offset voltages (Vos) of Pmax and Pmin alternately and the ES51966 will count them to digital data. Then ES51966 sends the counts to microprocessor, and microprocessor must record them.

Because of existence of the offset voltage, the DINT time of voltage measurement with PEAK HOLD requires longer than that of voltage measurement without PEAK HOLD. The time of each phase when PEAK HOLD is executed at various conversion rate are as follow:

C[0:1]	ZI (ms)	AZ (ms)	INT (ms)	DINT (ms)	Total time (ms)
01	8	10	10	27	55
00	**16**	**20**	**20**	**54**	**110**
10	32	40	40	108	220
11	80	100	100	270	550

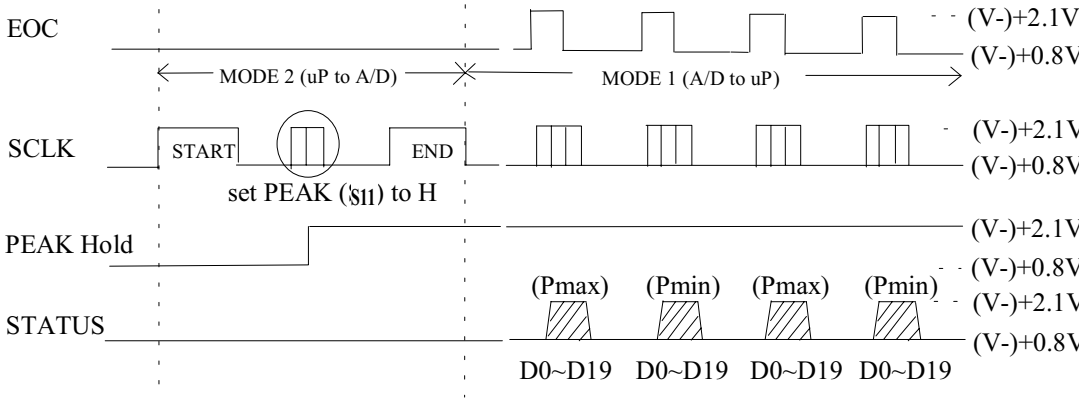
If zero and peak functions are set to ON at the same time by uP, peak function will be disabled by zero function. If peak function is set to ON at non-voltage/current measurement, it will also be disabled.

PEAK Hold calibration:

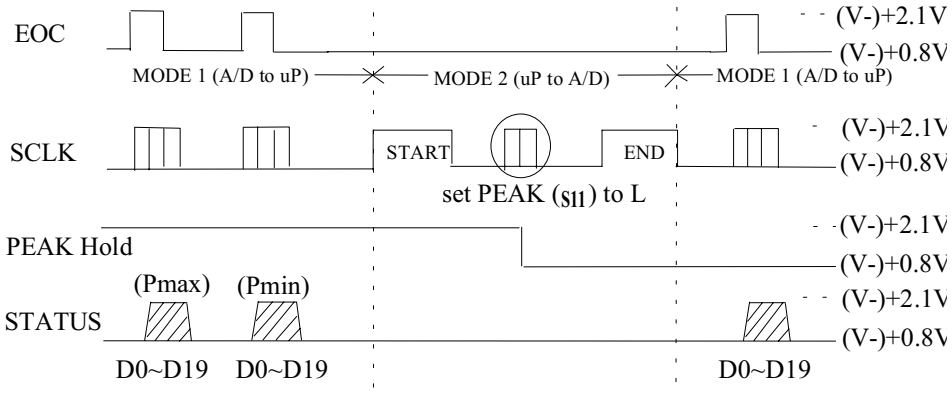


Note: it is not necessary to set PEAK to H at the same time.

To active PEAK Hold after calibration:



To cancel PEAK Hold function:



Note: After changing X10 mode, if we want to active PEAK Hold function, we must active calibration again.

(10)Frequency and duty cycle

When F[0:2] = "110", ES51966 calculates frequency and duty cycle of FREQ at the same time. However, some more computations are required to obtain both the results. There are three output data at this measurement: D0, D1, and D2 which can be obtained from the serial output.

▪ 40Hz range:

$$\text{Frequency} = \frac{(D2+1)\times 10^6}{5\times(150{,}950+D1)} \quad , \quad \text{Duty cycle} = \frac{100\times D0}{150950+D1}\%$$

▪ 400Hz range

$$\text{Frequency} = \frac{(D2+1)\times 10^6}{150{,}950+D1} \quad , \quad \text{Duty cycle} = \frac{100\times D0}{150{,}950+D1}\%$$

▪ 4000Hz range

$$\text{Frequency} = \frac{(D2+1)\times 10^7}{150{,}950+D1} \quad , \quad \text{Duty cycle} = \frac{100\times D0}{150{,}950+D1}\%$$

▪ 40KHz to 400MHz range (D2 is not needed.)

when C[0] = 0

$$\text{Frequency} = 10\times D1 \quad , \quad \text{Duty cycle} = \frac{D0}{200}\%$$

when C[0] = 1

$$\text{Frequency} = D1 \quad , \quad \text{Duty cycle} = \frac{D0}{200}\%$$

ES51966 can measure frequency from 0.5Hz to 409.6MHz. For each range, the measurable frequencies and resolution are shown in the following table:

Range	Measured frequency range	Resolutions
40Hz	0.5Hz ~ 40Hz	0.001Hz
400Hz	2.5Hz ~ 400Hz	0.01Hz
4000Hz	25Hz ~ 4000Hz	0.1Hz
40KHz	0 ~ 40.96KHz	1Hz
400KHz	0 ~ 409.6KHz	10Hz
4MHz	0 ~ 4.096MHz	100Hz
40MHz	0 ~ 40.96MHz	1KHz
400MHz	0 ~ 409.6MHz	10KHz

At 40/400/4000Hz, if the input frequency is less than its measurable range, it's underflow, and UL will set to 'H'. At the same ranges, if the input frequency is greater than its measurable range, it's overflow, and OL will set to 'H'. When UL or OL occur, the data D0, D1, and D2 will not be correct, please ignore them. At 40KHz ~ 400MHz ranges, OL and UL are always 'L', but it's overflow when the output counts is 40,960.

At different range, the conversion time is different. At 40/400/4000Hz, the conversion time is according to the input frequency. At other ranges, the conversion time is fixed at 110ms or 1.1s with C[0] = 0 or 1, respectively.

Range	Conversion time	
	C[0] = 0	C[0] = 1
40Hz	0.8s ~ 2s	
400Hz	0.16s ~ 0.4s	
4000Hz	0.16s ~ 0.4s	
40KHz	110ms	1.1s
400KHz	110ms	1.1s
4MHz	110ms	1.1s
40MHz	110ms	1.1s
400MHz	110ms	1.1s

(11)Voltage/Current Measurement with Frequency Counter

When F[0:2] = "001" or "011", ES51966 measures frequency of input together with voltage/current. At this measurement mode, voltage (or current) input is VR1/400mV (or IVSH/IVSL), and frequency input is FREQ. Q[0:2] is the range of voltage/current measurement, and C[0:2] is the range of frequency measurement. Only 40K to 400MHz ranges are selectable here. Unlike frequency measurement (F[0:2] = "110"), duty cycle is not measured in this mode. The conversion time is fixed at 110ms. Voltage/current can count up to 54,000 (or 540,000 when 10MHz OSC is used). AC and PEAK can still be active. D0 is the output of voltage/current, and (10×D1) is the result of frequency.

(12) Capacitance Measurement

ES51966 measures capacitance with 8 ranges. Capacitance can only be counted to about 40,000 counts, no matter the oscillator frequency. The conversion time, measurement range and resolution are as the following table.

Range	Conversion time	Measured frequency range	Resolutions
4nF	0.7sec	4.2000nF	0.1pF
40nF	0.7sec	42.000nF	1pF
400nF	0.7sec	420.00nF	10pF
4uF	0.7sec	4.2000uF	100pF
40uF	0.75sec	40.000uF	1nF
400uF	1.5sec	400.00uF	10nF
4000uF	3.75sec	4000.0uF	100nF
40000uF	7.5sec	40000uF	1uF

If needed, ES51966 can discharge the capacitor automatically before measuring until this chip can guarantee that it can obtain proper values in next two measurements. However, discharging by chip is slow, especially when capacitor is large or there is high voltage on the capacitor. This is because ES51966 must discharge the capacitor through the PTC resistor (about 1.5KΩ) for safety consideration. Therefore, it is strongly suggested that the user discharges the capacitor by himself when needed. If discharging occurs, the STATUS pin is pulled high immediately, and uP can check the STATUS to know if ES51966 is in discharging.

The application circuit of capacitance measurement is as Figure 10.1, the 9KΩ and 1KΩ resistors connected to R9K and R1K pins should be precision resistors.

Because there exists parasitic capacitor in the chip and the PCB board (about 200 ~300pF), compensation is required to prevent offset error at lower ranges (4n ~ 400nF ranges). There are two methods to compensate the effect of the parasitic capacitors. One method is to measure the parasitic capacitors directly by opening the input (i.e., the input capacitance is zero) and record this value for EACH RANGE (especially 4nF/40nF/400nF), and then subtracting the value of that range after each measurement. Another method is to connect a compensation capacitor C_{CMP} on the CCMP pin as the

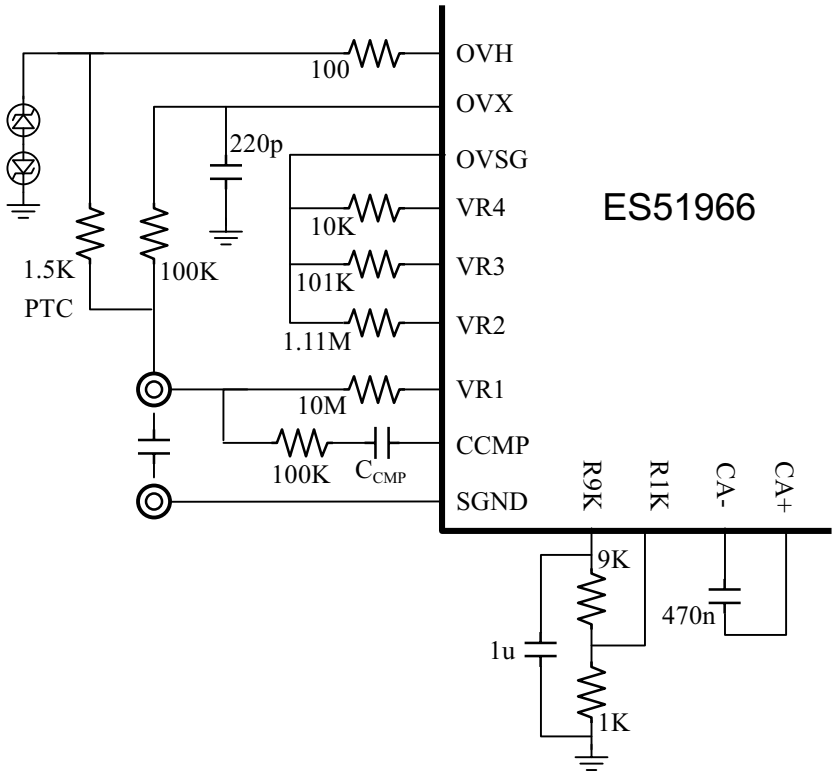


Figure 10.1 Application circuit of capacitance measurement

figure above, and then ES51966 will execute the compensation automatically. The value of C_{CMP} relates to the parasitic capacitor. The adequate value of CCMP is to let the display digits show about tens counts when input opens.

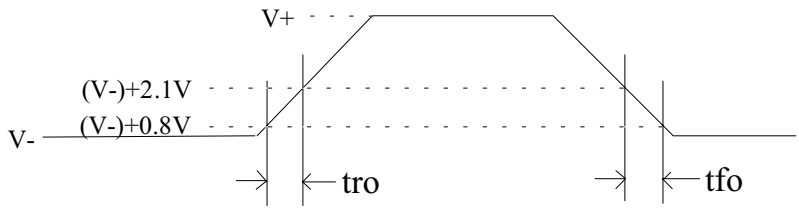
(13) SLEEP mode

If SLEEP bit is set 'H' by uP, ES51966 enters sleep mode. In sleep mode, if SCLK keeps low, all the circuit is shut down, and the supply current is about 0.1uA. If SCLK is high in sleep mode, only the oscillator is active to prepare for the following re-power operation.

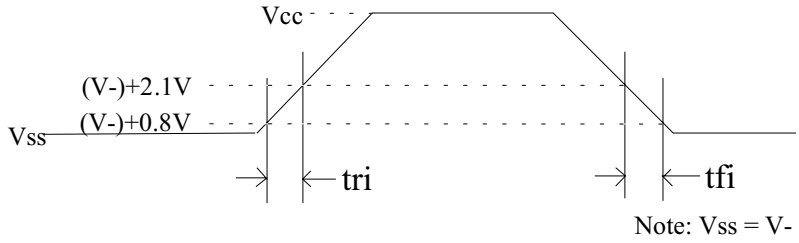
(14) Digital Signals Rising and Falling times

The digital signals include EOC, SCLK, and STATUS, and those rising and falling times are defined as follow:

EOC and STATUS are output to microprocessor:



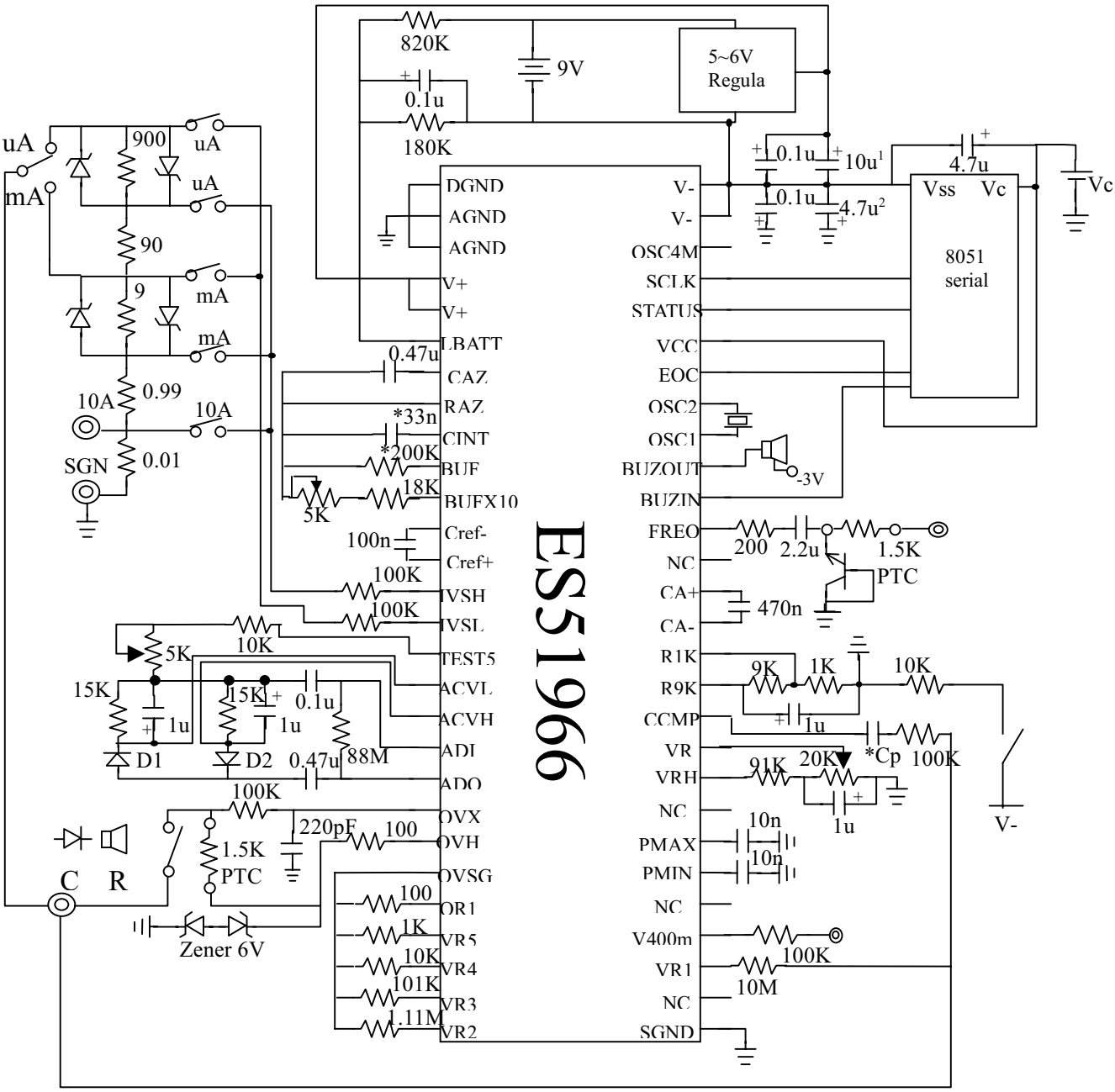
SCLK and STATUS are input from microprocessor:



Note: Vss = V-

Symbol	Condition	Min	Max	Units
tro	A/D to uP	-	20	ns
tfo	A/D to uP	-	20	ns
tri	uP to A/D	-	20	ns
tfi	uP to A/D	-	20	ns

Application Circuit



Note:

1.SCLK STATUS EOC 訊號線 Peak mode 時,需加 shielding，否則 4V 檔 couple 的 noise 很大

2.a.電容檔 COM 與 V-間需加 10K 電阻以 bypass 流至 COM 之電流

b 電容檔時 Cint 需加最大至 220nF 或者把 Rint 加大至 1MΩ，否則小電容檔 full scale 會不夠。

3.BufX10 所接的 VR 必須調整使得 $R_{buff} = 10\ R_{buffX10}$，若不匹配則在 X10 mode 下會造成額外的誤差。($R_{buffX10} = 18K\Omega + VR$, $R_{buff} = 200K\Omega$)

4.若交流電路部份照上圖應用電路(pin16 ~ pin20)接法，在 AC 檔時會多出負號，請在 uP 軟體部份自動將負號扣除即可，勿將二極體極性反接。

5.補償電容 Cp (pin CCMP)是用於小電容檔時補償電路板之寄生電容所用，在 4nF 檔時輸入端空接會有一個不歸零值，此值即爲所須接的補償電容值。

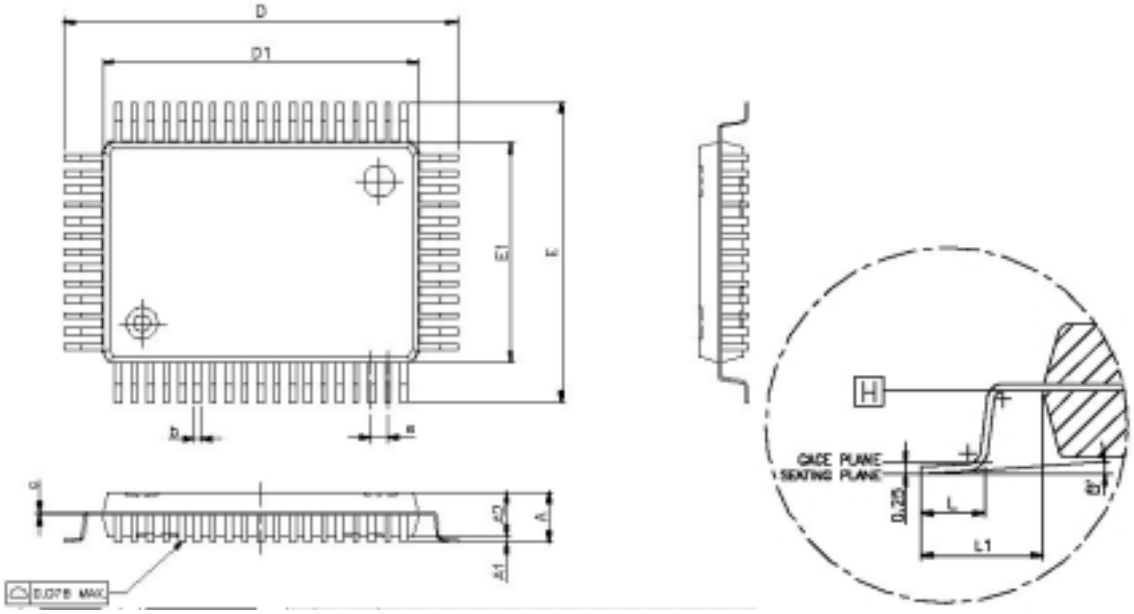
*:In capacitance mode, change 33nF to 220nF or change 200KΩ to 1MΩ.

1.Tantalum capacitor

2.Tantalum capacitor

Package

64 pins QFP package size



SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.40
A1	0.25	–	–
A2	2.55	2.72	3.05
b	0.35	0.40	0.50
c	0.11	0.15	0.23
D	25.00 BASIC		
D1	20.00 BASIC		
e	1.00 BASIC		
E	19.00 BASIC		
E1	14.00 BASIC		
L	1.15	1.30	1.45
L1	2.50 REF		
θ°	0	3.5	7

UNIT : mm

NOTES:

1.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .