GLT44108

512K X 8 CMOS DYNAMIC RAM WITH FAST PAGE MODE

Preliminary Aug 1999 (Rev.2.1)

Features :

- 524,288 words by 8 bits organization.
- Fast access time and cycle time.
- Low power dissipation.
  Operating Current-150mA max.
  TTL Standby Current-2mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh, Hidden Refresh and Test Mode Capability.
- 1024 refresh cycles/16ms.
- Available in 28pin 400 mil SOJ
- Single +5.0V±10% Power Supply.
- All inputs and Outputs are TTL-compatible.
- Fast Page Mode supports sustained data rates up to 50MHZ.

Description :

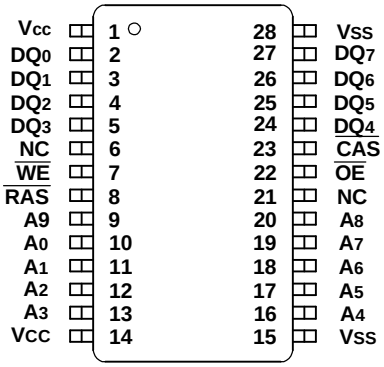
The GLT44108 is a 524,288 x 8 bit high-performance CMOS dynamic random access memory. The GLT44108 offers Fast Page mode with asymmetric address and accepts 512-cycle refresh in 8ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 8 bits within a page, with cycle times as short as 22ns.

The GLT44108 is best suited for graphics, digital signal processing and high performance peripherals.

PIN CONFIGURATION :

GLT44108
28 Lead SOJ



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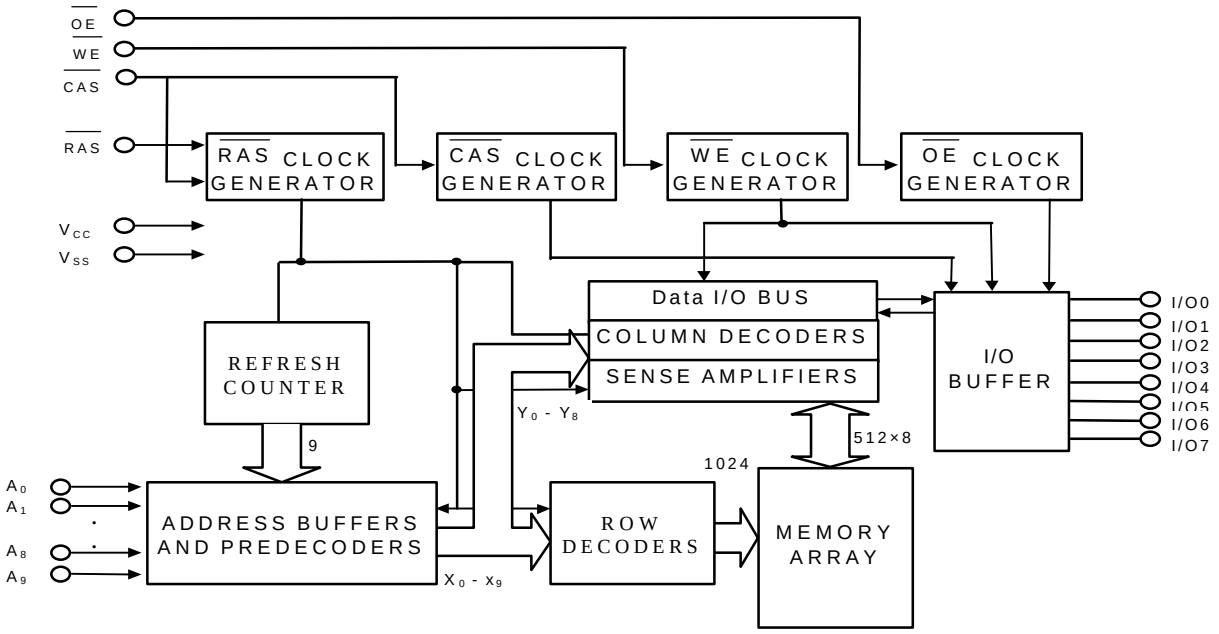
HIGH PERFORMANCE	-40	-50	-60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	40 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{AA})	20 ns	25 ns	30 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	22 ns	31 ns	40 ns
Min. Read/Write Cycle Time, (t_{RC})	75 ns	90 ns	110 ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	12 ns	13 ns	15 ns

Pin Descriptions:

Name	Function
$A_0 – A_9$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
DQ_0 - DQ_7	Data Inputs / Outputs
V_{CC}	+5V Power Supply
V_{SS}	Ground

Block Diagram:



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Absolute Maximum Ratings*

Operating Temperature, T_A (ambient)
.....-10°C to +80°C
Storage Temperature(plastic)....-55°C to +150°C
Voltage Relative to V_{SS}.....-1.0V to + 7.0V
Short Circuit Output Current.....50mA
Power Dissipation.....1.0W

*Note:Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

T_A=25°C, V_{CC}=5V±10%, V_{SS}=0V

Symbol	Parameter	Max.	Unit
C_{IN1}	Address Input	5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	7	pF
C_{OUT}	Data Input/Output	7	pF

*Note: Capacitance is sampled and not 100% tested

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 200μs and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

DC and Operating Characteristics (1-2)

TA = 0°C to 70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise specified.

Sym.	Parameter	Test Conditions	Access Time	Min.	Typ	Max.	Unit	Notes
I_{LI}	Input Leakage Current (any input pin)	0V ≤ V_{IN} ≤ 5.5V (All other pins not under test=0V)		-10		+10	µA	
I_{LO}	Output Leakage Current (for High-Z State)	0V ≤ V_{out} ≤ 5.5V Output is disabled (Hiz)		-10		+10	µA	
I_{CC1}	Operating Current, Random READ/WRITE	t_{RC} = t_{RC} (min.)	t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			150 140 120	mA	1,2
I_{CC2}	Standby Current,(TTL)	$\overline{RAS}$, $\overline{CAS}$, at V_{IH} other inputs ≥ V_{SS}				2	mA	
I_{CC3}	Refresh Current, $\overline{RAS}$ -Only	$\overline{RAS}$ cycling, $\overline{CAS}$ at V_{IH} t_{RC} = t_{RC} (min.)	t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			150 140 120	mA	2
I_{CC4}	Operating Current, FAST Page Mode	$\overline{RAS}$ at V_{IL}, $\overline{CAS}$,address cycling:t_{PC}=t_{PC}(min.)	t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			150 140 120	mA	1,2
I_{CC5}	Refresh Current, $\overline{CAS}$ Before $\overline{RAS}$	$\overline{RAS}$, $\overline{CAS}$, address cycling: t_{RC}=t_{RC}(min.)	t_{RAC} = 40ns t_{RAC} = 50ns t_{RAC} = 60ns			150 140 120	mA	1
I_{CC6}	Standby Current, (CMOS)	$\overline{RAS}$ ≥ V_{CC}-0.2V, $\overline{CAS}$ ≥ V_{CC}-0.2V, All other inputs ≥V_{SS}				1	mA	
V_{IL}	Input Low Voltage			-1		+0.8	V	3
V_{IH}	Input High Voltage			2.4		V_{CC}+1	V	3
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA				0.4	V	
V_{OH}	Output High Voltage	I_{OH} = -5mA		2.4			V	

Notes:

1.I_{CC} is dependent on output loading when the device output is selected. Specified $I_{CC(max.)}$ is measured with the output open.

2.I_{CC} is dependent upon the number of address transitions specified. $I_{CC(max.)}$ is measured with a maximum of one transition per address cycle in random Read/Write and Fast Page Mode.

3. Specified $V_{IL(min.)}$ is steady state operation. During transitions, $V_{IL(min.)}$ may undershoot to -1.0V for a period not to exceed 20ns.All AC parameters are measured with $V_{IL(min.)}$≥V_{ss} and $V_{IH(max.)}$≤V_{cc}.

AC Characteristics ($0^{\circ}C \le T_A \le 70^{\circ}C$, See note 1,2)

Test condition: V_{CC}=5.0V±10%, V_{IH}/V_{IL}=2.4V/0.8V, V_{OH}/V_{OL}=2.0V/0.8V

Parameter	Symbol	40 ns		50 ns		60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read/Write Cycle Time	t_{RC}	75	-	90	-	110	-	ns	
Read Midify Write Cycle Time	t_{RWC}	120	-	140	-	160	-	ns	
Access Time from $\overline{RAS}$	t_{RAC}	-	40	-	50	-	60	ns	3,4
Access Time from $\overline{CAS}$	t_{CAC}	-	12	-	13	-	15	ns	3,4
Access Time from Column Address	t_{AA}	-	20	-	25	-	30	ns	3,4
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0	-	0	-	0	-	ns	3
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFF}	0	8	0	10	0	13	ns	7
Transition Time(Rise and Fall)	t_T	3	50	3	50	3	50	ns	2
$\overline{RAS}$ Precharge Time	t_{RP}	25	-	30	-	40	-	ns	
$\overline{RAS}$ Pulse Width	t_{RAS}	40	10000	50	10000	60	10000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	12	-	13	-	15	-	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	40	-	50	-	60	-	ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	12	10000	13	10000	15	10000	ns	
$\overline{RAS}$ to CAS Delay Time	t_{RCD}	16	30	18	37	20	45	ns	4
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	11	22	13	25	15	30	ns	4
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	-	5	-	5	-	ns	8
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	6	-	8	-	10	-	ns	
Column Address Setup Time	t_{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	6	-	8	-	10	-	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	30	-	40	-	45	-	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	20	-	25	-	30	-	ns	
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	-	0	-	0	-	ns	9
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	-	0	-	0	-	ns	9
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	6	-	7	-	10	-	ns	10
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	30	-	40	-	45	-	ns	5

Parameter	Symbol	40 ns		50 ns		60 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Pulse Width	t_{WP}	6	-	7	-	10	-	ns	10
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	13	-	17	-	15	-	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	13	-	14	-	15	-	ns	
Data-In Setup Time	t_{DS}	0	-	0	-	0	-	ns	11
Data-In Hold Time	t_{DH}	6	-	7	-	10	-	ns	11
Data Hold Time Referenced to $\overline{RAS}$	t_{DHR}	33	-	40	-	45	-	ns	6
Refresh Time(256cycles)	t_{REF}	-	8	-	8	-	8	ms	
$\overline{WE}$ Setup Time	t_{WCS}	0	-	0	-	0	-	ns	5
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	60	-	70	-	85	-	ns	5
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	28	-	33	-	38	-	ns	5
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	38	-	43	-	53	-	ns	5
$\overline{CAS}$ Setup Time($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CSR}	5	-	5	-	5	-	ns	
$\overline{CAS}$ Hold Time($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	-	10	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5	-	5	-	5	-	ns	
$\overline{CAS}$ Precharge Time(CBR Counter Test Cycle)	t_{CPT}	20	-	20	-	20	-	ns	
Access Time from $\overline{CAS}$ Precharge	t_{CPA}	-	25	-	30	-	35	ns	3
Fast Page mode Read/Write Cycle Time	t_{PC}	30	-	35	-	40	-	ns	
Fast Page mode Read Modify Write Cycle Time	t_{PRWC}	65	-	80	-	90	-	ns	
$\overline{CAS}$ Precharge Time(Fast Page mode)	t_{CP}	7	-	8	-	10	-	ns	
$\overline{RAS}$ Pulse Width(Fast Page mode)	t_{RASP}	40	125000	50	125000	60	125000	ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	25	-	30	-	35	-	ns	
Access Time from $\overline{OE}$	t_{OEA}	-	10	-	13	-	15	ns	
$\overline{OE}$ to Delay Time	t_{OED}	8	-	10	-	13	-	ns	
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	8	0	10	0	13	ns	7
$\overline{OE}$ Hold Time	t_{OEH}	0	-	0	-	0	-	ns	
$\overline{WE}$ Hold Time(Hidden Refresh Cycle)	t_{WHR}	15	-	15	-	15	-	ns	

Notes

1. An initial pause of 200μs is required after power-up followed by any 8 $\overline{RAS}$ only Refresh or $\overline{CAS}$ before $\overline{RAS}$ Refresh cycles to initialize the internal circuit.

2. $V_{IH(min.)}$ and $V_{IL(min.)}$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH(min.)}$ and $V_{IL(max.)}$ are assumed to be 5ns for all inputs.

3. Measured with an equivalent to 1 TTL loads and 50pF.

4. For read cycles, the access time is defined as follows:

Input Conditions	Access Time
$t_{RAD} \leq t_{RAD(MAX.)}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{RAC(MAX.)}$
$t_{RAD(max.)} < t_{RAD}$ and $t_{RCD} \leq t_{RCD(MAX.)}$	$t_{AA(MAX.)}$
$t_{RCD(max.)} < t_{RCD}$	$t_{CACMAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ indicate the points which the access time changes and are not the limits of operation.

5. t_{WCS},t_{RWD},t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and the data output will remain high impedance for the duration of the cycle.If $t_{CWD} \geq t_{CWD(min.)}$,$t_{RWD} \geq t_{RWD\ (min.)}$ and $t_{AWD} \geq t_{AWD(min.)}$, then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data
out is indeterminate.

6. t_{AR},t_{WCR}, and t_{DHR} are referenced to $t_{RAD(max.)}$.

7. $t_{OFF(max.)}$ and $t_{OEZ(max.)}$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL}.

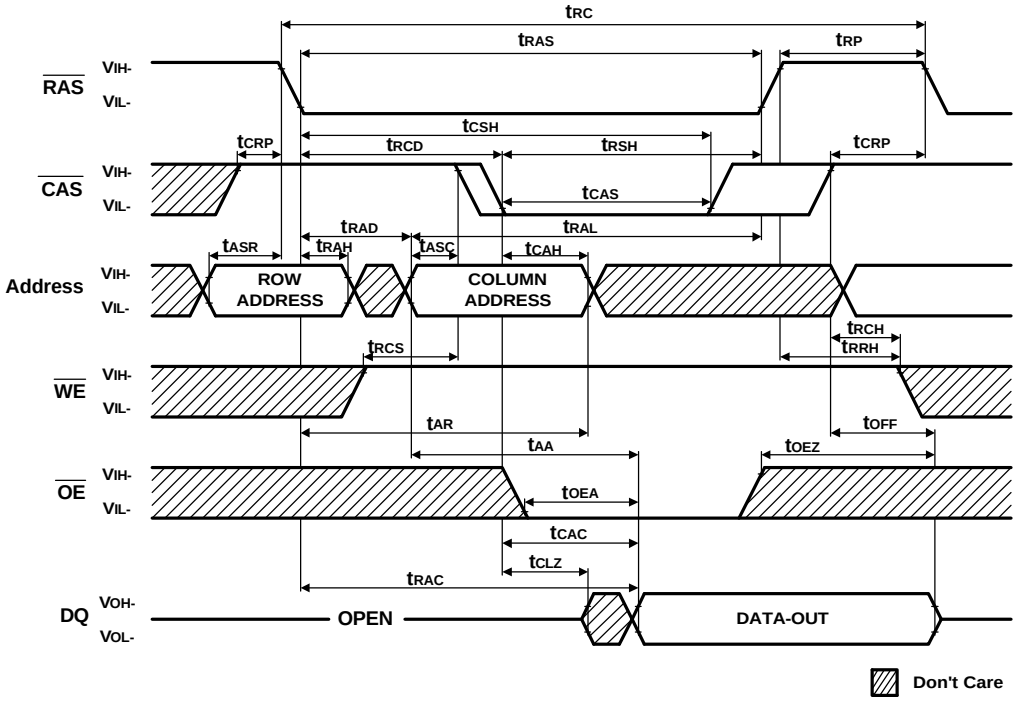
8. $t_{CRP(min)}$ requirement should be applicable for $\overline{RAS}$, $\overline{CAS}$ cycle preceded by any cycles.

9. Either $t_{RCH(min.)}$ or $t_{RRH(min.)}$ must be satisfied for a read cycle.

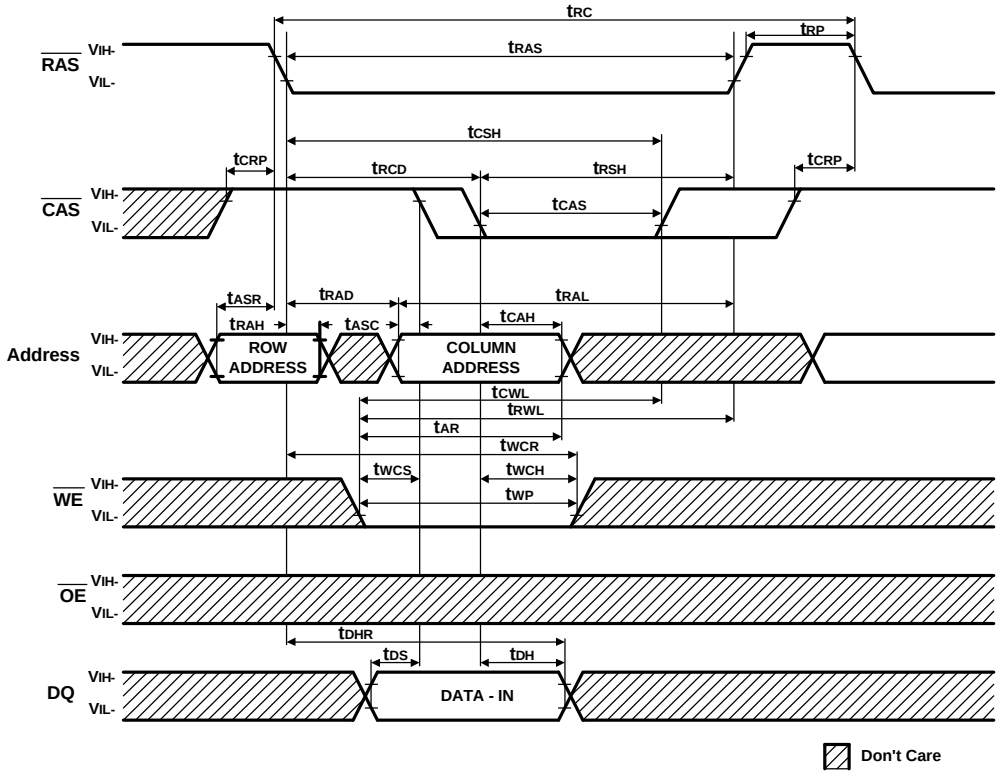
10. $t_{WP(min.)}$ is applicable for late write cycle or read modify write cycle. In early write cycles,$t_{WCH(min.)}$ should be satisfied.

11. This specification is referenced to $\overline{CAS}$ falling edge in early write cycles and to $\overline{WE}$ falling edge in late write or read modify write cycles.

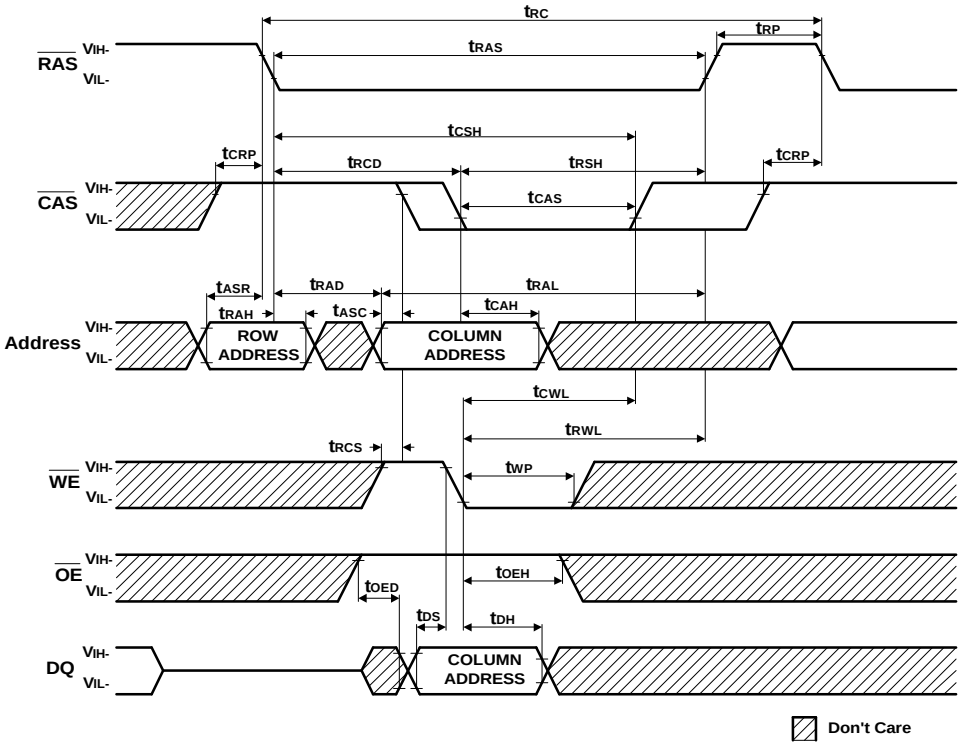
Read Cycle



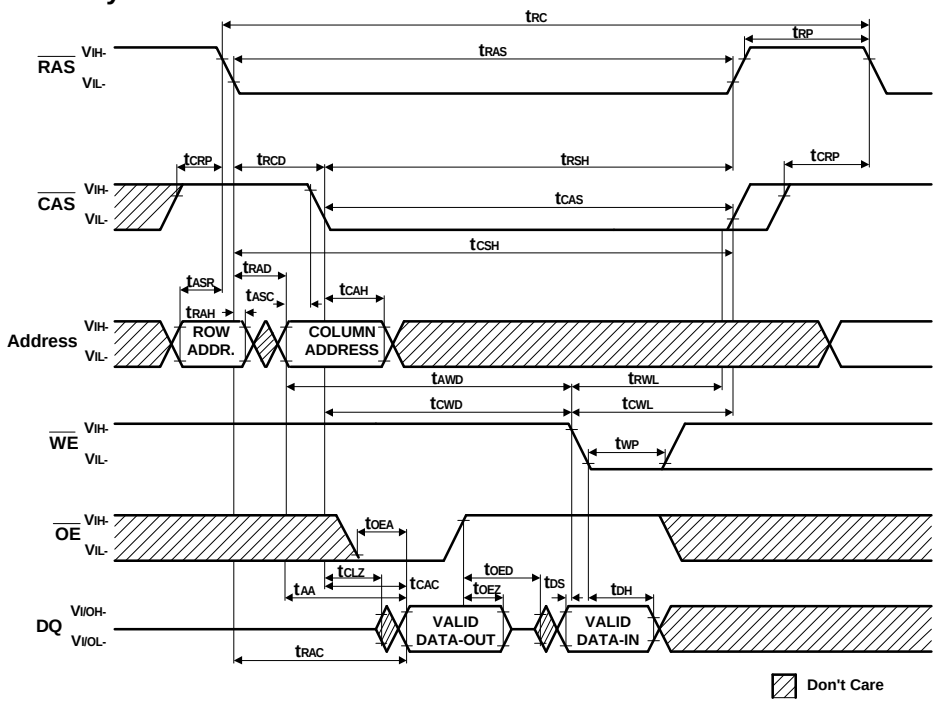
Early Write Cycle NOTE : D_{OUT} = Open



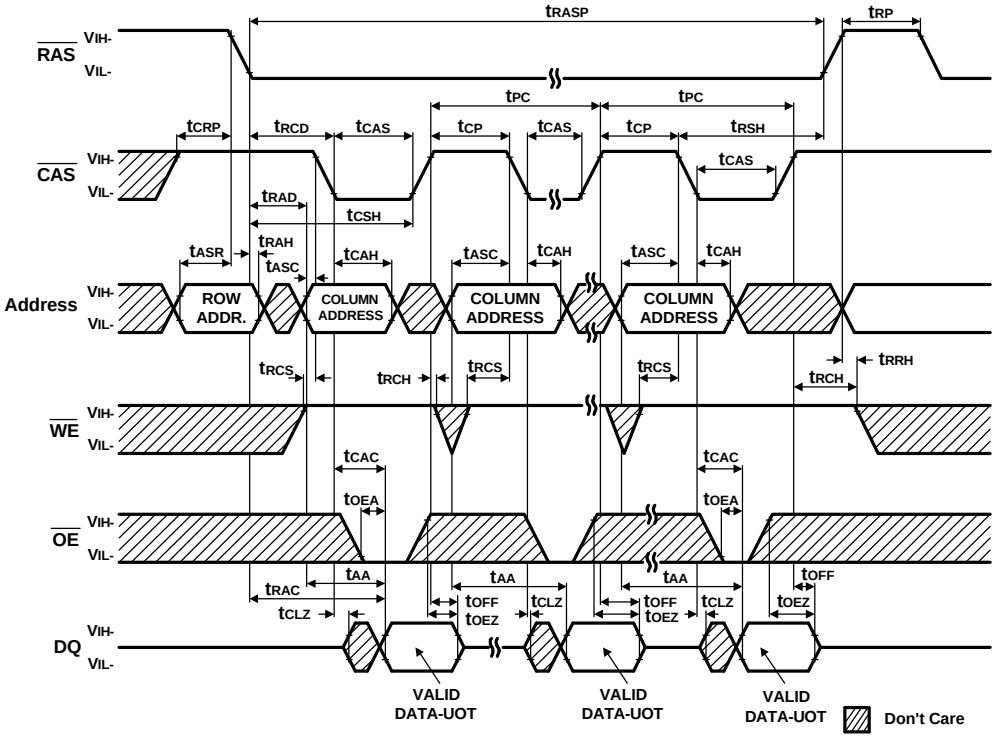
Late Write Cycle ($\overline{OE}$ Controlled Write) NOTE : D_{OUT} = Open



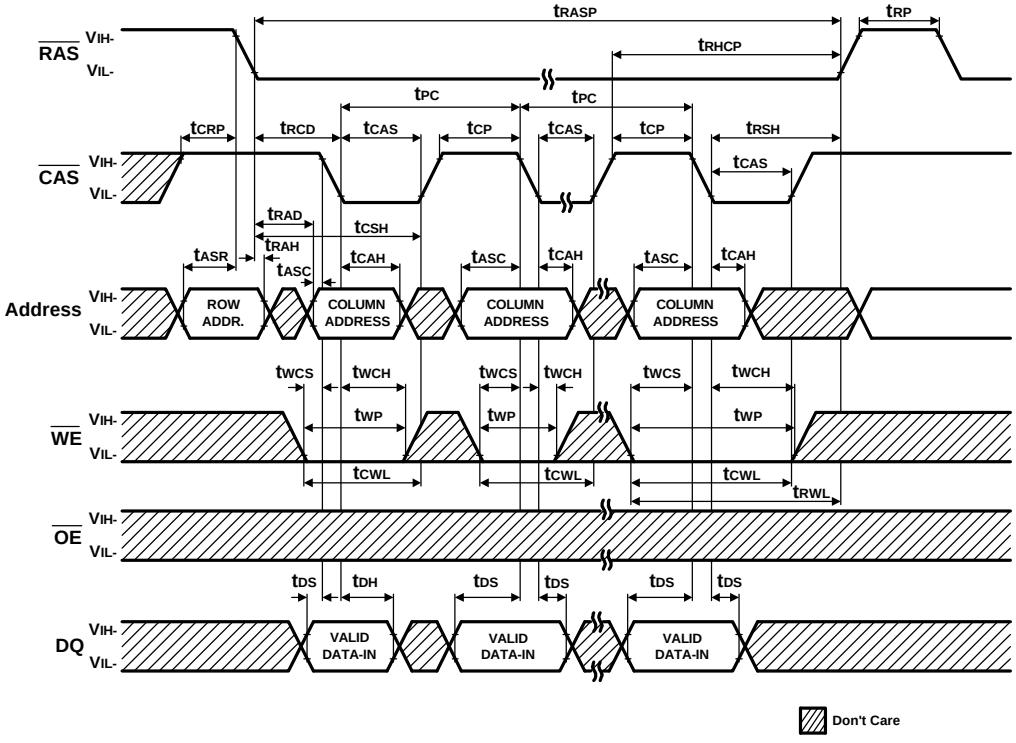
Read - Modify - Write Cycle



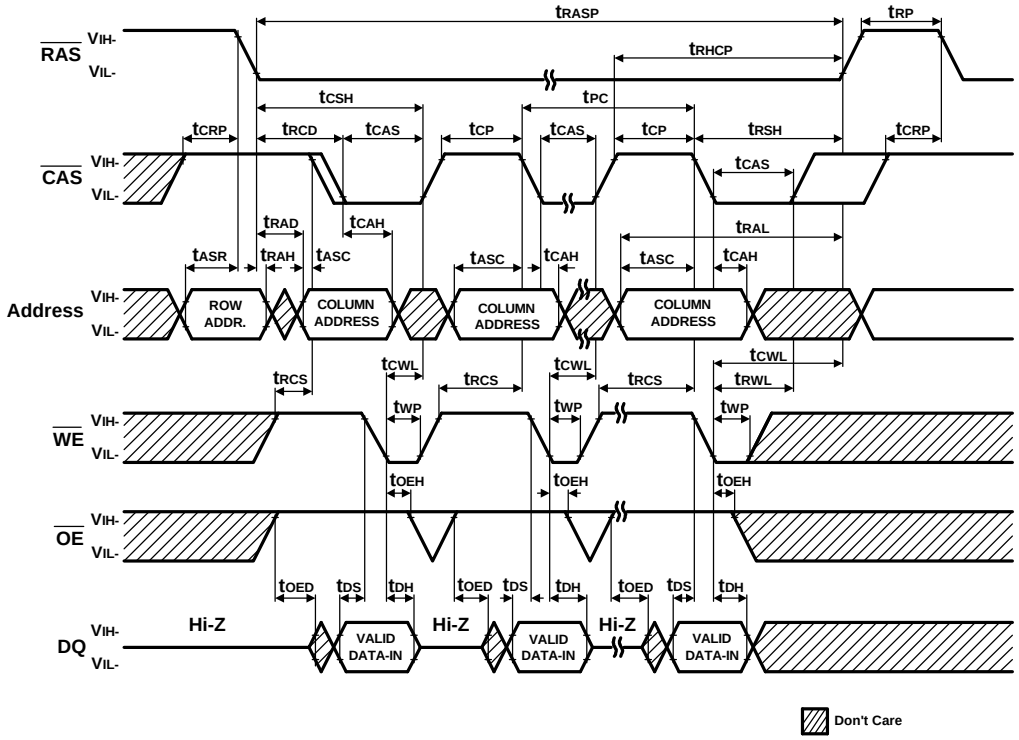
Fast Page Read Cycle



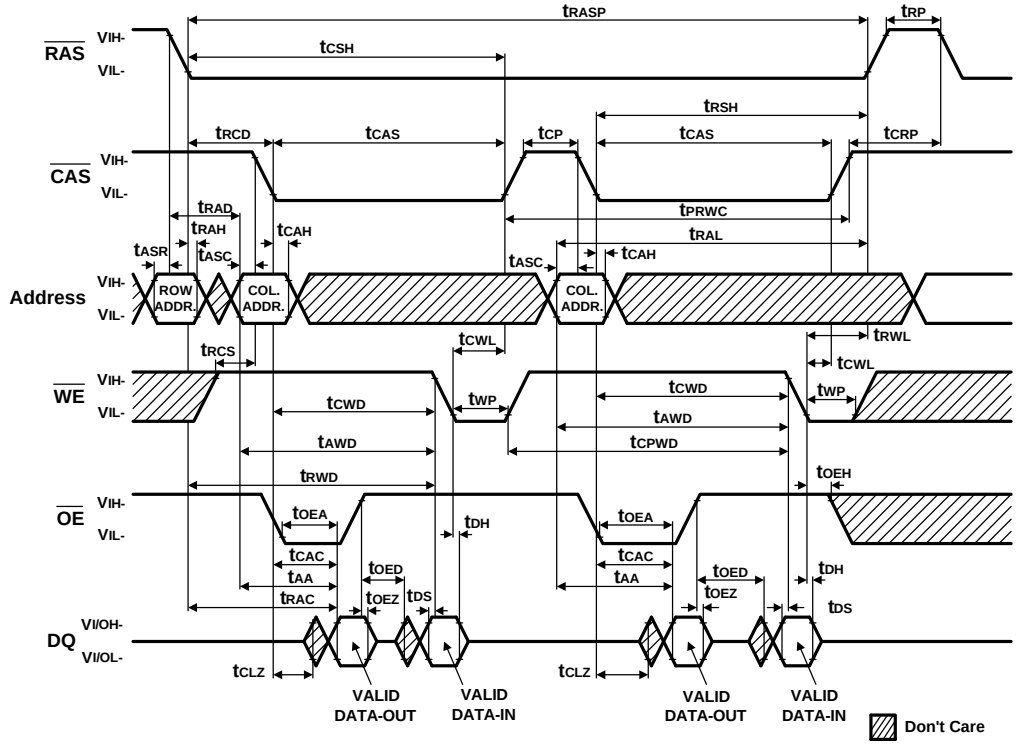
Fast Page Write Cycle NOTE : D_{OUT} = Open



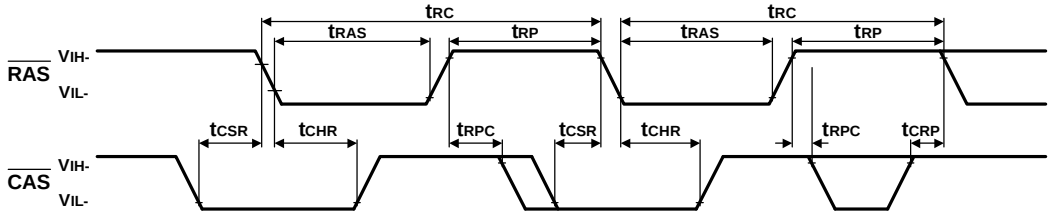
Fast Page Mode Late Write Cycle



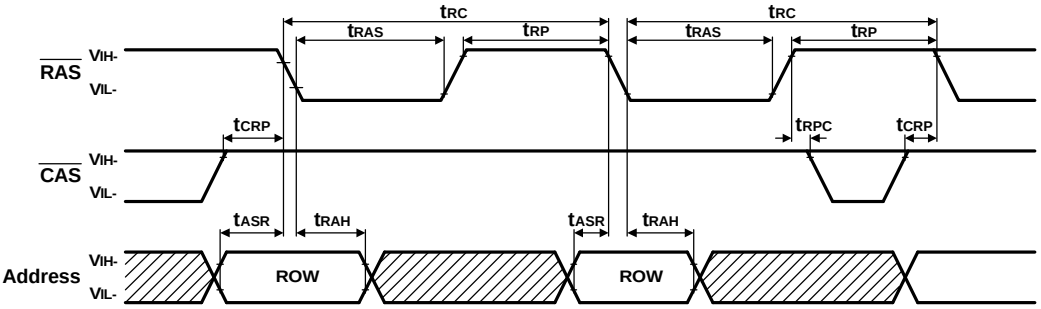
Fast Page Read - Modify - Write Cycle



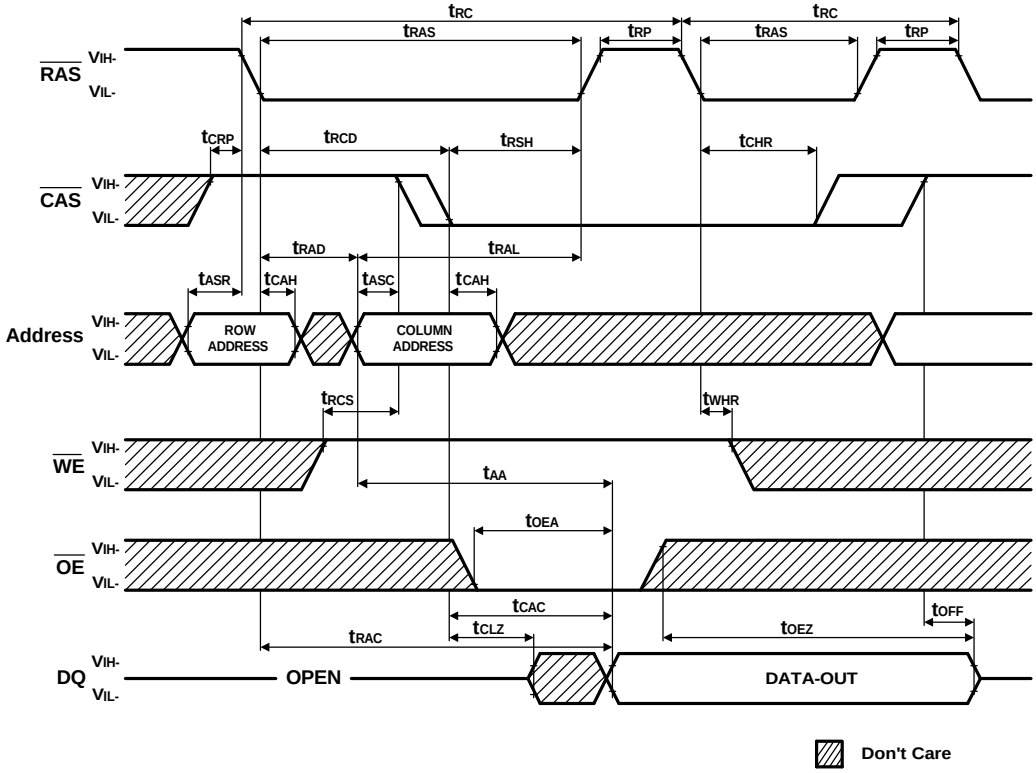
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



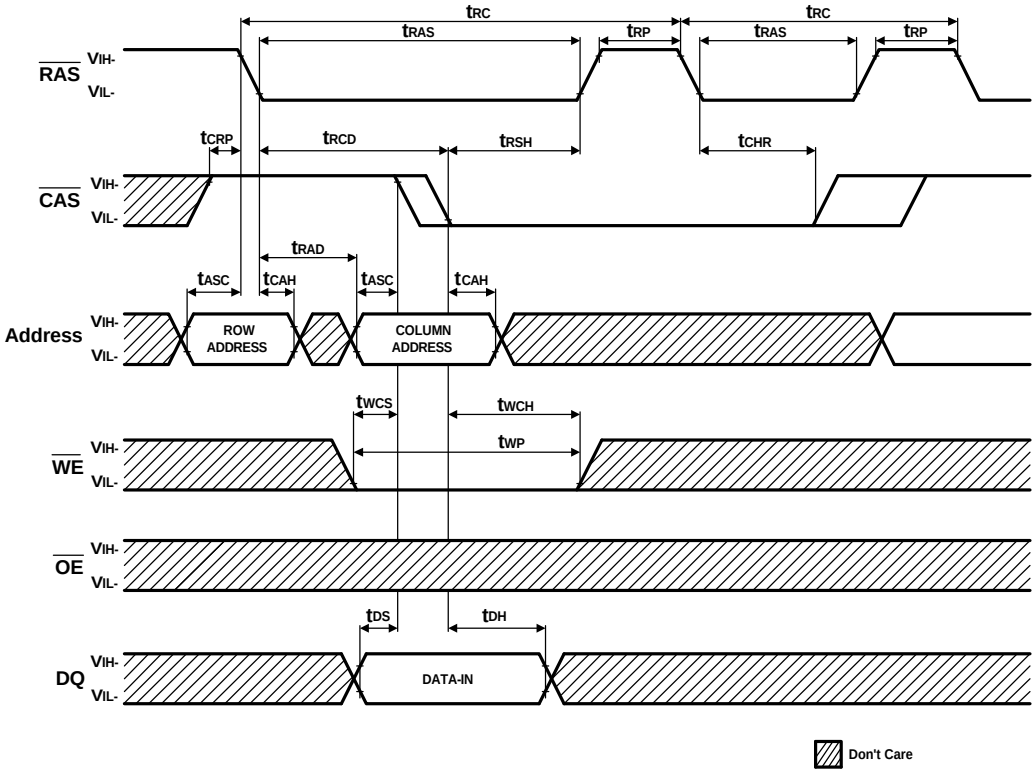
$\overline{RAS}$ -Only Refresh Cycle



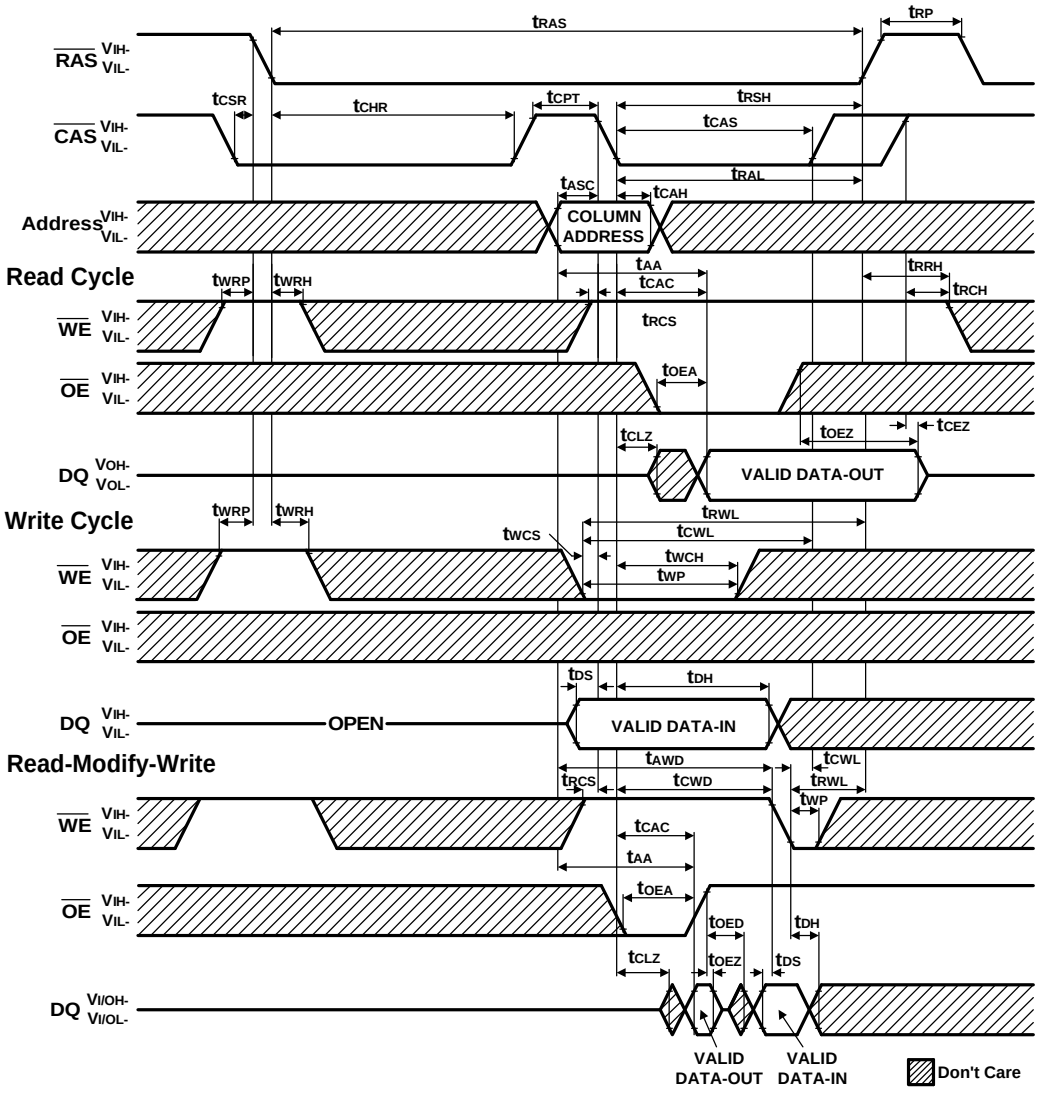
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write) NOTE : D_{OUT} =Open



$\overline{CAS}$ - Before $\overline{RAS}$ Refresh Counter Test Cycle



Ordering Information

Part Number	*SPEED*	*POWER*	*FEATURE*	*PACKAGE*
GLT44108-40J4	40ns	Normal	FPM	SOJ 400mil 28L
GLT44108-50J4	50ns	Normal	FPM	SOJ 400mil 28L
GLT44108-60J4	60ns	Normal	FPM	SOJ 400mil 28L

Parts Numbers (Top Mark) Definition :

GLT 4 41 _ 08 - 40 J4

4 : DRAM
6 : Standard SRAM
7 : Cache SRAM
8 : Synchronous Burst SRAM

-SRAM
064 : 8K
256 : 256K
512 : 512K
100 : 1M

-DRAM
10 : 1M(C/EDO)*
11 : 1M(C/FPM)*
12 : 1M(H/EDO)*
13 : 1M(H/FPM)*
20 : 2M(EDO)
21 : 2M(FPM)
40 : 4M(EDO)
41 : 4M(FPM)
80 : 8M(EDO)
81 : 8M(FPM)
*See note

VOLTAGE
Blank : 5V
L : 3.3V
M : Mix Voltage

CONFIG.
04 : x04
08 : x08
16 : x16
32 : x32

SPEED
-SRAM
12 : 12ns
15 : 15ns
20 : 20ns
70 : 70ns
-DRAM
35 : 35ns
40 : 40ns
45 : 45ns
50 : 50ns
60 : 60ns

PACKAGE
T : PDIP(300mil)
TS : TSOP(Type I)
TC : TSOP(Type II)
PL : PLCC
FA : 300mil SOP
FB : 330mil SOP
FC : 445mil SOP
J3 : 300mil SOJ
J4 : 400mil SOJ
P : PDIP(600mil)
Q : PQFP
TQ : TQFP

Note : C➔CDROM , H➔HDD.
Example :
1.GLT710008-15T 1Mbit(128Kx8)15ns 5V SRAM PDIP(300mil)Package type.
2.GLT44016-40J4 4Mbit(256Kx16)40ns 5V DRAM SOJ(400mil)Package type.

Package Information

400mil 28 Lead Small Outline J-form Package (SOJ)